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Enhanced stability of filament-type resistive switching by interface engineering

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The uncontrollable rupture of the filament accompanied with joule heating deteriorates the resistive switching devices performance, especially on endurance and uniformity. To suppress the undesirable filaments rupture, this work presents an interface engineering methodology by inducing a thin layer of NiO_x into a sandwiched Al/TaO_x/ITO resistive switching device. The NiO_x/TaO_x interface barrier can confine the formation and rupture of filaments throughout the entire bulk structure under critical bias setups. The physical mechanism behind is the space-charge-limited conduction dominates in the SET process, while the Schottky emission dominates under the reverse bias.

The modern non-volatile memory has been successfully scaled down to achieve ultra-high-density storage with the development of photolithography technology. However, the conventional charge storage memory is approaching the technical limit and three-dimensional (3D) crossbar structure would be a promising scaling scheme for next generation non-volatile memory^{1,2}. Resistive switching random access memory (RRAM) is favorable with its high-density 3D crossbar integration ability, fast operation speed and low power consumption^{3,4}. In the last two decades, oxide based RRAM has been intensively studied^{5,6}, and TaO_x has been recognized as one of potential choices due to its excellent endurance and retention performance^{7,8}. It is well acknowledged that there are only two stable stoichiometric solid phases in TaO_x: (a) high oxygen defective phase (or conductive path) and (b) low oxygen defective phase (or insulating matrix)^{9,10}. Such property guarantees relatively stable filaments formation in the TaO_x based RRAM devices^{11,12}.

However, nearly all the filaments-type RRAM could not avoid a critical issue that the RESET of device will involve the rupture of filaments, either by ion migration or Joule heating^{13,14}. This issue inevitably causes some negative effects, such as scattered switching voltage distribution and endurance deterioration^{15,16}. Recently, some groups have proposed different designs to improve the filaments property in TaO_x based RRAM. For example, Lee *et al.* has presented a so-called Metal-Insulator-Base-Metal (MIBM) structure to constrain the filaments in a thin highly insulating Ta₂O_{5-x} layer and to use another less insulating TaO_{2-x} layer as the reservoir of oxygen vacancies to enhance the filaments transition in the insulator layer¹⁷. By applying different voltages on the 1-transistor-1-memoristor (1T1M) device, Miao *et al.* realized the manipulation of the filaments in TaO_x which related to the oxygen vacancies, and obtained varying switching behavior¹⁸. However, these designs still involve the destruction of filaments at the interface area during the reset process, which infers to the abrupt decrease of current by several orders in the *I-V* characteristic^{19,20}. In this paper, we introduce a thin NiO_x layer between TaO_x and top electrode to introduce a barrier, which successively prevents the abrupt rupture of the filaments in the RESET process. Our proposal in using a hybrid structure of n-type TaO_x and p-type NiO_x interface engineering to control the formation of the filaments, instead of breaking and reconnecting them. Our design effectively improves the endurance and uniformity of resistive switching (RS) behavior, and offers an alternative design for future RRAM device.

Results

The bipolar RS cycles of ITO/TaO_x/NiO_x/Al device is demonstrated in Fig. 1a. The electroforming procedure is needed to initialize the resistive switching process (not shown here). As the arrow indicates, the device is initially at the high resistance state (HRS) and the switching cycle starts with a positive DC sweep. A dramatic current increment occurs at around 0.7 V, which corresponds to the SET operation, and the device reaches the low

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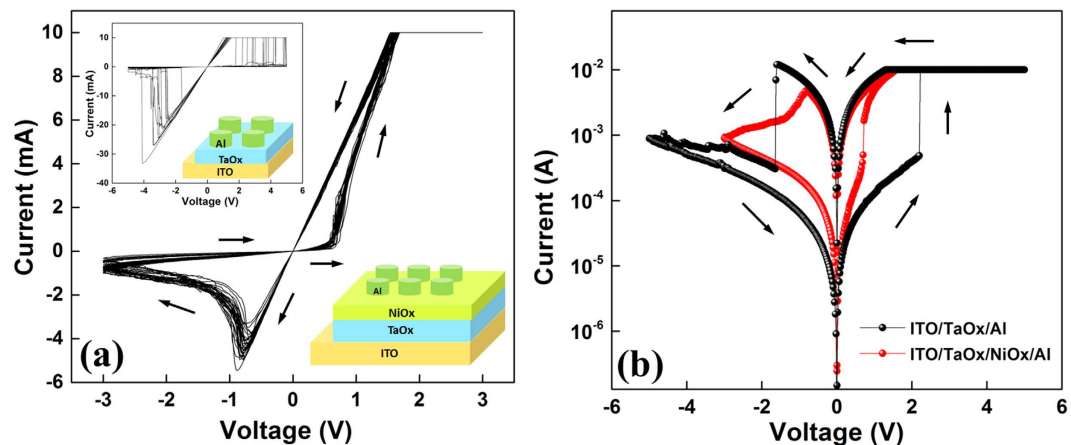


Figure 1. (a) The bipolar RS cycles and structure schematic of the ITO/TaO_x/NiO_x/Al device, the inset shows the switching cycles and structure schematic of device without the NiO_x layer; (b) Comparison of the switching cycles between the ITO/TaO_x/NiO_x/Al and the ITO/TaO_x/Al devices in $\log(I)$ -V scale.

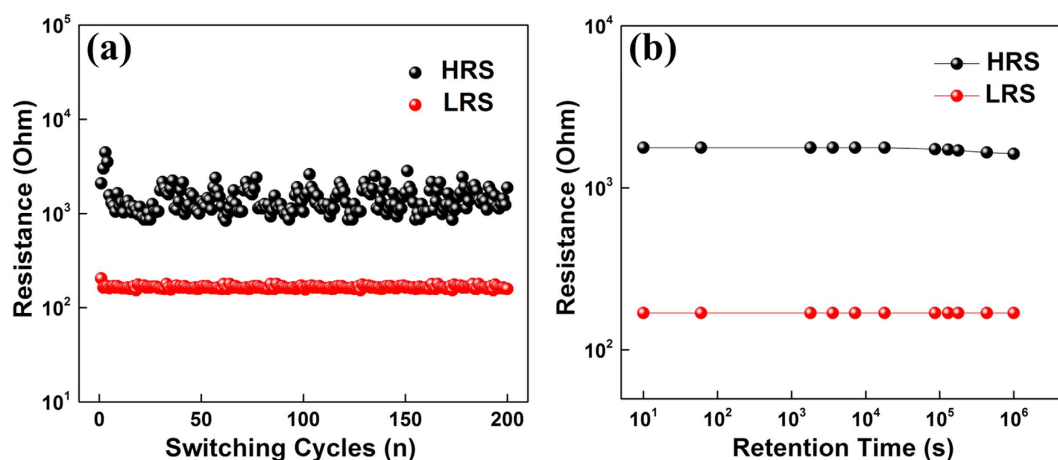


Figure 2. (a) Endurance performance of the ITO/TaO_x/NiO_x/Al RRAM; (b) Retention performance of the ITO/TaO_x/NiO_x/Al RRAM.

resistance state (LRS). A compliance current (CC) of 10 mA is imposed in order to prevent the permanent breakdown of oxide layers at >1.5 V. As the bias sweeps back from positive to negative region, the device maintains the linear I-V characteristics from 1.5 to ~ -0.8 V. The device is reset to HRS again and this completes one switching cycle. The same multiple switching cycles of the regular ITO/TaO_x/Al device (without the added NiO_x barrier) is also plotted in the inset of Fig. 1a. Several apparent distinctions could be noticed through the comparison. The distribution of the switching threshold voltage is more concentrated and the switching curves are more uniform for the device with the inserted NiO_x layer. The two batch of switching curves having different shapes could be further distinguished in the log-log I-V plotting as shown in Fig. 1b. The LRS behaviors of both two devices are similar, however, an obvious abrupt change of current in both SET and RESET processes could be observed only in the regular ITO/TaO_x/Al device, but not in our newly proposed ITO/TaO_x/NiO_x/Al design. The transition of the high and low resistance states becomes smoother after the introduction of NiO_x layer between TaO_x and top electrode, which indicates that two different switching mechanisms are present in these two different devices (see below).

The HRS and LRS resistance of ITO/TaO_x/NiO_x/Al device at 200 DC switching cycles is shown in Fig. 2a in order to characterize the endurance performance. The LRS resistance shows excellent consistency and the HRS resistance also becomes relatively stable after first several cycles. The resistance window is maintained well at about one order of magnitude difference, which is sufficient to realize binary storage. The retention characteristic at room temperature is shown Fig. 2b. After continuous sampling for around 10^6 s, the LRS resistance remains unchanged while the HRS resistance shows a little bit of decay after 10^5 s. These results manifest the potential application of non-volatile memory with such proposed device structure.

To further reveal the improvement by inserting a thin NiO_x layer into the ITO/TaO_x/Al structure, the cumulative distribution of switching voltages and two states resistance are also analyzed. In Fig. 3a, both SET and RESET voltages of ITO/TaO_x/NiO_x/Al device are highly centralized, which are respectively ranged from 0.64 to 0.78, and

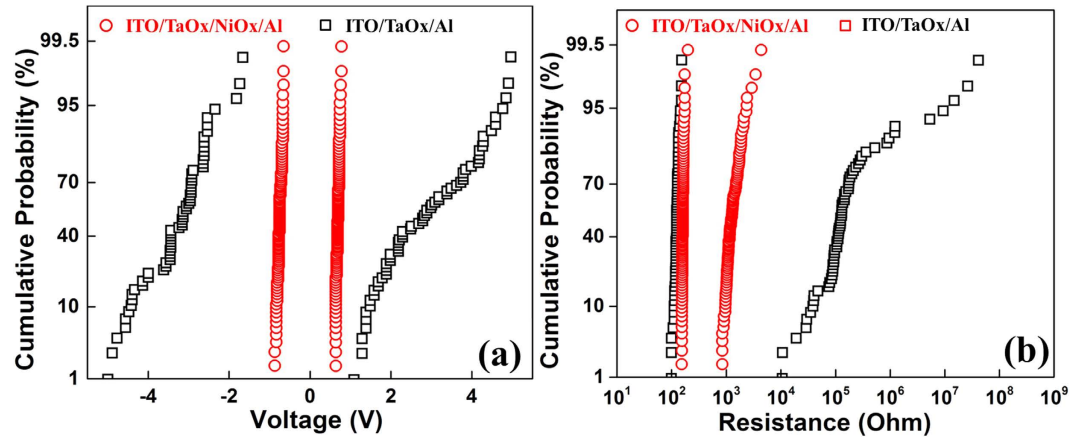


Figure 3. Cumulative probability comparison of (a) SET & RESET voltages, and (b) LRS & HRS resistances between the ITO/TaO_x/NiO_x/Al and the ITO/TaO_x/Al devices.

−0.68 to −0.88 volts, while the voltage distribution of ITO/TaO_x/Al one is much scattered (1.3 to 4.9 volts, −1.7 to −5.0 volts), which is consistent with the feature shown in Fig. 1. In Fig. 3b, the distributions of the LRS resistance of two devices are both in narrow range (100 Ω to 200 Ω); however, the distribution of the HRS resistance is greatly optimized in the ITO/TaO_x/NiO_x/Al structure (from a big range of 10 KΩ–100 MΩ to a smaller range of 1–4 KΩ). Moreover, the ITO/TaO_x/Al device only exhibits less than 100 stable switching cycles at our DC measurement, and the endurance has been improved with additional NiO_x layer as indicated in Fig. 2a.

Analysis and Discussions

To determine the mechanism for such a remarkable improvement by introducing a thin p-type NiO_x layer, the conduction properties of the as-prepared device and the RS processes are studied. Before electroforming operation, the as-prepared ITO/TaO_x/NiO_x/Al stacks are in the high resistance state. At this state, the *I*-*V* curves with increasing temperatures were plotted in log-log scale in Fig. 4a and b, and we can observe that the cases in the positive and negative sweep ranges are totally different. When the positive bias is applied on top electrode, the *I*-*V* curves all have a slope of around one at low voltage region (ohmic conduction), but gradually converge to *V_c* as the electric field increases as demonstrated in Fig. 4a. This is the typical behavior of the trap-limited-conduction^{21,22}. We consider the energy state of the traps solid is described by an exponential function $N(E) = N_t/(kT_t) \exp[(E - E_c)/kT_t]$, where *N_t* is the trap density, *E_c* is the band edge energy, *k* is Boltzmann's constant and *T_t* is the characteristic trap temperature. This regime is known as the trap-limited SCLC or Mark-Helfrich (MH) law²³ with its current density given by:

$$J_{MH} = N_c \mu e^{1-l} \left[\frac{\varepsilon_0 \varepsilon_r I}{N_t (l+1)} \right]^{\frac{1}{l}} \left(\frac{2l+1}{l+1} \right)^{l+1} \frac{V^{(l+1)}}{D^{(2l+1)}}, \quad (1)$$

where *N_c* is the effective density of states corresponding to the energy at the bottom of the conduction band, *μ* is the electron mobility, and *l* = *T_t*/*T* is the ratio of distribution of traps to the free carriers. The traps will be gradually filled as the electric field increased at all temperatures. When the applied voltage reach a critical value, all traps will be filled. This critical voltage is independent of temperature and given by ref. 22:

$$V_c = \frac{q N_t D^2}{2 \varepsilon_0 \varepsilon_r}, \quad (2)$$

where *q* is the electron charge. By extrapolating the *I*-*V* curves, we obtain a typical value for *V_c*, which is about 10 volts for our device. The electron transport behavior is confirmed to be in the trap-limited region.

When negative bias is applied, the *I*-*V* curves follow the Schottky emission²⁴:

$$I = AT^2 \exp \left[\frac{-q(\phi - \sqrt{qV/4\pi\varepsilon_0\varepsilon_r D})}{kT} \right], \quad (3)$$

where $A = 4\pi m e k_B^2 / h^3 = 1.2 \times 10^6 \text{ Am}^{-2} \text{ K}^{-2}$ is the Richardson constant, *T* is the temperature, *φ* is the barrier height. By re-plotting the *I*-*V* curves in the form of $\ln(I) - \sqrt{V}$ (see Fig. 4b), the linear and parallel feature at high (negative) voltage region agrees well with the Schottky emission process. Furthermore, the Arrhenius plots in Fig. 4c show the linearity of $\ln(I/T^2) - 1/T$ relationship, which also confirms the dominant conduction in the negative voltage region is Schottky emission²⁵. For comparison, we also analyzed the *I*-*V* characteristics of Al/NiO_x/Al and ITO/TaO_x/ITO stacks. It is found that the SCLC is the main conduction mechanism in these two stacks, which excludes the barrier effect at Al/NiO_x and ITO/TaO_x interfaces. Thus, we conclude the Schottky emission observed in ITO/TaO_x/NiO_x/Al is attributed to the n-type TaO_x and p-type NiO_x interface barrier.

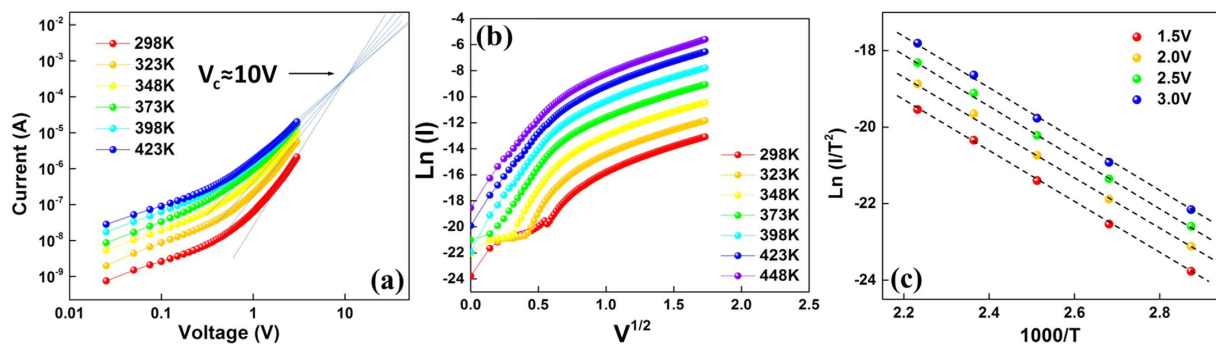


Figure 4. *I-V* characterization before electroforming process: (a) $\text{Log}(I)$ - V plotting under the positive bias; (b) $\text{Ln}(I) - V^{1/2}$ plotting under the negative bias; (c) Arrhenius plots of $\text{Ln}(I/T^2) - 1/T$ under the negative bias.

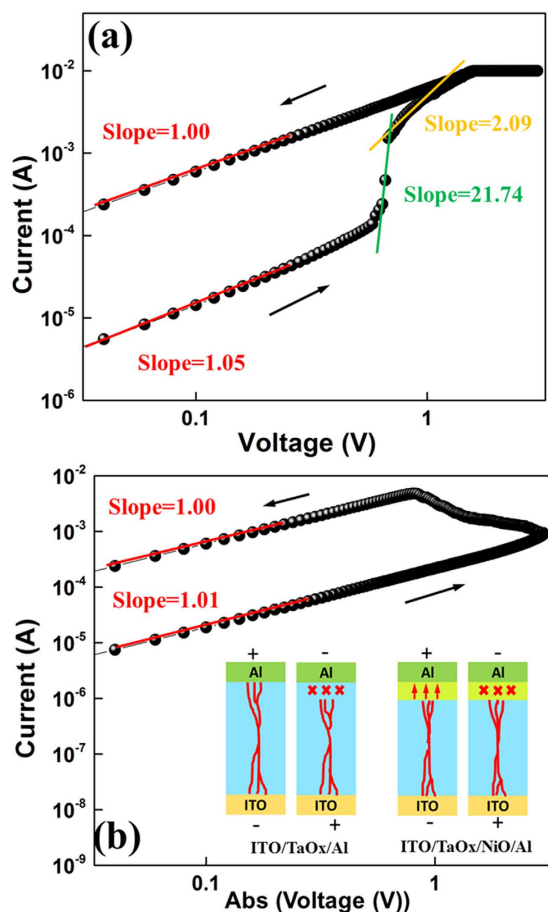


Figure 5. Log-log scale *I-V* characterization after electroforming process: (a) SET under the positive bias; (b) RESET under the negative bias.

The conduction properties in LRS and HRS are also investigated. From the *I-V* curves plotted in the log-log scale in Fig. 5a, a typical SCLC behavior in HRS could be identified. As the injected carriers are not comparable with intrinsic thermal carriers in low voltage region, ohmic conduction with slope of about 1 ($= 1.05$ indicated in Fig. 5a) is expected. The current density depends proportionally on the concentration of thermally generated carriers n_0 , given as

$$J_{Oh} = n_0 q \mu \frac{V}{D}. \quad (4)$$

With higher injecting current density, the injected carriers promptly fill the traps in the oxides, which lead to a high current gain with a slope of 21.74. These traps are well known to be as oxygen vacancies for n-type TaO_x and

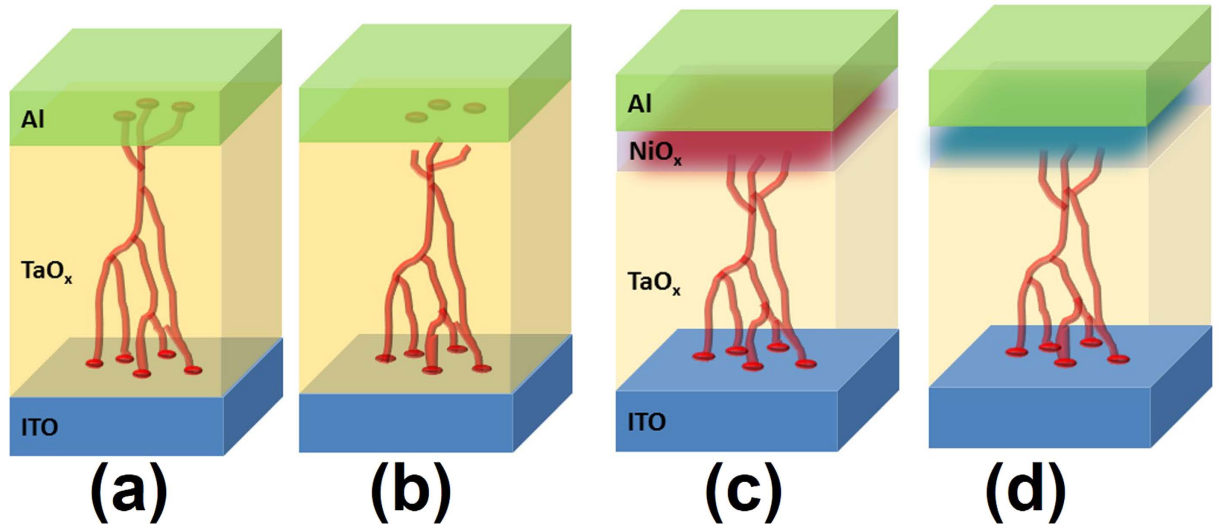


Figure 6. Schematics of the resistive switching mechanism comparison between (a,b) the ITO/TaO_x/Al, and (c,d) the ITO/TaO_x/NiO_x/Al RRAM devices.

Ni vacancies for p-type NiO_x. This region is known as the trap-limited SCLC or Mark-Helfrich (MH) law²³ given by Eq. (1) with slope $I + 1$. When the traps are gradually occupied fully, the slope reduces to around 2 ($= 2.09$ indicated in Fig. 5a), indicating that the conduction enters the trap-free SCLC, and the current density is determined by the Mott-Gurney (MG) law^{26,27}:

$$J_{MG} = \frac{9}{8} \varepsilon_0 \varepsilon_r \mu \frac{V^2}{D^3}. \quad (5)$$

For the LRS, the high current with ohmic conduction is the standard metallic property of filament formed in oxide²⁸. In the RESET process as shown in Fig. 5b, the ohmic behavior with the slope of 1 is still maintained in LRS until the filament based conduction is gradually impeded and the device gets back to HRS. The slope of 1 in HRS corresponds to the low thermal current in oxide again.

Based on the above results, the different RS process in these two stacks could be described by taking into the consideration of both filaments and interface barriers effects (see Fig. 6). For a ITO/TaO_x/NiO_x/Al device (Fig. 6c), the positive voltage on top electrode will reduce the TaO_x/NiO_x barrier and enables injected electron hopping among the traps (usually oxygen vacancies in TaO_x) to realize the conduction throughout the whole stacks²⁹. When the voltage increase, we enter the SCLC regime, and the oxygen vacancies migrate along the applied field (to the bottom ITO/TaO_x interface), which will trigger soft dielectric breakdown from bottom up. When the filaments formed completely with the migration of oxygen vacancies and successively passed through the n-TaO_x/p-NiO_x interface to the top electrode, the device is set to LRS states. Concurrently, the oxygen vacancies in NiO_x will be extracted to TaO_x with the positive bias, which will also make both oxide layers to be more conductive to facilitate the filament based conduction. Thus the LRS is sustainable even after removing the external field due to the existence of filament, which satisfies the non-volatile storage.

Subsequently, when negative voltage is applied on the top electrode (Fig. 6d), the filamentary conduction still maintains in a small region. However, the increasing reverse bias on n-TaO_x/p-NiO_x junction will raise the barrier height and hinder the conduction to reset the device to HRS. Similarly, the negative voltage will also absorb some oxygen vacancies from TaO_x back into NiO_x and make them to be highly resistive, further impeding the reverse current. It is worth to mention that the filaments in TaO_x are not broken here, because the current is reducing gently instead of abrupt drops as shown in Fig. 1b. This provides the evident that the gradually rising TaO_x/NiO_x barrier weakens the filamentary conduction through the interface, avoiding the rupture of filaments. Therefore, the next SET cycle will only need to lower the barrier and enable the filaments passing through again without the requirement of reconnecting or repairing any rupture filaments.

For the traditional ITO/TaO_x/Al device (Fig. 6a and b), a filament rupture procedure at TaO_x/ITO interface with negative bias is required in RESET operation, which is consistent to a sudden current drop of several orders depicted in Fig. 1b³⁰. From the comparison, we could understand that the improvement of RS by inserting a NiO_x layer is mainly ascribed to employing an interface barrier effect to control the filaments conduction without making any destructive operation on the filaments as in the RS processes. The resistance fluctuation, especially in the HRS, is greatly suppressed because the HRS originates from the reverse bias of barrier, not from the randomly broken filaments. The switching threshold value is also optimized because tuning the barrier height is much more stable than the ruinous handling of filaments. At the same time, a better endurance could be also obtained by selecting this gentle RESET strategy. The major defect in NiO_x is Ni vacancy, so under the reverse bias, the oxygen vacancies migrate into NiO_x, counteracting the Ni vacancies and form more stoichiometric NiO which are higher resistive. The process is similar like the formation of space charge region in PN junction, which is due to the major carrier election in N region diffusing into P region. Such process somehow causes some so-called “damage” on

the filament but only at the TaO_x/NiO_x interface region. Such “damage” is actually a part of the “barrier tuning filament” effect, and will not affect the whole filament establish inside TaO_x.

Summary. In conclusion, an interface engineering resistive switching device of ITO/TaO_x/NiO_x/Al structure was designed and fabricated. The device shows an enhanced improvement in the endurance performance and the distribution of switching voltages and resistance over the traditional ITO/TaO_x/Al structure. For the as-prepared device, SCLC is the main conduction mechanism in the positive bias regime, and Schottky emission dominates the conduction in negative bias regime, which proves the formation of a confined TaO_x/NiO_x interface barrier. The introduction of such an interface barrier with TaO_x can control and manipulate the passing status of filaments efficiently. The proposed design avoids the rupture of filaments in RESET process, which will enable a more uniform and stable resistive switching behavior comparable to other RRAM devices^{12,17,31}.

Experiment Section. The Al/NiO_x/TaO_x/ITO RRAM devices were fabricated by magnetron sputtering system at room temperature. The ITO commercial glass was employed as the substrate for deposition and bottom electrode. A 50 nm n-type TaO_x layer was deposited by using a Ta₂O₅ target with the RF sputtering power of 100 W. The pressure sputtering chamber was maintained at an Ar (Argon) atmosphere of 5×10^{-3} Torr. A 10 nm p-type NiO_x layer followed in the same chamber atmosphere by using a NiO target with the RF power of 70 W. Lastly, a 200 nm Al top electrode layer was deposited with a shadow mask by using DC sputtering power of 60 W. A traditional ITO/TaO_x/Al RRAM device was also fabricated for comparison. The conduction type of TaO_x and NiO_x were confirmed by Hall effect measurement. *I-V* characterization was carried out on a probe station with the Keithley 4200 SCS semiconductor parameter analyzer. During the DC mode measurement, the biases with different polarities were applied on the Al top electrode and the ITO bottom electrode was always grounded.

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Author Contributions

Y.B. Zhu and X. Wu designed the experiments. K. Zheng fabricated the RRAM device. Y.B. Zhu carried out the electrical measurements and did the modeling on the space-charge mechanism. X. Wu and L.K. Ang analysis the data. All authors read and revised the manuscripts.

Additional Information

Competing financial interests: The authors declare no competing financial interests.

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