

http://pubs.acs.org/journal/acsodf

Article

Enhanced Graphene Oxide Electrical Properties for Thin-Film Electronics Using an Active/Shrinkable Substrate

Heba N. Abunahla, Humaira Zafar, Dalaver H. Anjum, Anas Alazzam, and Baker Mohammad*

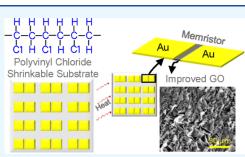
-								
	Cite	This:	ACS	Omega	2023,	8,	1671–1676	



ACCESS

III Metrics & More

ABSTRACT: The advances in material science along with the development of fabrication techniques have enabled the realization of thin-film-based electronics on active substrates. This has substantially enhanced and supported the deployment of electronic devices in several emerging applications with flexible functionality. In this work, we report a novel fabrication of graphene oxide (GO)-based memristor devices on an active/shrinkable substrate. The standard lithography process is used to fabricate planar Au–rGO–Au devices on a polymer substrate that has the ability to shrink at a certain temperature (i.e., 170 °C). Upon heating, the devices are shrunk to 50% of their original size. A detailed electrical characterization has been carried out to study the switching behavior of the fabricated devices before and after shrinking. The results prove that upon



Article Recommendations

shrinking, the device preserves its switching ability with enhanced electrical parameters (i.e., switching voltage). Also, material characterization performed for the deposited GO on the active substrate shows improved properties of the GO film due to the enhanced arrangement of GO flakes after shrinking. The novel approach proposed in this work provides new insights into and offers the ability to scale thin-film electronics postfabrication and thus overcome some of the device scaling challenges due to manufacturing limitations. It also unfolds a new path for the realization of GO-based electronic devices with improved electrical properties, which is a crucial aspect of the development of highly flexible and lightweight green electronics.

■ INTRODUCTION

Among the available memory technologies, emerging memristor (MR) devices that exhibit ionic resistance switching¹ provide outstanding electrical features that can accommodate the reliability of deploying nonvolatile memories in several emerging applications. MR device is considered the fourth fundamental circuit element. It was postulated by Chua in 1971 and has been physically synthesized by HP laboratories in 2008.² Since then, a growing interest has been directed toward developing MR devices for several applications, such as memory, computing, sensing, security, and communication systems.^{3,4} This is due to the outstanding features of MR devices that can overcome the limitations associated with complementary-metal-oxide-semiconductor (CMOS) technology in terms of scalability and leakage power.

MR is a two-terminal device that consists of a metal/ insulator/metal planar or vertical stack. Numerous metal oxide materials (i.e., TiO₂, CuO, and ZnO) have been deployed as the insulating/switching layer in MR devices.¹ Recently, researchers have been actively exploring the utilization of graphene oxide (GO) as the active switching layer in MR devices⁵ due to its high flexibility, lightweight, and ultrahigh specific stiffness,⁶ which can substantially enhance the electrical/mechanical properties of the device.

Not long ago, fabricating thin-film electronics on active substrates has become a crucial research interest. This has been

facilitated by advances in material sciences and the development of fabrication techniques. As shown in Figure 1, active substrates may have different properties, such as flexibility, bendability, stretchability, and shrinkability.⁷ The selection of the active substrate and consequently the associated feature are mainly linked to the desired functionality for the target applications. Few research efforts have reported the fabrication of GO-based memristive stacks on a flexible substrate, targeting wearable electronics applications.^{8–13}

To the best of our knowledge, this is the first work to report on GO-based MR devices fabricated on a flexible shrinkable substrate. The proposed approach improves the properties of the GO thin film. Moreover, it allows for downsizing the device dimensions after the lithography process is performed.

MATERIALS AND METHODS

Figure 2a details the fabrication process followed in this work. As shown, the active substrate, made from poly(vinyl chloride)

Received: November 14, 2022 Accepted: December 8, 2022 Published: December 16, 2022





© 2022 The Authors. Published by American Chemical Society

Active Substrates

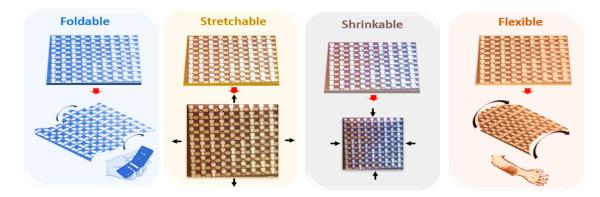


Figure 1. Examples of active substrates: foldable, stretchable, shrinkable, and flexible.

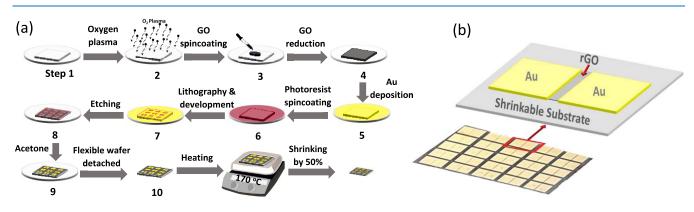


Figure 2. (a) Fabrication steps followed to achieve the rGO MR devices presented in this work. (b) Photograph and schematic of the planar MR device consisting of Au/rGO/Au fabricated on the active/shrinkable electrode.

(PVC), is mounted on a dummy wafer for support purposes (Step 1). In Steps 2 and 3, oxygen plasma is performed (PDC-002 from Harrick Plasma), followed by the deposition of GO (4 mg/mL dispersion in water from Sigma-Aldrich). The deposition is performed using a spin coater at a speed of 2000 rpm for 30 s (WS650Hzb-23NPP UD-3 from Laurell Technologies Corporation). After that, the wafer is immersed in hydroiodic acid (47% ACS Reagent, Sigma-Aldrich, St. Louis, MO) for a duration of 4 h to reduce the deposited GO film (Step 4). Then, the standard lithography/etching process is followed to pattern the planar electrodes (Steps 5-9). This includes Au deposition using a DC sputter (Q300 TT from Quorum Technologies), photoresist deposition (PR 1813 from MicroChem) using a spin coater, patterning the photoresist layer using a photolithography system (Dilase KLOE 650), photoresist development (Microposit MF-319 Developer from MicroChem), Au etching, and then performing the liftoff process using acetone. In Step 10, the shrinkable substrate is detached from the dummy wafer. Finally, the substrate is placed on a hot plate (170 °C) for 20 s.

It is worth mentioning that by adding isopropanol to the GO dispersion, the concentration of the GO solution is adjusted to 1 mg/mL. Isopropanol improves the spin-deposited film. The thickness of the deposited layer was measured using AFM microscopy to be between 10 and 50 nm.¹⁴

Figure 2b shows the photograph of the fabricated devices and a schematic that describes the device structure consisting of a reduced GO (rGO) layer sandwiched between two planar gold electrodes.

RESULTS AND DISCUSSIONS

Here, detailed material characterization is performed to analyze the properties of the used active substrate before and after shrinking, with and without GO. The obtained SEM images of the samples with GO-coating and without GO-coating are shown in Figure 3a-d. A comparison between the shrunk and unshrunk cases is made for these samples. There are several differences and similarities between the samples. The surfaces are found to have undulations, pinholes, and cracks depending upon the sample type. For instance, the surface polymer is found to have holes after the shrinking of these samples. While similar morphologies are observed on the surfaces of GO/ polymer before the application of the shrinking process. However, interestingly, the delamination (or the buckling) of GO from the polymer surfaces is observed after the application of the shrinking process. The observed buckling or delamination of the GO layer occurs due to a different thermal coefficient of polymer compared to GO, as described in the literature.^{15–17}

Moreover, transmission electron microscopy (TEM) is performed to further explore the changes in the GO film before and after shrinking. For TEM analysis, GO layers are scratched from the unshrunk and shrunk substrates with a razor blade. The scratched pieces are collected in a vial using ethanol. TEM specimens are prepared by casting a drop of GO-containing ethanol solution of each sample on a conventional quantifoil-multiA carbon-coated copper grid. The prepared specimens are air-dried for several hours prior

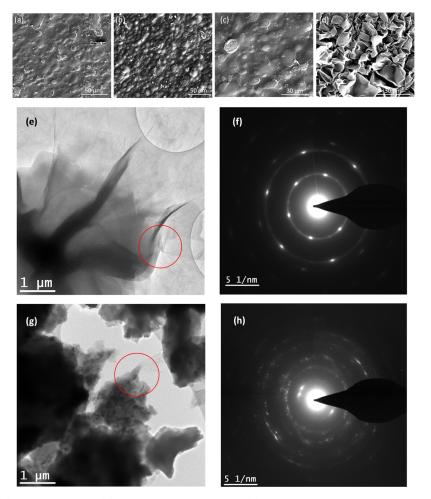


Figure 3. SEM images of (a) pristine substrate, (b) shrunk uncoated substrate, (c) unshrunk substrate coated with GO, and (d) shrunk substrate coated with GO. (e, f) BF-TEM image and SAED pattern of the unshrunk substrate, respectively. (g, h) BF-TEM image and SAED pattern of the shrunk substrate, respectively.

to performing TEM analysis. The TEM analysis of GO specimens is performed by an electron microscope (model Titan 80-300ST from ThermoFisher Scientific) at an accelerating voltage of 300 kV. The microscope is set to bright-field TEM (BF-TEM) mode to investigate the morphology by acquiring images at different magnifications. Selected area electron diffraction (SAED) patterns are also acquired to determine the structure of GO sheets. Both images and diffraction patterns are recorded using a charge-coupled device (CCD) of model US1000 from Gatan, Inc.

Figure 3e,f shows the BF-TEM image and SAED pattern of GO before shrinking, respectively. The lighter regions in the BF-TEM image show a sheet morphology, while darker regions show rotated/twisted regions of the multilayer GO. The SAED area shows a diffraction pattern produced from both regions of GO, as shown by the red circle in the BF-TEM image. The *d*spacing reported in Table 1 shows that the crystal structure of GO closely matches the hexagonal structure of graphene. The 0.35 nm spot (or 001 planes) indicates both thin GO and the possible presence of graphene in the unshrunk samples. The individual spots in the SAED are from the lighter regions, whereas the ringlike pattern is a characteristic of a polycrystalline GO sample, i.e., from the darker regions in the BF-TEM image. This implies that thick GO regions contain a polycrystalline structure. The intense spots in SAED indicate the preferred stacking orientations of GO layers.

Table 1. <i>d</i> -Spacing	(Interplanar)	Spacing) in	GO before and
after Shrinking			

d-spacing	for unshrunk GO	d-spacing for shrunk GO		
spot no.	d-spacing (nm)	spot no.	d-spacing (nm)	
1	0.2112	1	0.3459	
2	0.1215	2	0.1966	
3	0.1053	3	0.1548	
4	0.07927	4	0.1165	
5	0.06979	5	0.09763	

As for the BF-TEM image and SAED pattern shown in Figure 3e,f for the shrunk substrate, GO undergoes dramatic morphological changes during the shrinking of the substrate. The presence of fewer light regions is indicative of the fact that GO becomes much thicker during the shrinking process of the substrate. The SAED shows a diffraction pattern produced from both regions of GO, as shown by the circle inserted in the BF-TEM image. The *d*-spacing table shows that the crystal structure of GO closely matches the hexagonal structure of graphene. The presence of 0.35 nm spot (or 001) planes implies that some of the GO transformed into graphite oxide. The complete disappearance of individual intense spots in the SAED pattern indicates that the layers of GO got rotated/ twisted with respect to each other. This situation may be related to the nature of the observed electrical properties of

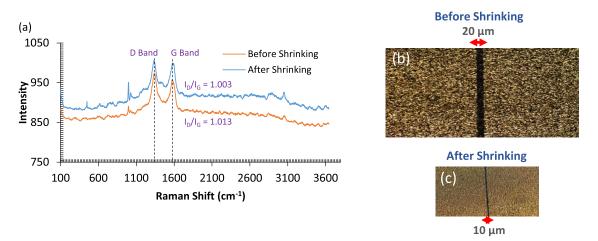


Figure 4. (a) Raman spectroscopy for the substrate coated with GO before and after shrinking. (b, c) Microscopic images of the fabricated device before and after shrinking, respectively.

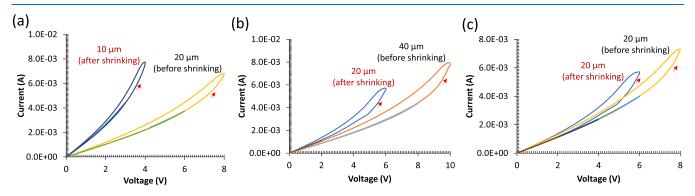


Figure 5. Electrical characterization results for (a) a 20 μ m device before shrinking and after shrinking to a 10 μ m device, (b) a 40 μ m device before shrinking and after shrinking to a 20 μ m device, (c) fabricating a 20 μ m device and a 40 μ m device after shrinking to a 20 μ m device.

Table 2. Comparison between the Flexible Shrinkable MR Device Reported in This Work and the Flexible GO-Based MR Devices Available in the Literature

ref	device structure	bending radius (mm)	switching material deposition	flexible substrate	shrinkable substrate
8	Al/GO/Al/PES	7	spin casting	\checkmark	×
18	rGO/(ZnO NRs)/Au/PET	6	spin coating	\checkmark	×
13	rGO/(g-C3N4-NS)/rGO/PET	8	spray coating		×
11	Al/Au-rGO/ITO/PET	N/A	spin casting		×
19	Al/GO/ITO/PET	4	spin coating		×
10	Al/carboxymethyl cellulose-GO (CMC-GO)/Al/PET	20	spin coating		×
this work	Au/rGO/Au	2	spin coating	\checkmark	\checkmark

GO on the shrunk substrates. This implies that thick GO regions contain a polycrystalline structure.

Figure 4a shows the Raman spectroscopy for the active substrate coated with GO before and after shrinking. The D-band and G-band intensity ratio (I_D/I_G) is calculated to determine the sp² carbon atoms density of defects. As shown, I_D/I_G slightly decreases after shrinking/heating, suggesting an increase in the ordering of sp²-bonded graphitic domains.¹⁸

A Keithley 4200-SCS parameter analyzer is used to perform the electrical characterization of devices fabricated with different rGO gaps of 20 and 40 μ m between the Au electrodes. Figure 5a presents the *I*–*V* characteristics of the 20 μ m device before and after shrinking. First, 6 V dual sweep voltage is applied across the unshrunk device and no switching takes place. Thus, the applied sweeping voltage is increased to 8 V and the device resistance switches from the high-resistance state (HRS) to the low-resistance state (LRS). After heating and shrinking the device, it can be observed that the device exhibits resistance switching under the application of 4 V. The same approach is followed for the device fabricated with a 40 μ m gap. As presented in Figure 5b, before shrinking, the device switches from HRS to LRS at 10 V, compared to a 6 V switching voltage after shrinking. In Figure 5c, the I-Vcharacteristic of the devices fabricated originally with a 20 μ m rGO gap is compared with the characteristics of the 20 μ m device achieved after shrinking. It is clear that the fabrication process reported in this work provides enhanced properties of the deposited GO and consequently switching is attained at a lower voltage. It is worth mentioning that the switching characteristics obtained in Figure 3 can be tuned by tuning the gap dimension, the electrode material, and the GO reduction time during fabrication.

Table 2 compares this work with the GO-based MR devices available in the literature and fabricated on active substrates. It is clear that the memristive system reported in this work is the first to provide the shrinkable property to GO-based MR devices. This would significantly reduce the fabrication cost via scaling devices using heat rather than lithography. This approach can be a great milestone for underdeveloped areas of research and potential future advances of GO-based thinfilm electronics.

CONCLUSIONS

This work presented a novel approach to fabricate GO-based electronic devices. To the best of our knowledge, this work is the first to study the behavior of GO on an active substrate through detailed material characterization as well as show the effect of device shrinkage on GO-based electronic devices (i.e., memristor). This provides new insight into and a great opportunity to tune/improve the GO electrical behavior (postfabrication) through a novel approach. The detailed material characterization results proved that enhanced GO characteristics can be achieved upon substrate shrinking. This is a milestone in the fabrication of efficient GO electronic devices on active substrates.

AUTHOR INFORMATION

Corresponding Author

Baker Mohammad – System on Chip Lab, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi, United Arab Emirates; Email: baker.mohammad@ku.ac.ae

Authors

- Heba N. Abunahla System on Chip Lab, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi, United Arab Emirates; © orcid.org/ 0000-0002-5357-2374
- Humaira Zafar Department of Physics, Khalifa University, Abu Dhabi, United Arab Emirates
- **Dalaver H. Anjum** Department of Physics, Khalifa University, Abu Dhabi, United Arab Emirates
- Anas Alazzam System on Chip Lab, Department of Mechanical Engineering, Khalifa University, Abu Dhabi, United Arab Emirates; ◎ orcid.org/0000-0002-8518-8027

Complete contact information is available at: https://pubs.acs.org/10.1021/acsomega.2c07306

Author Contributions

H.N.A. conceived the presented idea, performed device fabrication and electrical characterization, and wrote the manuscript. H.Z. and D.H.A. performed material characterization for the fabricated devices. A.A. and B.M. supervised the findings of this work. B.M. secured the fund. All authors discussed the results and contributed to the final manuscript.

Funding

This publication is based upon work supported by the Khalifa University of Science and Technology under Awards No. RC2-2018-020.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors are sincerely thankful to Nahla Al Amoodi for her assistance in using the shrinkable substrate used in this work. Also, the authors are thankful to Fadi Dawaymeh for his support in performing Raman spectroscopy.

REFERENCES

(1) Mohammad, B.; Abi Jaoude, M.; Kumar, V.; Al Homouz, D. M.; Nahla, H. A.; Al-Qutayri, M.; Christoforou, N. State of the art of metal oxide memristor devices. *Nanotechnol. Rev.* **2016**, *5*, 311–329.

(2) Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. The missing memristor found. *Nature* **2008**, *453*, 80–83.

(3) Abunahla, H.; Abi Jaoude, M.; O'Kelly, C. J.; Mohammad, B. Sol-gel/drop-coated micro-thick TiO2 memristors for γ -ray sensing. *Mater. Chem. Phys.* **2016**, 184, 72–81.

(4) Marani, R.; Gelao, G.; Perri, A. G. A review on memristor applications, 2015. arXiv:1506.06899. https://arxiv.org/abs/1506.06899.

(5) Sahu, D. P.; Jetty, P.; Jammalamadaka, S. N. Graphene oxide based synaptic memristor device for neuromorphic computing. *Nanotechnology* **2021**, *32*, No. 155701.

(6) Zhu, J.; Yang, D.; Yin, Z.; Yan, Q.; Zhang, H. Graphene and Graphene-Based Materials for Energy Storage Applications. *Small* **2014**, *10*, 3480–3498.

(7) Catania, F.; Oliveira, H. D. S.; Lugoda, P.; Cantarella, G.; Münzenrieder, N. Thin-film electronics on active substrates: review of materials, technologies and applications. *J. Phys. D: Appl. Phys.* **2022**, 55, No. 323002.

(8) Jeong, H. Y.; Kim, J. Y.; Kim, J. W.; Hwang, J. O.; Kim, J.-E.; Lee, J. Y.; Yoon, T. H.; Cho, B. J.; Kim, S. O.; Ruoff, R. S.; Choi, S. Y. Graphene oxide thin films for flexible nonvolatile memory applications. *Nano Lett.* **2010**, *10*, 4381–4386.

(9) Lin, C.-C.; Chen, Y.-D.; Lin, N.-C. In *Graphene Oxide Based Device for Flexible RRAM Application*, IEEE International Symposium on Next-Generation Electronics, 2013; pp 396–398.

(10) Liu, T.; Wu, W.; Liao, K.-N.; Sun, Q.; Gong, X.; Roy, V. A.; Yu, Z.-Z.; Li, R. K. Fabrication of carboxymethyl cellulose and graphene oxide bio-nanocomposites for flexible nonvolatile resistive switching memory devices. *Carbohydr. Polym.* **2019**, *214*, 213–220.

(11) Midya, A.; Gogurla, N.; Ray, S. K. Flexible and transparent resistive switching devices using Au nanoparticles decorated reduced graphene oxide in polyvinyl alcohol matrix. *Curr. Appl. Phys.* **2015**, *15*, 706–710.

(12) Yuan, F.; Ye, Y.-R.; Wang, J.-C.; Zhang, Z.; Pan, L.; Xu, J.; Lai, C.-S. In *Retention Behavior of Graphene Oxide Resistive Switching Memory on Flexible Substrate*, IEEE 5th International Nanoelectronics Conference (INEC), 2013; pp 288–290.

(13) Zhao, F.; Cheng, H.; Hu, Y.; Song, L.; Zhang, Z.; Jiang, L.; Qu, L. Functionalized graphitic carbon nitride for metal-free, flexible and rewritable nonvolatile memory device via direct laser-writing. *Sci. Rep.* **2014**, *4*, No. 5882.

(14) Abunahla, H.; Alamoodi, N.; Alazzam, A.; Mohammad, B. Micro-Pattern of Graphene Oxide Films Using Metal Bonding. *Micromachines* **2020**, *11*, 399.

(15) Jones, R. M. Thermal buckling of uniformly heated unidirectional and symmetric cross-ply laminated fiber-reinforced composite uniaxial in-plane restrained simply supported rectangular plates. *Composites, Part A* **2005**, *36*, 1355–1367.

(16) Cui, Y.; Wang, B.; Wang, P. Analysis of thermally induced delamination and buckling of thin-film thermoelectric generators made up of pn-junctions. *Int. J. Mech. Sci.* **2018**, *149*, 393–401.

(17) Vescovini, R.; Dozio, L. Thermal buckling behaviour of thin and thick variable-stiffness panels. J. Compos. Sci. 2018, 2, 58.

(18) Zhou, Z.; Xiu, F.; Jiang, T.; Xu, J.; Chen, J.; Liu, J.; Huang, W. Solution-processable zinc oxide nanorods and a reduced graphene oxide hybrid nanostructure for highly flexible and stable memristor. *J. Mater. Chem. C* **2019**, *7*, 10764–10768.

(19) Hong, S. K.; Kim, J. E.; Kim, S. O.; Choi, S.-Y.; Cho, B. J. Flexible resistive switching memory device based on graphene oxide. *IEEE Electron Device Lett.* **2010**, *31*, 1005–1007.