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High Performance All Nonmetal SiN_x Resistive Random Access Memory with Strong Process Dependence

Te Jui Yen[1], Albert Chin[1*] & Vladimir Gritsenko[2,3,4]

All-nonmetal resistive random access memory (RRAM) with a N^+–Si/SiN_x/P^+–Si structure was investigated in this study. The device performance of SiN_x developed using physical vapor deposition (PVD) was significantly better than that of a device fabricated using plasma-enhanced chemical vapor deposition (PECVD). The SiN_x RRAM device developed using PVD has a large resistance window that is larger than 10^4 and exhibits good endurance to 10^5 cycles under switching pulses of 1 μs and a retention time of 10^4 s at 85 °C. Moreover, the SiN_x RRAM device developed using PVD had tighter device-to-device distribution of set and reset voltages than those developed using PECVD. Such tight distribution is crucial to realise a large-size cross-point array and integrate with complementary metal-oxide-semiconductor technology to realise electronic neurons. The high performance of the SiN_x RRAM device developed using PVD is attributed to the abundant defects in the PVD dielectric that was supported by the analysed conduction mechanisms obtained from the measured current–voltage characteristics.

Resistive random access memory (RRAM)[1–26] has attracted considerable attention over the past two decades due to its simple structure, nonvolatility, high scalability, rapid switching speed, and relatively low operating power. These advantages make RRAM devices suitable for use in future artificial intelligence and neuromorphic computing applications[1–4]. A variety of binary composite materials, such as HfO_x, TaO_x, TiO_x, SiO_x, and GeO_x, that exhibit different device properties have been used as the switching layer. Although various conduction mechanisms for RRAMs have been proposed, the carrier transport behaviour of RRAMs still has not been completely confirmed. To prevent the metal ions from contributing to transport behaviour, we pioneered nonmetal GeO_x dielectric RRAM devices[6–10] and all-nonmetal N^+–Si/SiO_x/P^+–Si RRAM devices[11]. In this study, we investigated the all-nonmetal SiN_x RRAM devices in which the bond enthalpy of SiN is lower than that of SiO[27]. The SiN_x material has been widely used in the semiconductor industry for various applications, such as the passivation layer of an integrated circuit and the charge-trapping layer of a flash memory. This material can be easily integrated into complementary metal-oxide-semiconductor (CMOS) technology. Moreover, the RRAM device performance strongly depends on the SiN_x formation process. A high-performance RRAM device with a large memory window, good endurance, long retention time, and tight device-to-device distribution of the set–reset voltages V_{set}–V_{reset} is only achievable when the SiN_x layers are formed using low-temperature physical vapor deposition (PVD) rather than the standard plasma-enhanced chemical vapor deposition (PECVD). The high-performance SiN_x RRAM device developed using PVD (PVD-SiN_x RRAM device) is linked to the high number of defects and high amount of defect-related current conduction in the SiN_x dielectric.

Results

Figure 1(a) displays the forming process of the PVD-SiN_x RRAM device and the SiN_x RRAM device developed using PECVD (PECVD-SiN_x RRAM device). While the forming step of fabricating the PECVD-SiN_x RRAM device, the I_{cc} value was increased from 100 μA with a 100-μA step until the resistance state could be switched to the low-resistance state (LRS) at an I_{cc} value of 1 mA. The PVD-SiN_x RRAM device exhibited lower I_{cc} and lower forming voltage than those of the PECVD-SiN_x RRAM device. These results reflect that the initial PVD-SiN_x

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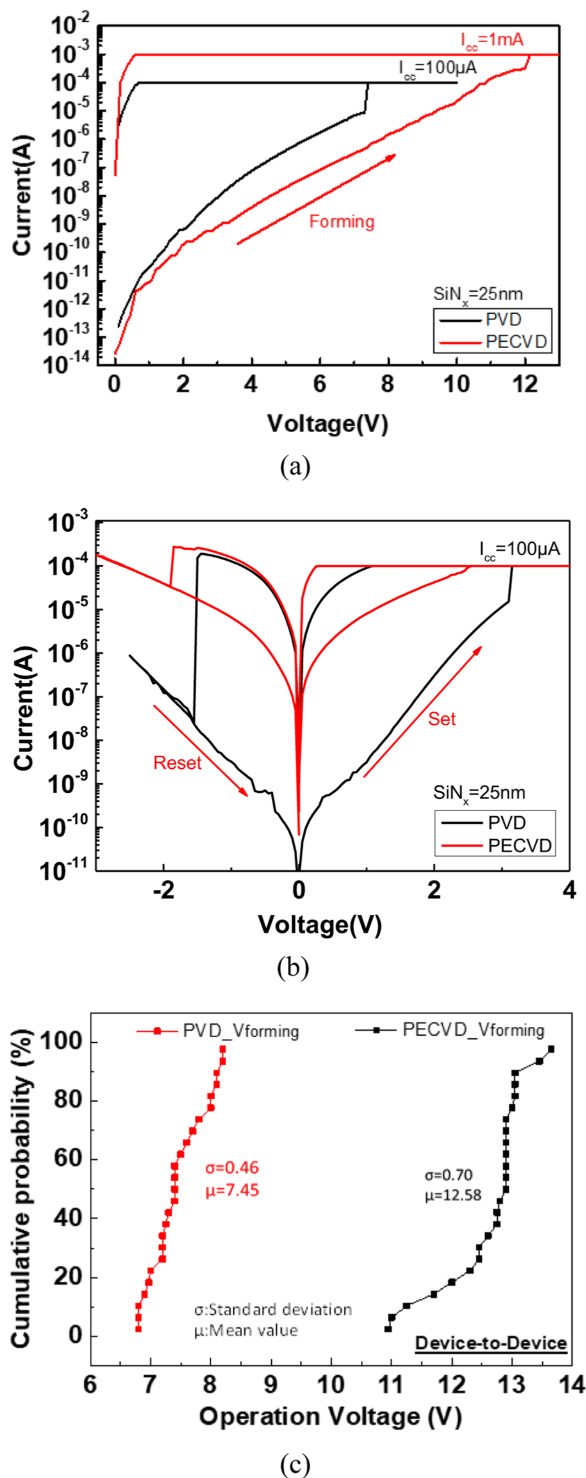


Figure 1. *I-V* characteristics of PVD and PECVD SiN_x RRAM devices of (**a**) forming process, (**b**) set-reset processes, and (**c**) forming voltage distributions.

RRAM device has more defects to form a conduction path than the PECVD-SiN_x RRAM device. Figure 1(b) depicts the typical bipolar switching characteristics of both PVD-SiN_x and PECVD-SiN_x RRAM devices. The PVD-SiN_x RRAM device exhibits a significantly lower high-resistance state (HRS) current and a larger resistance window than those of the PECVD-SiN_x RRAM device. The much higher HRS current in the PECVD-SiN_x RRAM device may be related to the higher I_{cc} and bias voltage values needed during the forming process, where such high power may damage the SiN_x and create unrecoverable defects. The asymmetric LRS *I-V* curve of the PECVD device may be due to the large forming voltage and power to generate excessive defects, which may be partially annihilated by injected electrons during negative voltage swept. Figure 1(c) shows the forming voltage

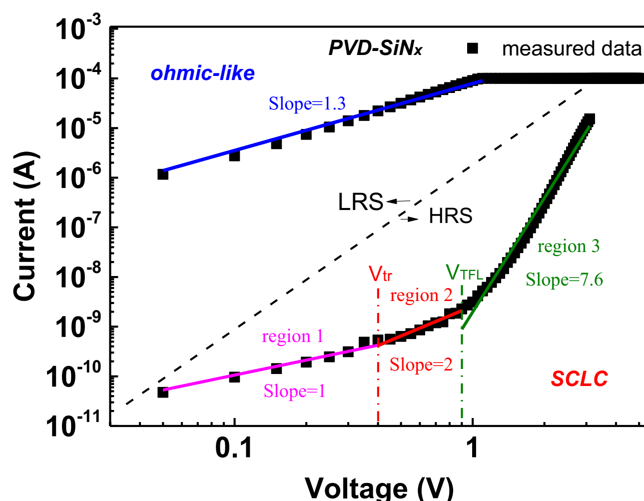


Figure 2. *I-V* characteristics of PVD-SiN_x RRAM device were analyzed by the space-charge limited conduction (SCLC) in HRS and ohmic-like behavior conduction in LRS.

distributions of PVD-SiN_x and PECVD-SiN_x devices, which are ranged from 6.8 to 8.2 V and from 11.0 to 13.7 V, respectively.

To further understand the carrier conduction mechanism, we analysed the measured data by using various transport mechanisms. Because there is no metal inside the dielectric to form the metallic filament, the conduction mechanism of nonmetal RRAM device is attributed to defect-related hopping conduction[10,12,13]. Figures 2 and 3 display the analysed conduction mechanisms for PVD-SiN_x and PECVD-SiN_x RRAM devices, respectively. The very low HRS current in the PVD-SiN_x RRAM devices, as presented in Fig. 2, is attributed to the space-charge limited conduction (SCLC) mechanism[14–16,28]. The SCLC regions are divided into three regions by using the transition voltage V_{tr} and trap-filled limited voltage V_{TFL}. For the low-bias voltage region that is less than V_{tr}, the current is proportional to voltage and follows Ohm's law, with an extremely high resistance of approximately 10 GΩ. The current density–voltage (*J–V*) relationship obtained when the applied voltage is larger than V_{tr} but lower than V_{TFL} (region 2) can be expressed as follows[17,29]:

$$J = \frac{9\mu\varepsilon\theta}{8d^3}V^2,\ \theta = \frac{J_{free}}{J_{trap} + J_{free}}, \tag{1}$$

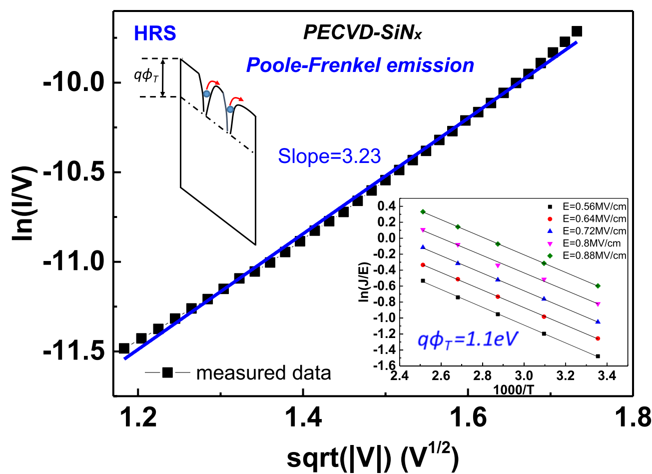
where J, μ, ε, d, and θ represent the current density, electron mobility, static dielectric constant, dielectric layer thickness, and ratio of the free current density to the trapped and free current densities, respectively. In this region, shallow traps are gradually filled by increasing the electric field, and the injected free carrier current density J_{free} significantly contributes to the total current density. All the traps at voltages larger than V_{TFL} are filled by injected carriers. A massive number of free carriers contribute to current conduction under a high electric field, thus leading to a steep current–voltage (*I–V*) slope (region 3) For the PVD device, the currents of HRS *I-V* curves increase with increasing temperature[18]. Conversely, the LRS, which exhibited ohmic-like behavior, can be analysed with a slope of 1.3[9,13].

For the HRS current of the PECVD-SiN_x devices presented in Fig. 3(a), the current conduction resembles Poole–Frenkel (P–F) emission[19,20,29–32]:

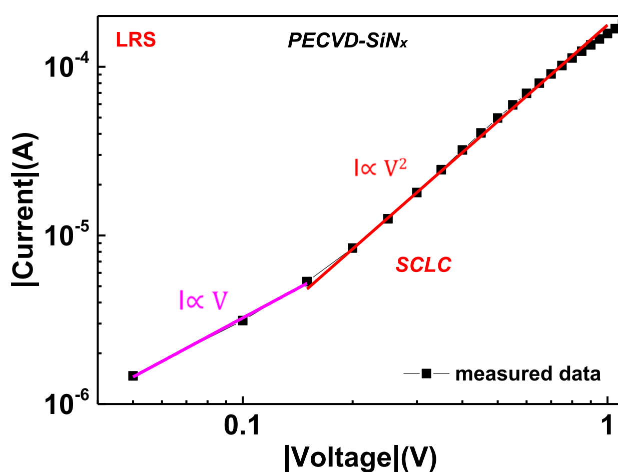
$$J = q\mu N_c E \exp\left[\frac{-q(\phi_T - \sqrt{qE/\pi\varepsilon_i\varepsilon_0})}{kT}\right], \tag{2}$$

where J, μ, N_c, $q\phi_T$, E, ε_i, ε_0, k, and T are the current density, electron drift mobility, density state in the conduction band, energy level of trap, electric field, dynamic permittivity, vacuum permittivity, Boltzmann's constant, and absolute temperature, respectively. A trap energy $q\phi_T$ of 1.1 eV was determined according to the Arrhenius plots presented in Fig. 3(a) at a temperature range from 298 to 398 K. An ε_i value of 4.3 was obtained from the slope of P–F plots and is lower than the static permittivity ($\varepsilon = 7$)[33]. P–F emission occurs due to electrons hopping between nearby traps[34] which leads to a high HRS current, as shown in Fig. 1(b). Figure 3(b) displays the LRS *I–V* characteristics of the PECVD-SiN_x device that adheres to the SCLC under the most-negative voltage bias region.

Figure 4 illustrates the potential switching behaviours of the SiN_x RRAM device. The PVD-SiN_x dielectric has abundant defects in the initial condition because of its room temperature deposition with a low annealing temperature of 200 °C. The current conducting path can be formed and switched to LRS with a relatively low I_{cc} value and voltage. By contrast, the PECVD-SiN_x dielectric was deposited at a relatively high temperature of 300 °C, with fewer defects, so the conducting path could not be formed under low I_{cc} and voltage values. Therefore, a high forming voltage of 12 V and a high I_{cc} of 1 mA were required. Under such a high electric field, a large number of Si–N bonds were broken and excessive defects were created. The excessive defects in the PECVD-SiN_x layer



(a)



(b)

Figure 3. *I-V* curves of PECVD-SiN_x RRAM were analyzed with (**a**) Poole-Frenkel (P-F) emission in HRS and (**b**) space charge limited conduction in LRS. The inset figure in (**a**) is Arrhenius plot of the PF emission.

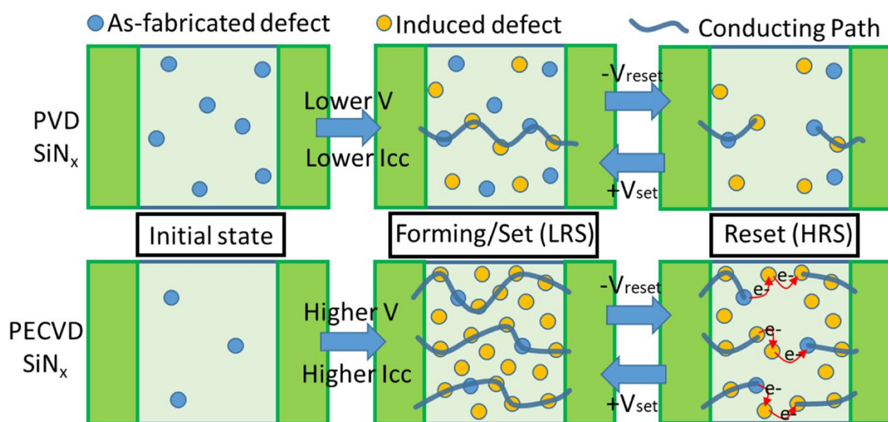


Figure 4. Schematic diagram of potential resistance switching in SiN_x RRAM.

may create multiple conduction paths and lead to a high HRS current, as shown in Fig. 1(b). To switch from LRS back to HRS, a negative V_{reset} was applied to rupture the conducting path. Although the conducting paths were ruptured, the electrons in the PECVD-SiN_x layer had a high possibility to conduct current in parallel ways via

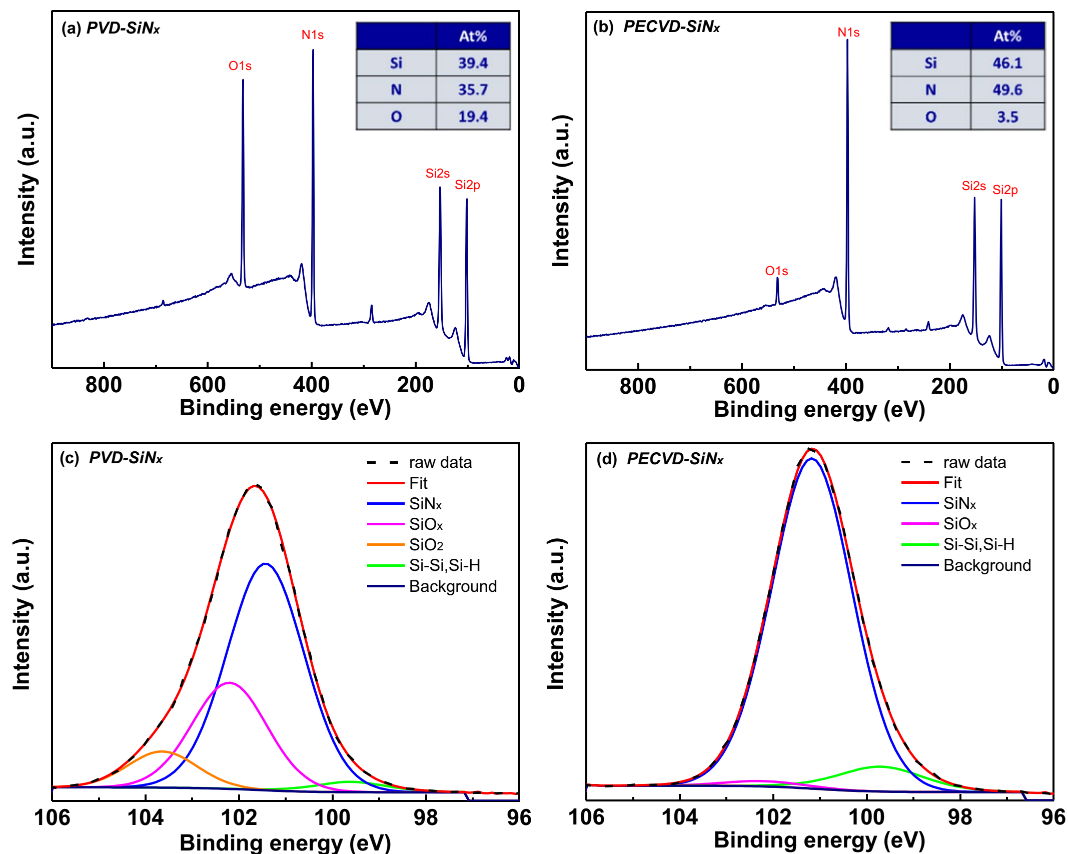


Figure 5. XPS data of (**a**) PVD-SiN_x (**b**) PECVD-SiN_x layers, and the related Si 2p spectrum of (**c**) PVD-SiN_x film (**d**) PECVD-SiN_x layers.

hopping through nearby defects. This further led to the high measured HRS current. Conducting paths can be formed again for electron transportation when a positive V_{set} is applied to the top electrode.

The deposited SiN_x layers were further analysed using X-ray photoelectron spectroscopy (XPS). Figure 5(a,b) depict the XPS data for PVD-SiN_x and PECVD-SiN_x layers, respectively. The related Si 2p spectra obtained from the XPS data are displayed in Fig. 5(c,d) for the PVD-SiN_x and PECVD-SiN_x layers, respectively. The N–Si composition of the as-fabricated PVD-SiN_x and PECVD-SiN_x layers were 0.91 and 1.08, respectively, which indicates a high number of defects inside the PVD-SiN_x layer. The nitride vacancies[21,35] and Si dangling bonds[22,23] can play crucial roles to form the conducting path. The slightly higher oxygen content in the PVD-SiN_x layer than in the PECVD-SiN_x layer cannot explain the significantly better device performance because the bond enthalpy of SO is higher than that of SN. That is, it is more difficult to break the SO bond to form the defects. Therefore, the XPS results support the proposed model depicted in Fig. 4 and adequately explain the measured *I*–*V* characteristics in Fig. 1 and the analysed current conduction mechanisms in Figs. 2 and 3. Such defect-assisted conduction is also the major mechanism for similar GeO_x RRAM devices[10]. The conducting path can be constructed or broken by the different polarities of the applied voltage.

Device endurance and data retention are the crucial characteristics of a nonvolatile memory. Figure 6 shows the retention data of PVD-SiN_x and PECVD-SiN_x RRAM devices under an 85 °C test condition. The PECVD-SiN_x device exhibits a much smaller resistance window and a rapid degradation from an initial value of 56 to 11 after 10^4 s retention at 85 °C. The poor retention can be ascribed to the high forming voltage with large kinetic energy; then the electrons at 85 °C can partially annihilate or create a leakage path with multiple defects, as shown in Fig. 4. By contrast, the resistance window of an all-nonmetal PVD-SiN_x RRAM device slightly decreases from 1.8×10^3 to 1.3×10^3 after a retention time of 10^4 s at 85 °C. The RRAM device endurance data are shown in Fig. 7, where the V_{set} and V_{reset} pulses of +5 V and −5 V were applied to devices with a 1-µs pulse width. The resistance window of the PECVD-SiN_x device degraded quickly, and the device failed after 10^3 endurance cycles. Conversely, a large resistance window of two orders of magnitude was obtained for the PVD-SiN_x RRAM device, even after 10^5 pulse cycles. The excellent endurance of the PVD-SiN_x device is related to the high number of defects that can be set and reset easily, with less destruction to the dielectric material.

Figure 8(a,b) display the device-to-device and cycle-to-cycle distributions of V_{set} and V_{reset} respectively, which are critical for the RRAM cross-point array[24–26]. The coefficient of variation (CV) was used to study the distribution and is defined as follows:

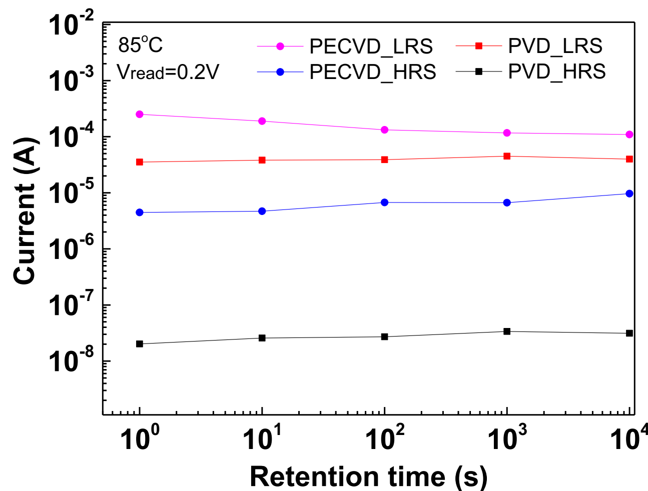


Figure 6. Retention test of N^+-Si/PVD-SiN_x/P^+-Si and N^+-Si/PECVD-SiN_x/P^+-Si RRAM devices under 85 °C.

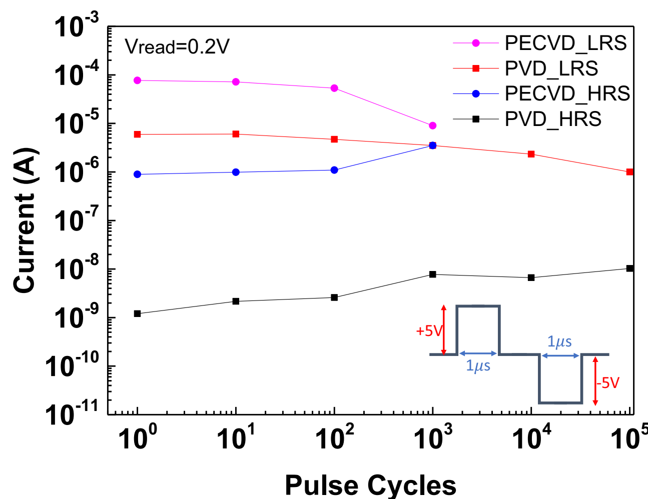


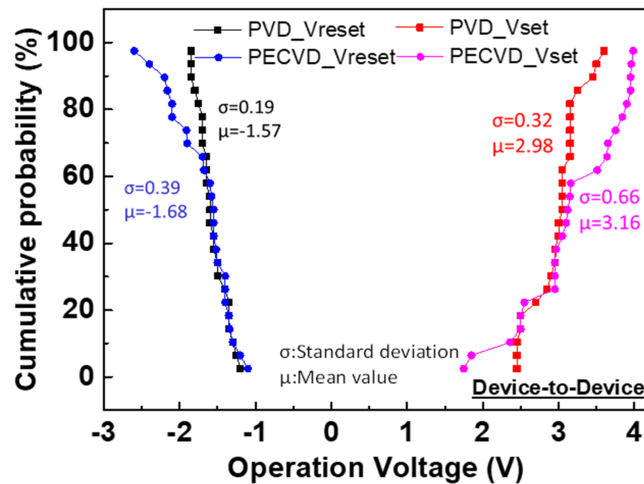
Figure 7. Endurance characteristics of N^+-Si/SiN_x/P^+-Si RRAM devices.

$$\mathrm{CV} = \frac{\sigma}{|\mu|} \times 100\%, \tag{3}$$

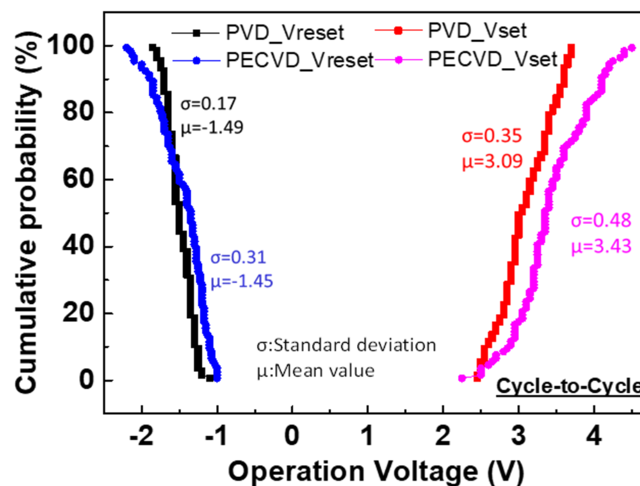
where σ is the standard deviation, and μ is the mean value. The lower CV value represents a tighter distribution and is crucial for a larger array size[26]. The device-to-device distributions were extracted from 25 different devices. The CVs of V_{set} and V_{reset} of the PVD-SiN_x RRAM were 10.7% and 12.1%, respectively, which are remarkably tighter than the 18.3% and 23.2% of PECVD-SiN_x devices, respectively. The cycle-to-cycle variations of the first 100 consecutive DC switching cycles, depicted in Fig. 8(b), also show the crucially tighter operation voltage distributions of PVD-SiN_x RRAM devices than those of PECVD-SiN_x ones. During the forming step, the dielectric soft breakdown must occur by breaking part of the SiN bonds. Based on the preceding discussion, the PECVD-SiN_x RRAM device requires a higher I_{cc} value and voltage during fabrication to create a conducting path that has an excessive number of defects and an uncontrollable reset current. These results further lead to poor V_{set} and V_{reset} distribution and fewer endurance cycles. One issue of nonmetal RRAM device is the relatively larger operation voltage than that of metal-oxide RRAM device, even though the operation voltage is still much less than that of a flash memory[36]. One possibility to lower the operation voltage is to use the weak bond-enthalpy GeO_x dielectric[9], in which the defect-related conduction path can be formed by breaking the dielectric at low energy.

Conclusion

High-performance all-nonmetal N^+–Si/SiN_x/P^+–Si RRAM devices were achieved. The device performance was highly dependent on the deposition process. In this process, the current conduction in the RRAM device was highly related to the defects inside the SiN_x layer. The PVD-SiN_x RRAM devices exhibited favourable memory characteristics: a large memory window, high pulsed endurance, a long data retention time at 85 °C, and tight



(a)



(b)

Figure 8. Operation voltage distributions of SiN_x RRAM devices for (**a**) device to device and (**b**) cycle-to-cycle.

device-to-device V_{set} and V_{reset} distributions. The PVD-SiN_x RRAM device has high potential to realise a large-size cross-point memory array and to be embedded in CMOS technology to realise electronic neurons.

Methods

A P^+ silicon wafer was used as a bottom gate. After conducting the RCA clean for the wafer and dipping the wafer into dilute HF to remove the native oxide, a 25-nm-thick SiN_x layer was formed by either PVD using electron-beam evaporation or PECVD. Additional furnace annealing was applied to the PVD-SiN_x layer at 200 °C in a N_2 ambient for 30 min. For the PECVD-SiN_x layer, a NH_3 of 6 sccm, 8% SiH_4 in Ar of 125 sccm, and N_2 of 200 sccm were used at a temperature of 300 °C. Finally, the N^+–Si top electrode was fabricated as the top electrode with a diameter of 120 μm[11]. The electrical characteristics were measured using the HP4155B analyser. The pulse stress was generated using a pulse generator (81110, Agilent). Material analysis was performed through XPS analysis by using Thermo Scientific K-Alpha with an X-ray spot size of 400 μm.

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Author contributions

T.J. Yen did the experiments; Albert Chin is the principle investigator (PI) to monitor the project; Vladimir Gritsenko is the co-PI for this work. All authors reviewed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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The results of this research have important contributions for RRAM device.

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