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Author Correction: Carrier control in 2D transition metal dichalcogenides with Al_2O_3 dielectric

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Correction to: *Scientific Reports* https://doi.org/10.1038/s41598-019-45392-9, published online 19 June 2019

The original version of this Article contained an error in Figure 3b, where the y-axis

"/(nA)"

now reads:

"/(μA)"

The original Figure 3 and accompanying legend appear below. The original Article has been corrected.

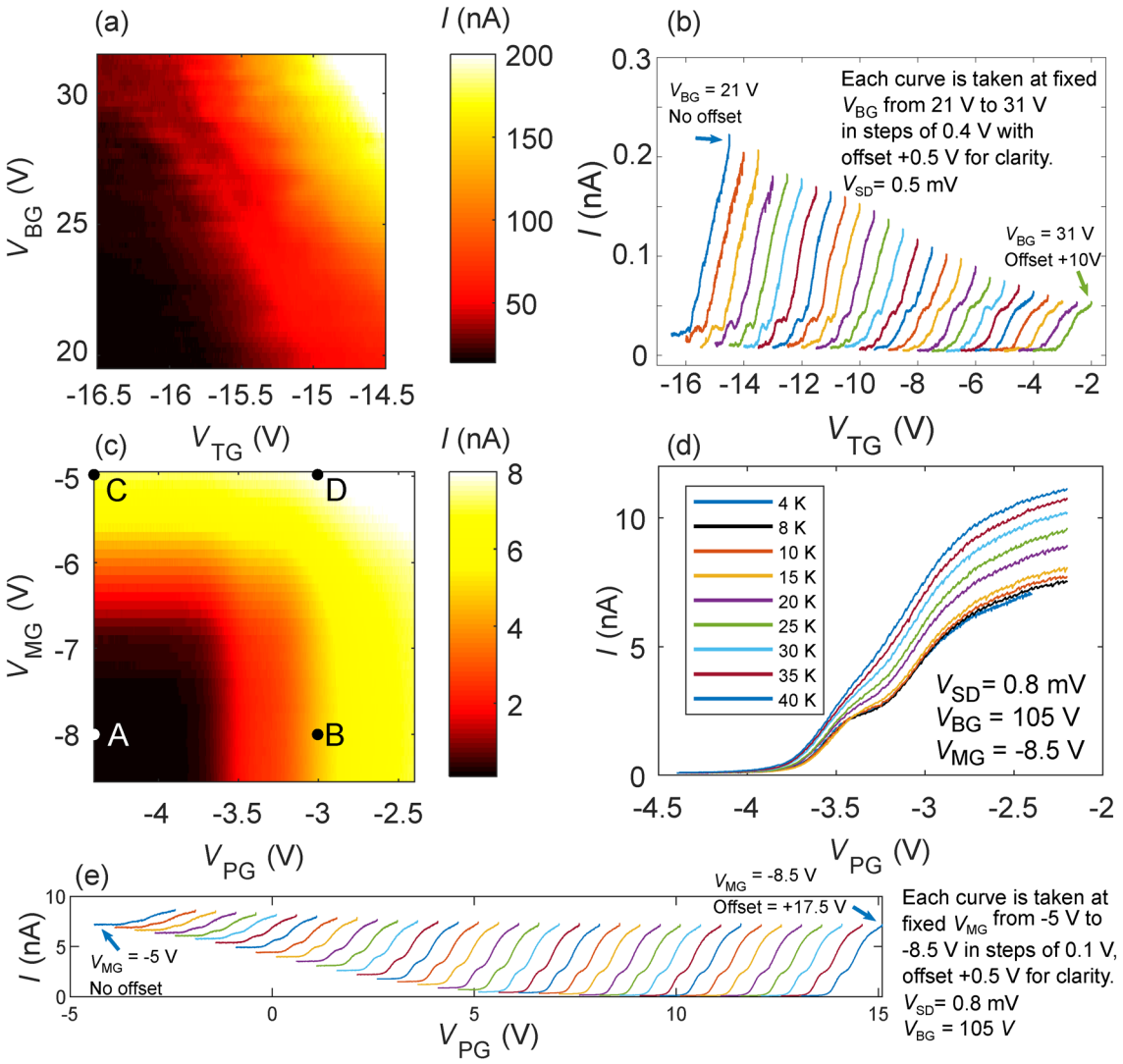

Figure 3. Top gate control. (**a**) Current I vs top gate voltage V_{TG} and back gate voltage V_{BG} for MoS_2 D1. The current can be smoothly tuned by both V_{TG} and V_{BG}. The dark lower left region highlights the voltage space when the conducting channel of the device is pinched off. (**b**) I vs V_{TG} at various applied V_{BG}, where current steps can be observed, suggesting the formation of a quantum constriction. (**c**) Current I vs top gate voltages V_{MG} and V_{PG} at $V_{BG} = 105$ V for WSe_2 D2 (see Fig. 1c inset). The current through the device can be independently controlled by the split top gates PG and MG. (**d**) Current I vs V_{PG} at fixed V_{BG} and V_{MG} taken at different temperatures. The current steps are visible up to 25 K. (**e**) I vs V_{PG} at various applied V_{MG} and fixed $V_{BG} = 105$ V, where similar current steps are observed.