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High Pressure Deuterium Passivation of Charge Trapping Layer for Nonvolatile Memory Applications

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Abstract: In this study, the deuterium passivation effect of silicon nitride (Si_3N_4) on data retention characteristics is investigated in a Metal-Nitride-Oxide-Silicon (MNOS) memory device. To focus on trap passivation in Si_3N_4 as a charge trapping layer, deuterium (D_2) high pressure annealing (HPA) was applied after Si_3N_4 deposition. Flat band voltage shifts (ΔV_{FB}) in data retention mode were compared by CV measurement after D_2 HPA, which shows that the memory window decreases but charge loss in retention mode after program is suppressed. Trap energy distribution based on thermal activated retention model is extracted to compare the trap density of Si_3N_4 . D_2 HPA reduces the amount of trap densities in the band gap range of 1.06–1.18 eV. SIMS profiles are used to analyze the D_2 profile in Si_3N_4 . The results show that deuterium diffuses into the Si_3N_4 and exists up to the Si_3N_4 - SiO_2 interface region during post-annealing process, which seems to lower the trap density and improve the memory reliability.

Keywords: deuterium high pressure anneal; flash memory; silicon nitride; retention



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1. Introduction

Although research on ReRAM, MRAM, PCM etc. is being actively conducted for next-generation nonvolatile memories [1,2], the demands for Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) flash memory are still dominant. SONOS memory can obtain large capacity easily and have a simple circuit structure. Due to these advantages, the memory has been continuously developed since its invention, improving its storage capacity and reliability [3]. In SONOS, to optimize the silicon nitride (Si_3N_4) film which is used as charge trapping layer (CTL) of the device is very important for the performance enhancement. Substantial research has been carried out to improve the Si_3N_4 by varying Si/N ratio during deposition, post-annealing condition, or imbedding nano particles [4–8].

Several works on deuterium (D_2) passivation of Si_3N_4 with high pressure annealing (HPA) has been also reported. In the conventional CMOS transistors, D_2 HPA has been used for the hot carrier reliability [9–11]. HPA is known to enhance the deuterium incorporation at the Si/ SiO_2 interface, and the deuterium-passivated silicon materials and interfaces are more electrically stable and reliable. In the case of the memory device, Tanaka's group at Toshiba Corporation has reported that the MONOS devices with the memory window increment and improve reliability by applying D_2 treatment in 2002 [12]. With variations in the pressure of D_2 , they show that D_2 annealing can be used to terminate the traps. In 2004–2005, S.M. Choi's group checked the high temperature (900 °C) D_2 annealing effect on the memory device [13,14], and it showed excellent program/erase endurance and a significantly reduced charge loss rate. They focused on D_2 annealing to passivate the interface traps between the tunneling oxide and Si substrate. The decreased interface trap was confirmed by the quasi-static capacitance measurement. In 2016, L. Breuil's group investigated D_2 effect on poly-Si channel with trap passivation at the interface between the ONO layer and the poly-Si channel and in the bulk poly-Si [15]. The D_2 high pressure

annealing has been conducted at the last step of the fabrication process. The results show drive current (I_{ON}), subthreshold swing (SS) improvement after D_2 annealing, which points to a reduction of the defects at the channel and Si-SiO₂ interface. Threshold voltage (V_{TH}) is also reduced due to the passivation of negative fixed charges in the ONO stack. However, in this study, retention characteristics seem not to be affected. In 2020, J.M. Yu's group at Korea Advanced Institute of Science and Technology investigated the high-pressure D_2 annealing effects on Gate-All-Around SONOS memory [16]. Maximum transconductance ($g_{m,max}$), SS, and I_{ON} were extracted, which were improved after D_2 annealing. The low-frequency noise (LFN) measurement was used to extract the oxide trap density (D_{OT}) and it was found that the tunneling oxide-channel interface trap decreases by the trap passivation effect of deuterium annealing.

In this study, D_2 high pressure annealing (HPA) at low temperature is suggested to suppress the shallow trap formation of Si₃N₄. Unlike previous research where D_2 annealing is applied after the metallization and the analyses are concentrated on the oxide-channel interface traps, the suggested process is applied before the metal deposition and the passivation effect of the traps in silicon nitride is focused on.

During Si₃N₄ deposition, stoichiometric Si₃N₄ is formed and nonstoichiometric bonding would be created. In nonstoichiometric bonding, there may be silicon vacancies and nitrogen vacancies, and some studies found out that the Si-O-N bond caused by oxygen diffusion to nitrogen vacancy makes shallow traps [17,18]. The oxygen ions can migrate from the tunneling oxide. The suggested D_2 passivation is intended to cure the nitrogen vacancies and suppress the trap generation (similar to the oxygen complex bond). If the deuterium ion occupies the vacancy site, Si-O-N bond cannot be formed even though the oxygen ion migrates. Compared with H₂ passivation, D_2 passivation can cure defects more stably because deuterium forms stronger bond than hydrogen [19]. Via passivate shallow traps with D_2 , the memory window can be decreased, but the retention characteristic is expected to improve.

The fabricated devices are programmed and then flat band voltage (V_{FB}) is extracted in retention mode at a high temperature via CV measurement. Based on the experimental results, trap energy distribution of Si₃N₄ is extracted based on the thermal activated retention model. To find out D_2 profile and bonding formation in Si₃N₄, secondary ion mass spectroscopy (SIMS) and Fourier transform infrared spectroscopy (FT-IR) are analyzed. FT-IR spectroscopy is often used to see atomic bonding in materials [20,21] where each atomic bonding absorbs specific wavelength of light. Furthermore, the greatest benefit of FT-IR is its high sensitivity in order to inspect light atoms such as hydrogen and deuterium.

2. Experiments

A metal-nitride-oxide-silicon structure capacitor was fabricated and Figure 1 shows the process flows. Contrary to the SONOS structure, the blocking oxide is skipped to remove the process effect by blocking oxide deposition, which is also preferable for the direct correlation of electrical characteristics with SIMS profile whose sample is nitride/oxide/Si substrate. With p-type silicon substrate, SiO₂ for tunneling oxide was grown to 7 nm via dry oxidation. Then, the Si₃N₄ for CTL was deposited via plasma enhanced chemical vapor deposition (PECVD) with a thickness of 15 nm. Next, D_2 high pressure annealing was performed on some samples. D_2 6%/N₂ 94% forming gas was used and high-pressure annealing condition was 450 °C, 10 atm. Afterward, post-annealing was done in 600 °C in N₂ ambient. Ti 100 nm was deposited via RF sputter for use as a top and bottom gate. Table 1 shows the experimental conditions. The as-deposited sample functions as a reference, and the D_2 HPA sample and D_2 HPA + post-anneal sample are for testing the temperature effect in D_2 treatment. For the electrical analysis, CV was measured using a Hewlett Packard 4284A precision LCR meter. Programming was completed via same program voltage using Hewlett Packard 41501A pulse generator. The thermal activated retention model is used to extract the trap energy distribution of Si₃N₄ based on the measurement. Physical analyses were also used to support the experiment results. D_2 is well

known for possessing a heavier ion than H_2 , but they both are still very light ions compared with other atoms. Thus, there are not many methods to detect D_2 in the silicon nitride layer. In this study, SIMS and FT-IR were used to find out D_2 profile and bonding formation in the silicon nitride after the annealing process.

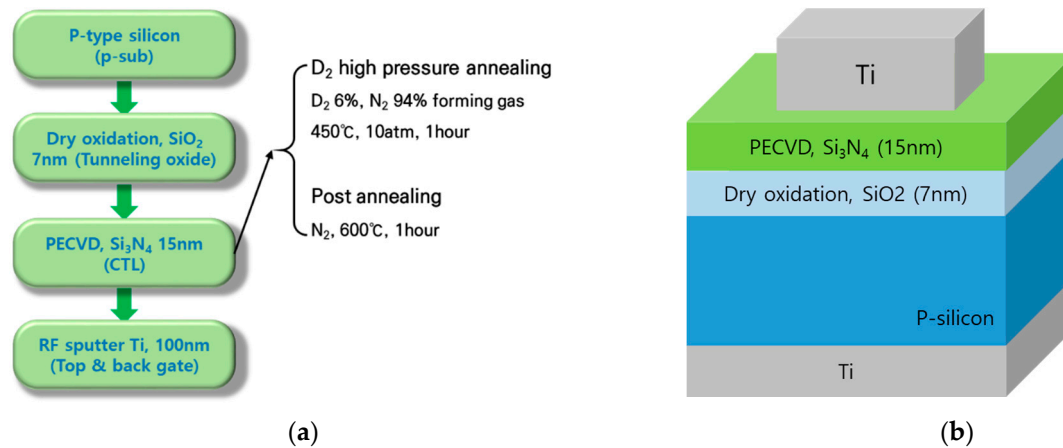


Figure 1. (a) Fabrication process and (b) the cross view of the capacitor-type device with metal nitride oxide silicon (MNOS) structure.

Table 1. Experimental conditions of the post treatment on the silicon nitride, which is performed before the metal deposition.

	As-Deposited	D ₂ HPA	D ₂ HPA + Post Anneal
D ₂ , 450 °C, 10 atm	×	O	O
N ₂ , 600 °C	×	×	O

3. Results and Discussion

3.1. Electrical Analysis

3.1.1. Memory Window

Figure 2a shows the I-V measurement results of the fabricated devices and shows similar breakdown properties of NO stack independent of annealing conditions. Figure 2b is the CV measurement results at the initial and program state. The maximum capacitance is determined by the nitride/oxide thickness and the values are observed to be similar in all samples, which indicates that the NO thickness is not changed by the annealing condition. The programming pulse width was 0.1 s, and the magnitude was 20 V for one pulse time. Sweep mode with long integration time was used in 1 MHz frequency. Compared with the reference, the device with D₂ HPA shows a decreased memory window and this effect was accelerated in one experiment with additional post-annealing. This seems to be the result of trap curing in Si₃N₄ bulk and interface [22].

3.1.2. Retention Characteristics

Retention properties are measured at various temperatures. The flat band voltage (V_{FB}) decrement was measured with CV measurement in retention mode after programming. The retention characteristic was quantified with the percentage of $V_{FB} \downarrow$ decrease by $V_{FB} \downarrow_{\text{program-initial}}$. As shown in Figure 3a, compared with the reference (which shows a 27.53% V_{FB} decrement), the device subjected to D₂ HPA exhibits slight improvement, with a 21.37% decrement. Then, additional post-anneal activity makes a significant difference in V_{FB} decrease during retention mode. Figure 3b is a comparison result of charge loss amount at various temperatures, which shows that D₂ passivation effects become clearer at higher temperatures. The extracted values are summarized in Table 2.

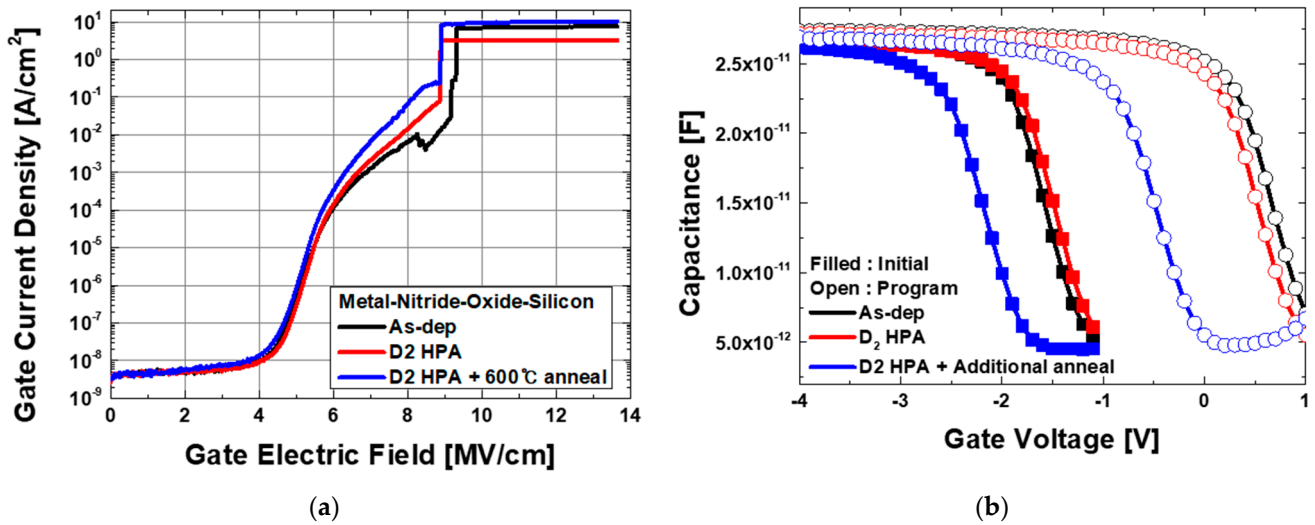


Figure 2. (a) The I-V measurement results of the fabricated devices and (b) the CV measurement results at the initial and programmed state. Here, as-dep is a reference device, and D₂ HPA is D₂ high pressure annealed device at 450 °C and D₂ HPA + Post-anneal is D₂ high pressure annealed device with post-anneal at 600 °C.

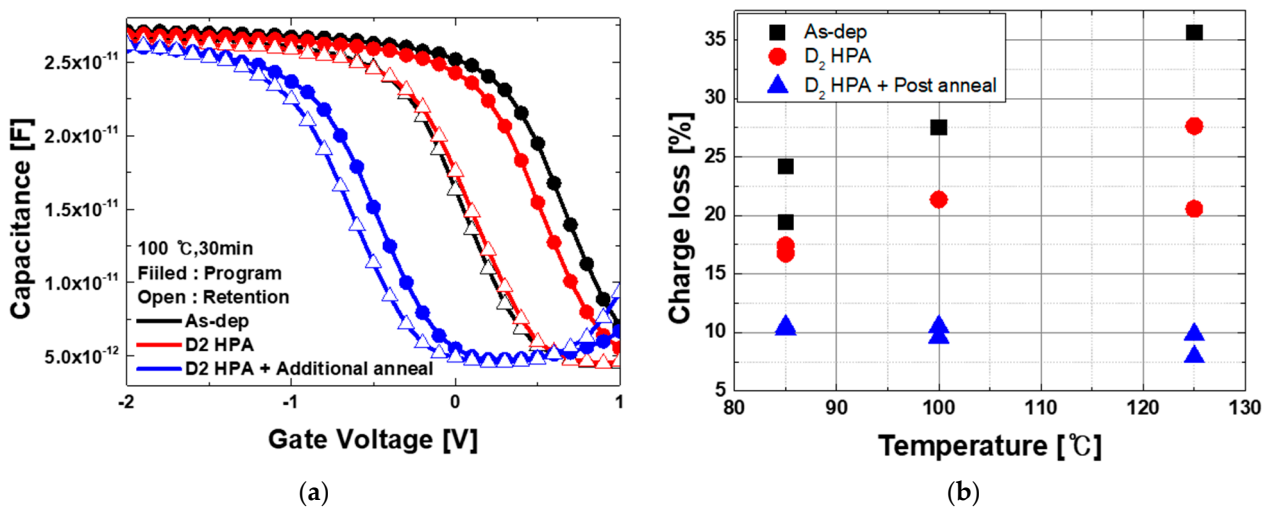


Figure 3. CV measurement results in data retention mode at 30 min after programming. (a) CV shift at 100 °C retention mode; (b) extraction results of charge loss amount (percent) in retention mode at various temperature. Here, charge loss was calculated by the amount of V_{FB} shift after retention time divided by the memory window.

Table 2. Charge loss percent of each device in retention mode after programming at various temperature.

	Charge Loss (%) = $\frac{V_{FB program} - V_{FB retention}}{V_{FB program} - V_{FB initial}} \times 100$		
Temperature	85 °C	100 °C	125 °C
As-dep	19.43	27.53	35.65
D ₂ HPA	16.75	21.37	27.65
D ₂ HPA + Post-anneal	10.30	10.52	9.84

3.1.3. Trap Energy Level Distribution

Trap energy level of CTL can be extracted by measuring the charge loss through the tunneling oxide. In this experiment, it is assumed that most of the shallow traps are located at or near the interface between Si₃N₄ and SiO₂ tunneling oxide and the amount of charge

loss through the metal gate can be ignored. To extract the trap density in Si₃N₄, thermal activated retention model is used like follows [23].

$$\frac{\partial \Delta V_{TH}}{\partial \log(t)} = -2.3k_B T X_N \left(\frac{X_N}{2\epsilon_N} + \frac{X_{OX}}{\epsilon_{OX}} \right) g(E_{TA}) \quad (1)$$

$$E_{TA} = k_B T \ln(AT^2 t) \quad (2)$$

$$A = 2\sigma_n \sqrt{\frac{3k_B}{m^*}} \left[\frac{2\pi m^* k_B}{h^2} \right]^{3/2} \quad (3)$$

Equation (1) shows the charge decay model in relation to V_{TH} shift according to time at specific temperature. E_{TA} is the energy level expressed like Equation (2). In Equation (3), σ_n is the capture cross-section and m* is the effective mass of electron in the silicon nitride. Measurements were conducted at 85 °C.

Figure 4a shows the extracted energy distribution of trap in each process condition based on the experimental results of charge loss according to the retention time as shown in Figure 4b. The results show that D₂ passivation reduces the amount of trap densities in the band gap range of 1.06 eV~1.18 eV, and this suppression seems to be reinforced with post-annealing. This result explains the program window reduction in D₂ HPA, as mentioned before.

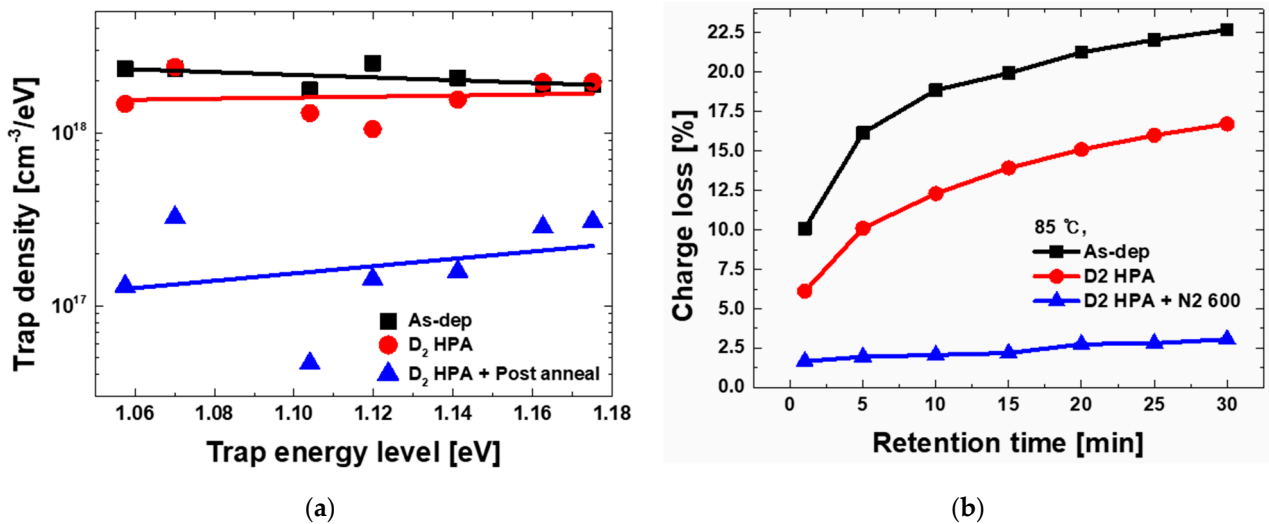


Figure 4. (a) Trap energy level distribution is Si₃N₄ according to the post treatment. (b) Measurement results of charge loss according to the retention time at 85 °C. The extraction is based on thermal activated retention model.

3.2. Physical Analysis

3.2.1. Secondary Ion Mass Spectroscopy

SIMS can be used to find out the D₂ profile in Si₃N₄ [24,25]. The selected elements Si, O, N, D, and depth profiles were obtained with a commercial SIMS instrument (CAMECA IMS 7f). The primary ions were 6 keV Cs⁺ at 10 nA and raster into a 250 μm × 250 μm with a detected area of 63 μm in diameter. Figure 5 shows the SIMS profile results for as-deposited silicon nitride and D₂ passivated Si₃N₄, including the post-anneal process. As-deposited Si₃N₄ has a negligible quantity of deuterium, but in the sample treated with D₂ high pressure annealing, it can be seen that deuterium exists from the surface side. Furthermore, with additional post-annealing, it was confirmed that deuterium diffuses into the Si₃N₄ and exists up to the Si₃N₄-SiO₂ tunneling oxide interface region. It is possible that deuterium can be dissociated during the post-annealing period, but the SIMS results indicate that deuterium affects silicon nitride property during N₂ 600 °C anneal. That is, even if some injected deuterium could dissociate and diffuse out to air at 600 °C, some could diffuse

into the layer and form bondage with Si and N atoms. Furthermore, previous research had conducted D₂ high pressure annealing even at 900 °C [12]. This result supports our theory as why V_{FB} in the initial state is shifted to the left and the memory window decreases.

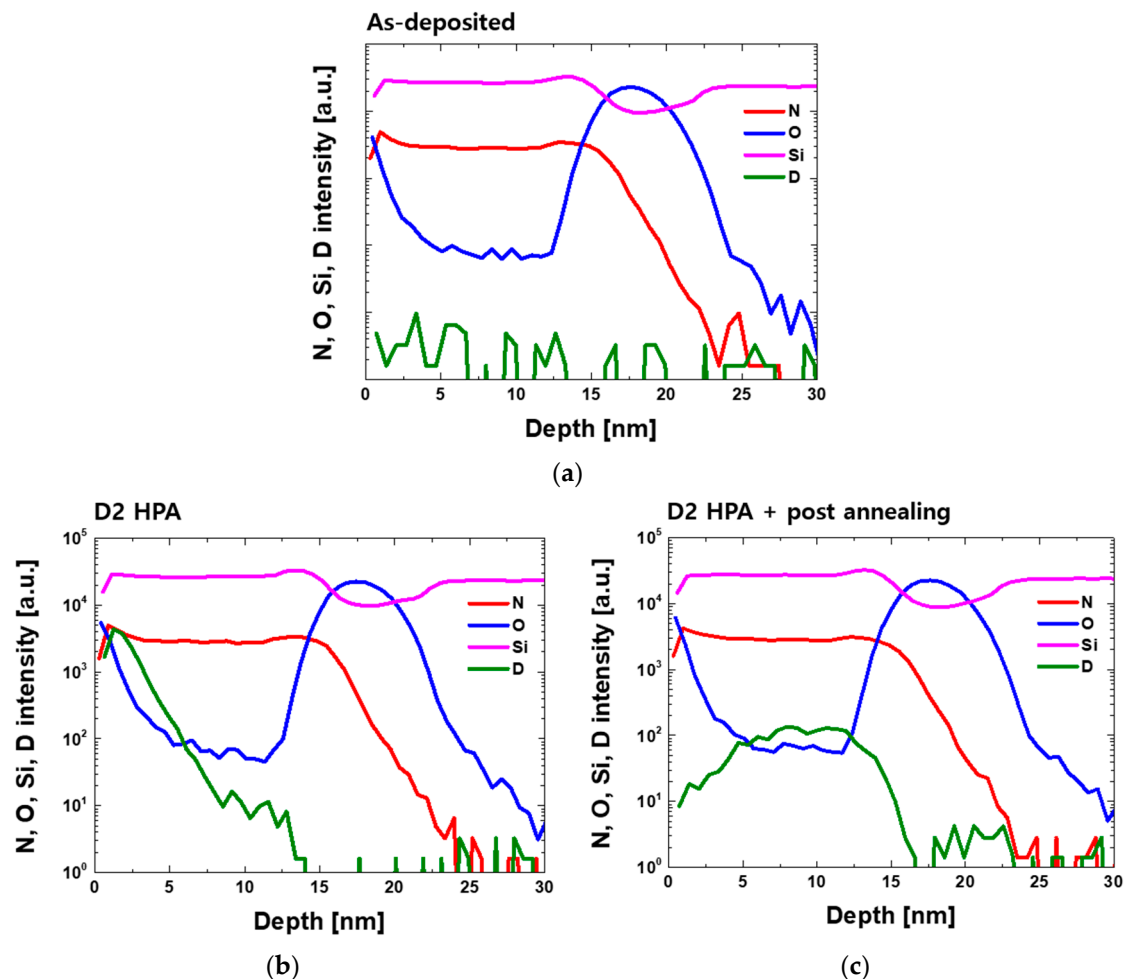


Figure 5. SIMS profile of N, O, Si, D in (a) as-deposited silicon nitride; (b) D₂ high pressure annealed silicon nitride; (c) D₂ high pressure anneal with post-annealing silicon nitride.

3.2.2. Fourier Transform InfraRed Spectroscopy

To analyze the change in atomic bonding in Si₃N₄, it is needed to detect the deuterium bonding. In FT-IR, each bonding absorbs specific wavelength of Infrared light and the results don't affect each other. The analysis can be employed for detecting and determining bond densities of light atoms such as H₂ or D₂. In 2008, G. Scardera investigated high temperature annealing effect on silicon-rich silicon nitride films using FT-IR spectroscopy [20]. Si-H bonding is detected by FT-IR measurement, allowing for investigation of changes in bonding ratio after annealing process. In 1995, Z. Lu's group also used FT-IR spectroscopy to check the RTA effect on a-Si:N:H(D) films, where Si-H and Si-N-H bonds are detected and Si-D and Si-N-D peaks are also detected [21].

In this experiment, FT-IR spectroscopy is applied to find out the D₂ passivation effect on silicon nitride bonding structure. Figure 6 shows the results of FT-IR spectroscopy on Si₃N₄ with D₂ passivation. A Thermo-Nicolet 5700 FT-IR spectrometer was used. With reference to previous studies, the range of the SiN-D peak is around 2400 cm⁻¹. As shown in Figure 6, the sample with D₂ HPA with 600 °C annealing shows slightly increased absorbance in the range of 2375 cm⁻¹. Considering the difficulty of detecting the light atoms (such as H₂ or D₂), more precise physical method should be studied.

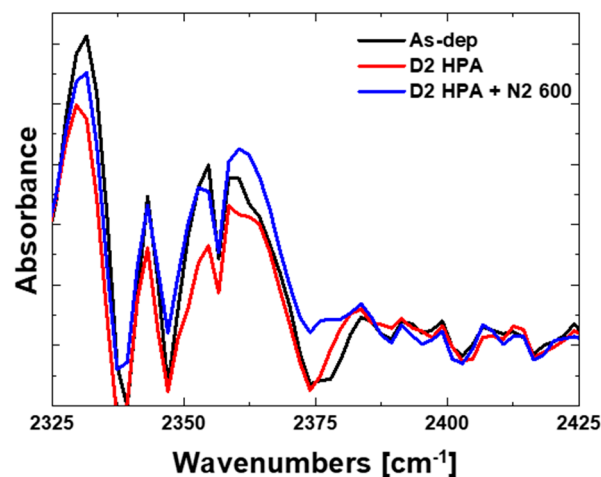


Figure 6. FT-IR result for silicon nitride comparing with the as-deposited sample and the D₂ passivated sample. The sample with D₂ HPA with 600 °C annealing shows slightly increased absorbance in the range of 2375 cm⁻¹.

4. Conclusions

In this study, the effects of D₂ HPA on Si₃N₄ are investigated in MNOS-type flash memory device. To focus on silicon nitride's trap control, D₂ passivation is conducted directly on Si₃N₄ films before metal deposition. The results show the memory window decreased after D₂ passivation, but the charge loss in retention mode after the program is suppressed, which becomes clearer as temperature increases. The D₂ passivation effect seems to be reinforced with post-annealing. Trap energy distribution based on the thermal activated retention model is also extracted to compare the trap density. The results show that D₂ passivation reduces the amount of trap densities in the band gap range of 1.06 eV–1.18 eV. SIMS and FT-IR spectroscopy are also applied to find out the deuterium profile and bond structure in Si₃N₄. SIMS results show that deuterium diffuses into the Si₃N₄ and exists up to the Si₃N₄-SiO₂ tunneling oxide interface region, which demonstrates the possibility of the deuterium passivation of shallow traps near Si₃N₄ and SiO₂ interface.

Author Contributions: Methodology, Formal Analysis, Investigation, Writing—original draft preparation. J.-Y.S.; Data Curation, Visualization, J.-K.J., W.-S.K. and J.-H.B.; Methodology, H.-D.L.; Conceptualization, Methodology, Writing—review and editing and Funding acquisition, Supervision G.-W.L. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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