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CMOS-compatible synaptic transistor gated by chitosan electrolyte-Ta$_2$O$_5$ hybrid electric double layer

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This study proposes a hybrid electric double layer (EDL) with complementary metal-oxide semiconductor (CMOS) process compatibility by stacking a chitosan electrolyte and a Ta$_2$O$_5$ high-*k* dielectric thin film. Bio-inspired synaptic transistors with excellent electrical stability were fabricated using the proposed hybrid EDL for the gate dielectric layer. The Ta$_2$O$_5$ high-*k* dielectric layer with high chemical resistance, thermal stability, and mechanical strength enables CMOS-compatible patterning processes on biocompatible organic polymer chitosan electrolytes. This technique achieved ion-conduction from the chitosan electrolyte to the In-Ga-Zn oxide (IGZO) channel layer. The on/off current ratio, subthreshold voltage swing, and the field-effect mobility of the fabricated IGZO EDL transistors (EDLTs) exhibited excellent electrical properties of 1.80×10^7, 96 mV/dec, and 3.73 cm^2/V·s, respectively. A resistor-loaded inverter was constructed by connecting an IGZO EDLT with a load resistor (400 MΩ) in series. This demonstrated good inverter action and responded to the square-wave input signals. Synaptic behaviours such as the hysteresis window and excitatory post-synaptic current (EPSC) variations were evaluated for different DC gate voltage sweep ranges and different AC gate spike stimuli, respectively. Therefore, the proposed organic–inorganic hybrid EDL is expected to be useful for implementing an extremely compact neural architecture system.

Neural systems have been actively investigated to replace traditional Boolean logic and von Neumann architecture[1,2]. Inspired by biological neurons and synapses, neural systems have many distinctive advantages, including massive parallelism, power-efficiency, storage/computation combination, and self-learning[3,4]. Two-terminal memristors, which use conducting filaments, phase change materials, and protonic layers between two electrodes, have been proposed for artificial synaptic devices through the various neural functions and geometric advantages[5–7]. However, cross-point array memristors are suppressed by the sneak current issue, in which the current flows through the unselected cells, and this can lead to low energy efficiency and excessive noise problems[8,9]. In contrast, multi-terminal synaptic devices are more appropriate for complex neural networks and real-time processing due to their additional gate terminals. When the voltage spike stimulus is applied to the gate terminals, the channel conductance between the source and the drain terminals is modulated. Therefore, three-terminal synaptic transistors can be simultaneously realised for the functions of learning/memory with a high energy efficiency[1,10,11].

In the past few years, three-terminal synaptic transistors that are gated by ion-conducting electrolytes have attracted significant attention. The ion-conducting electrolytes are reasonable for the electric-double-layer (EDL) modulation, and they enable the EDL transistors (EDLTs) to achieve synaptic dynamic functions. The most important property of the EDL is to act like a nanogap capacitor (typical EDL thickness is ~ 1.0 nm). The specific capacitance of the EDL can be extremely large (~ μF/cm^2) due to the EDL effect and the induced high-carrier density is up to 10^{15} cm^{-2}. Therefore, the modulated EDL can precisely trigger an ionic excitatory post-synaptic current (EPSC) to control the synaptic plasticity for low power consumption, which is a connection strength between two neighbouring synapses[12–15].

Meanwhile, recent interest in using natural biomaterials has received significant attraction because they are eco-friendly and biocompatible for electronic systems. Chitosan is a natural cationic biopolymer that is derived

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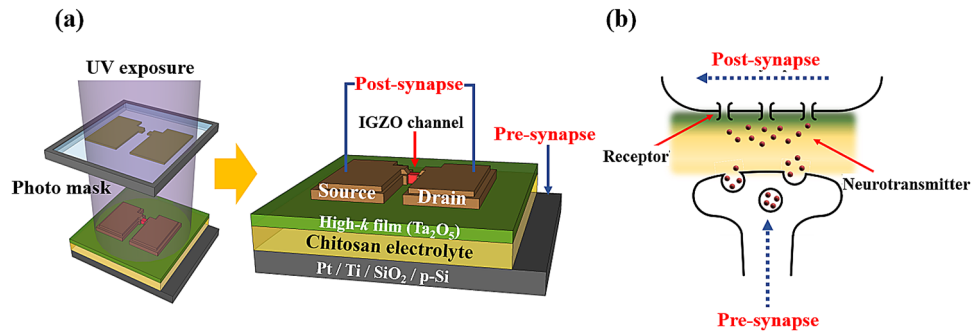
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Figure 1. Schematic of (**a**) the bottom-gate top-contact structure chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLTs fabricated by the photolithography process and (**b**) the simplified biological synapse.

from chitin, which is composed of repeated β(1,4)-linked D-glucosamine (*N*-deacetylated chitin) and *N*-acetyl-D-glucosamine units[16,17]. Chitosan-based bio-electrolyte is promising based on the following advantages, and it is widely investigated for the EDL. (1) Chitosan is the second most abundant polysaccharide on Earth and is extracted from the shells of crabs and shrimp; (2) Chitosan is an inexpensive, non-toxic, biocompatible polymer; (3) Chitosan is a low-cost solution that can achieve processability; (4) Chitosan has high-transparency and flexibility for its medium molecular weight; (5) Finally, chitosan has high-capacitance for protonic mobile ions[10,18,19]. In previous studies, numerous studies of chitosan electrolyte-based synaptic transistors, such as chitosan electrolyte-based metal–oxide–semiconductor channel-synaptic transistors on transparent glass substrate[19,20], synaptic transistors on flexible freestanding chitosan-based membranes[10,21], chitosan electrolyte-based SnO$_2$ nanowire channel synaptic transistors[22], and two-dimensional MoS$_2$ channel-synaptic transistors[23], have been extensively reported. This highly applicable chitosan electrolyte could offer not only artificial synaptic device applications but also versatile engineering platforms like skin-attachable, wearable, bio-sensor, and digestible smart electronics. However, despite the advantages of chitosan-based EDL, organic electrolyte-based EDLTs are hard to apply for the conventional complementary metal-oxide semiconductor (CMOS) process. This is attributed to their low chemical resistance, thermal, and ambient instabilities[24].

Therefore, in this study, we propose an organic–inorganic hybrid EDL. This is achieved by stacking a Ta$_2$O$_5$ high-*k* thin film on a solution-processed chitosan electrolyte layer to fabricate three-terminal synaptic transistors with excellent electrical characteristics and CMOS process compatibility. The excellent chemical resistance, thermal stability, and mechanical strength of the inorganic Ta$_2$O$_5$ film allowed the CMOS-compatible patterning process of the organic polymer chitosan electrolyte layer to obtain small feature size EDLTs. The transfer and output characteristics of the fabri19cated organic–inorganic hybrid IGZO EDLT were evaluated. In addition, by configuring an IGZO EDLT-based resistor-loaded inverter with load resistors that are connected in series, we verified the static voltage transfer characteristics and dynamic inverting characteristics. Finally, we evaluated the synaptic behaviours, such as the change in the hysteresis voltage for the direct current (DC) gate voltage sweep range and the variation in the EPSC for the alternating current (AC) gate spike stimulus.

Results

Photolithography process on chitosan electrolyte-Ta$_2$O$_5$ hybrid EDL. Figure 1a shows a schematic of the fabricated bottom-gate top-contact structure chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLT. The process of patterning the IGZO active channel and the top-contact source/drain (S/D) Ti electrodes was followed using a photolithography process for the chitosan electrolyte-Ta$_2$O$_5$ hybrid EDL. The dimensions of the fabricated EDLT are 20 μm for the channel width (W$_{CH}$) and 10 μm for the channel length (L$_{CH}$). Figure 1b illustrates a simplified schematic of a biological synapse. When the synaptic signal (stimulus) reaches the pre-synaptic neuron (Pt bottom-gate), it releases neurotransmitters from the pre-synapse. Subsequently, the receptors capture the neurotransmitters, and this can lead to the potential change in the post-synaptic neuron (IGZO channel)[1,25].

In the organic–inorganic hybrid EDLT that is displayed in Fig. 1a, the organic polymer chitosan electrolyte functions as a neurotransmitter to mimic the synaptic behaviour. However, despite the remarkable imitation properties for the synapses, it is hard to apply a photolithography process that is essential for device integration on an organic electrolyte layer due to swelling and an insufficient chemical resistance[18,21,24,26]. Although the chitosan patterning process in a previous study was conducted by electrodeposition or mould casting that was used at both micro and macro levels[27]. we developed a CMOS-compatible patterning process by performing photolithography.

Figure 2 shows the optical microscope images of the fabricated bottom-gate top-contact EDLTs. In the absence of the Ta$_2$O$_5$ high-k thin film, as shown in Fig. 2a,b, the EDL undergoes swelling or outgassing during baking or photolithography. This indicates that the chemical resistance of the chitosan electrolyte is insufficient. In contrast, as shown in Fig. 2c, the hybrid EDL with the Ta$_2$O$_5$ high-k thin film on the baked organic polymer chitosan layer was well prepared without swelling or outgassing during photolithography (see Supplementary Information Figure S1). Accordingly, it has been determined that the Ta$_2$O$_5$ high-k thin film acts as an effective barrier to prevent deformation of the organic polymer chitosan layer to ensure a stable CMOS patterning process.
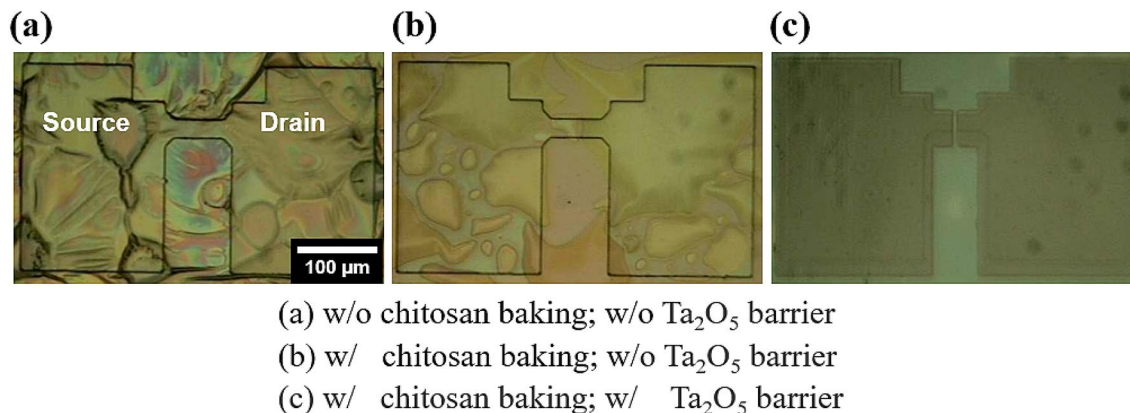
(a) w/o chitosan baking; w/o Ta$_2$O$_5$ barrier
(b) w/ chitosan baking; w/o Ta$_2$O$_5$ barrier
(c) w/ chitosan baking; w/ Ta$_2$O$_5$ barrier

Figure 2. Optical microscopic images of the EDLTs fabricated by the lithography process. (**a**) Without chitosan baking and without the Ta$_2$O$_5$ thin film. (**b**) With chitosan baking and without the Ta$_2$O$_5$ thin film. (**c**) With chitosan baking and with the Ta$_2$O$_5$ thin film. (**a**) and (**b**) show the deformed EDL, and (**c**) shows the normal EDL.
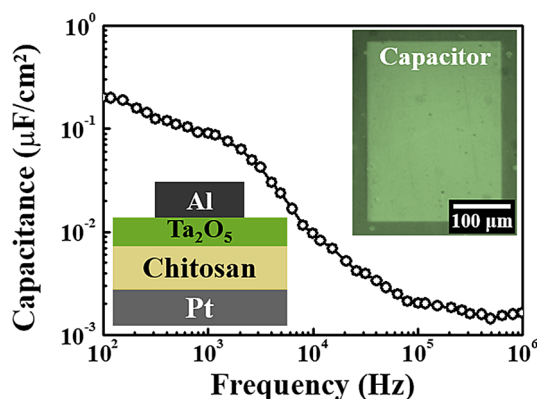

Figure 3. Capacitance–frequency (C–*f*) curve for the chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLC that is measured in the frequency range from 10^2 to 10^6 Hz. The insets show the schematic and the optical microscope image of the hybrid EDLC.

Electrical properties of the chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLT. To evaluate the dynamic behaviour of the chitosan electrolyte, the capacitance–frequency (C–*f*) curve characteristics of the Al/Ta$_2$O$_5$/chitosan/Pt structure EDL capacitor (EDLC) were measured in the frequency range of 10^2–10^6 Hz. As a result, a specific capacitance profile is clearly expressed for the specified frequency range as shown in Fig. 3. As demonstrated, the capacitance increases with a decreasing frequency, and the maximum capacitance of ~0.2 μF/cm^2 was obtained at a frequency of 10^2 Hz. This strong frequency-dependent capacitance can be originated from the EDL effect through the mobile ions within the chitosan electrolyte[23,28–30]. There are many mobile ions in the chitosan electrolyte, which includes anions and cations.

Figure 4a shows the transfer characteristics (I$_D$–V$_G$) of the chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLT. Moreover, to evaluate the hysteresis characteristics of the EDLT, the drain current (I$_D$) was measured for the dual-sweep mode with a drain voltage (V$_D$) of 1 V, the gate voltage (V$_G$) was swept from – 3 to 3 V, and back to – 3 V. The threshold voltage (V$_{th}$) was obtained by extrapolating the linear curve for the transfer characteristics, which was – 0.19 V; this exhibited a high on/off current ratio of about 1.8×10^7. The subthreshold voltage swing (SS) and field-effect mobility (μ$_{FE}$) were 96 mV/dec and 3.73 cm^2/V·s, respectively, and these were obtained by the following equations:

$$SS = \left[\left(\frac{d\log I_D}{dV_G} \right)_{max} \right]^{-1} \tag{1}$$

and

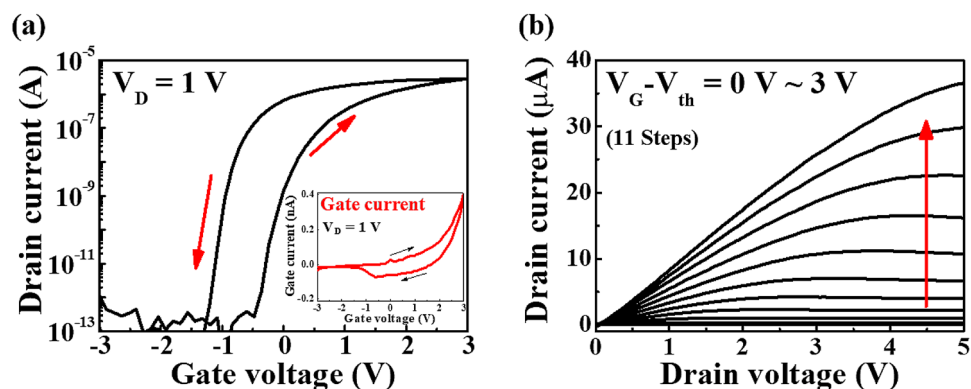$$\mu_{FE} = \frac{L}{W \cdot C_i \cdot V_D} \cdot \frac{dI_D}{dV_G} \tag{2}$$

Figure 4. Electrical properties of the chitosan electrolyte-Ta$_2$O$_5$ hybrid EDLT. (**a**) The transfer characteristics, where V$_G$ was swept from − 3 to 3 V in the dual-sweep mode at V$_D$ = 1 V. The inset shows the gate leakage current. (**b**) The output characteristics (I$_D$–V$_D$) measured by V$_G$–V$_{th}$ from 0 to 3 V in 0.3 V steps.
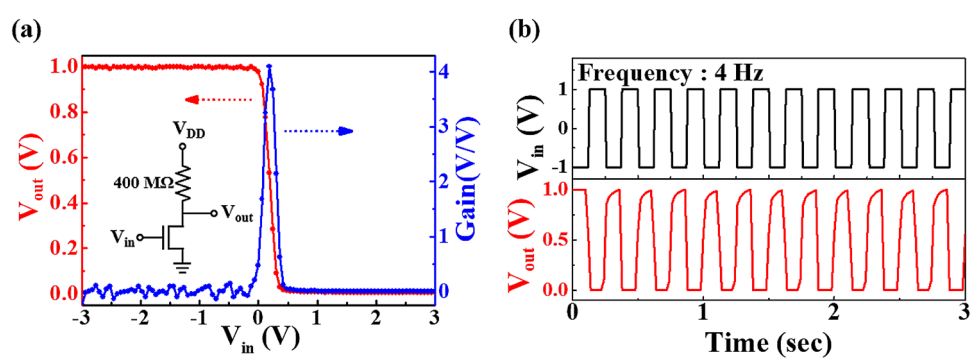

Figure 5. Resistor-loaded inverter characteristics of the chitosan-Ta$_2$O$_5$ hybrid EDLT. (**a**) The VTC curve and voltage gain were obtained by connecting a load resistor of 400 MΩ in series (V$_{DD}$ = 1 V). The inset is a simple schematic of an equivalent circuit for a resistor-loaded inverter. (**b**) The dynamic inverting response properties at a frequency of 4 Hz.

where L is the channel length, W is the channel width, and C$_i$ is the gate capacitance per unit area from the EDLC. In addition, the hysteresis window (ΔV$_{th}$) was defined as the difference between the threshold voltages for the forward sweep (V$_{th}^f$) and the backward sweep (V$_{th}^b$), $\Delta V_{th} = V_{th}^f - V_{th}^b$. As a result, a slow polarisation reaction by the mobile ions in the chitosan electrolyte induces a counter-clockwise hysteresis and the ΔV$_{th}$ is 0.92 V[18]. The inset of Fig. 4a is the gate current of the chitosan electrolyte-Ta$_2$O$_5$ hybrid type EDL in the transfer operation, which shows a low leakage current of 0.4 nA at 3 V. Figure 4b shows the output characteristics (I$_D$–V$_D$) that are measured by V$_G$–V$_{th}$ from 0 to 3 V by performing steps that are 0.3 V. In the low V$_D$ region, the I$_D$ linearly increases with an increasing voltage, which indicates ohmic contact between the IGZO channel layer and the metal (Ti) S/D electrode. In addition, as the V$_D$ further increases, the I$_D$ gradually becomes saturated and it exhibits pinch-off characteristics.

Figure 5 shows the static voltage transfer characteristics (VTC) and the dynamic inverting characteristics measured from a simple resistor-loaded inverter circuit. This was built by connecting a load resistor of 400 MΩ in series to a chitosan electrolyte-Ta$_2$O$_5$ hybrid type EDLT. As shown in the equivalent circuit of the inset in Fig. 5a, the source electrode of the EDLT was fixed at a ground voltage, and the supply voltage (V$_{DD}$) of 1 V was applied to a resistor that was connected in series to the drain electrode. Figure 5a shows the VTC curve of the inverter with the input voltage (V$_{in}$) applied to the pre-synapse gate electrode. When the V$_{in}$ is low (V$_{in}$ < − 0.1 V), the driver EDLT is in the "OFF" state, which was obtained with a high output (V$_{out}$) of ∼ 1 V. However, when V$_{in}$ is relatively high (V$_{in}$ > 0.4 V), the driver EDLT is in the "ON" state, which was obtained with a low V$_{out}$ of ∼ 0 V. It can be observed that an abrupt voltage transition of V$_{out}$ occurs in the VTC curve in response to V$_{in}$ at ∼ 0.3 V. The voltage gain (−dV$_{out}$/dV$_{in}$) from the VTC curve of the resister-loaded inverter is ∼ 4.1 (V$_{DD}$ = 1 V). Figure 5b is a dynamic inverting response of the resistor-loaded inverter, which switches between − 1 V and + 1 V in response to a square-wave V$_{in}$ with a frequency of 4 Hz (V$_{DD}$ = 1 V). The resistor-loaded inverter exhibits good inverting action and well responds by following a low-power square-wave input signal. Such relaxation time along the order of milliseconds appeared in the output signal is known to be related to the migration and the accumulation of protons in the chitosan electrolyte[19,30]. This long relaxation time is a drawback in traditional
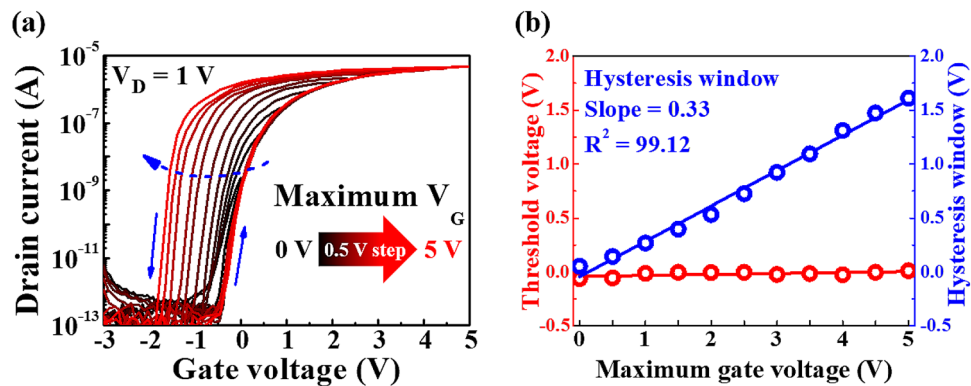
Figure 6. (**a**) Transfer characteristic curves of the chitosan electrolyte-Ta_2O_5 hybrid EDLT according to the V_G sweep range. Maximum $V_G = 0$ to 5 V, in 0.5 V increments. (**b**) Dependence of the hysteresis window and the V_{th} on the maximum V_G.

logic circuit applications, but it is rather favourable in the operation of low-power artificial synaptic electronics, which suggests potential applications[13,31,32].

Synaptic operations of the chitosan electrolyte-Ta_2O_5 hybrid EDLT.

The transfer characteristics presented in Fig. 4a display a counter-clockwise hysteresis window that is induced by the mobile ions in the chitosan electrolyte. To identify the magnitude of the polarisation response due to the migration of the mobile ions, we evaluated the transfer characteristics of the chitosan electrolyte-Ta_2O_5 hybrid type EDLT according to the V_G sweep range. Figure 6a shows the change in the counter-clockwise hysteresis window of the transfer characteristics that is measured in the dual-sweep mode according to the V_G sweep range ($V_D = 1$ V). It can be observed that the hysteresis window increases as the maximum V_G increases from 0 to 5 V in 0.5 V increments. Figure 6b shows the V_{th} and hysteresis window that is extracted from the transfer characteristic curves for the maximum V_G. As the maximum V_G increased from 0 to 5 V, V_{th} remained almost constant, while the hysteresis window exhibited a linear increase from 0.05 to 1.61 V. The relationship between the maximum V_G and the hysteresis window has high linearity (> 99%) with a slope of 0.33 V/V. The polarisation of the dipoles in the Ta_2O_5 high-k dielectric and the migration of mobile ions in the chitosan electrolyte induce charge carriers at the interface of the IGZO channel/hybrid type EDL. In addition, changes in the gate electric field can cause dipole alignment and migration of the mobile ions. The larger the maximum V_G, the larger the electric field, which can result in a stronger dipole alignment and ion movement. This makes it difficult to quickly return to the original state during the backward V_G sweep. This leads to a decrease in V_{th} and an increase in I_D; thus, resulting in greater hysteresis for the transfer characteristics during the dual-sweep mode. This hysteretic phenomenon is initialised by applying a relatively large negative $V_G = -3$ V, where the dipoles and migrated mobile ions are fully depolarised, and they release the charge carriers from the conductive channel. Therefore, the drain current of the chitosan-Ta_2O_5 hybrid EDLT returns to the initial off state. These initialisation properties and linear relationships of the maximum V_G vs hysteresis window indicate that the proposed device can mimic the biological synapse[33–35].

In the biological neural systems, synaptic plasticity is considered as the function for the mimicking synaptic operations of the EDLTs. In Fig. 1b, the mobile ions in the chitosan electrolyte are used as the neurotransmitters, which deliver the spike stimulus from the pre-synapse to the post-synapse. Therefore, the EPSC of the IGZO channel can be modulated by the synaptic weight[36,37]. To evaluate this behaviour for the biological synaptic operation of the chitosan electrolyte-Ta_2O_5 hybrid type EDLTs, a pre-synaptic spike (1 V, 100 ms) was applied to the bottom-gate electrode and a readout voltage ($V_D = 1$ V) for the EPSC measurement was applied between the S/D electrodes. Figure 7a shows the EPSC response according to the number of pre-synaptic stimulus spikes. When a single spike pulse is applied to the gate, the EPSC reaches a peak level ≈ 140 nA at the end of the stimulus, and then it rapidly decays to a resting current level ≈ 25 nA in milliseconds. This short EPSC duration time represents the short-term potentiation (STP). This occurs as a concentration gradient due to the migration of mobile ions by the stimulus, as it returns to equilibrium in a short time. In contrast, when multiple spike pulses are applied to the gate, the magnitude of the EPSC steadily increases with the number of spikes until the final stimulus, and then it decays gradually. Figure 7b shows the decay of the EPSC after the spike stimulus over time with respect to the number of spike pulses. It can be determined that the EPSC successively increases as the number of gate pulses increases. In contrast to the response after a single spike pulse, the EPSC after multiple spike pulses did not decay to the resting current level after 20 s from the peak current. This long EPSC duration time represents the long-term potentiation (LTP). Furthermore, as the number of pulses increases, the peak current and the resting current levels increase. By having a greater number of pulses, there is a greater concentration gradient of mobile ions in the chitosan electrolyte (ion charging process) and this increases the time to return to equilibrium (ion discharge process)[10,18,36]. In addition, there is a large number of traps due to the structural imperfections at the chitosan/Ta_2O_5 interface. As the number of protons increases with an increase in the number of pulses, the number of protons captured at this interface also increases; thus, resulting in a longer EPSC duration.
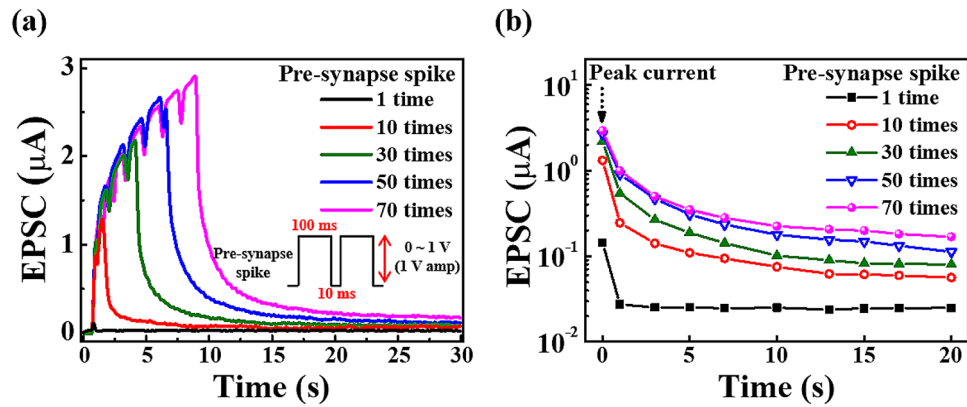
Figure 7. (**a**) EPSC response according to the number of pre-synaptic stimulus spikes (1 V, 100 ms). (**b**) The decay of the EPSC stimulated by a different number of pre-synaptic gate pulses.
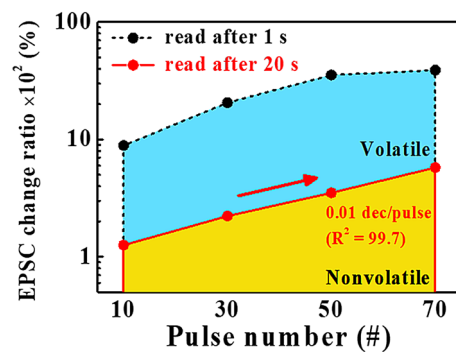

Figure 8. Dependence of the EPSC change ratio, $((I–I_0)/I_0 \times 100\%)$, according to the pulse spike numbers. I_0 is the resting current and I is the EPSC in the channel after the pre-synaptic stimulus.

The residual EPSC after 20 s over time is significantly enhanced with an increase in the spike pulse numbers, which indicates a different trend from the STP to the LTP. Figure 8 shows the pulse number dependence of the EPSC change ratio, $((I – I_0)/I_0 \times 100\%)$, where I_0 is the resting current and I is the EPSC of the channel after the pre-synaptic stimulus. The rate of the EPSC change increases with the number of pulses in the volatile and non-volatile regions. In addition, the non-volatile region is gradually increased with the number of pulses, which follows the linear relationship respect to the EPSC change ratio slope of 0.01 dec/pulse number ($R^2 = 99.7$). This suggests the possibility of biocontrol for the magnitude of the STP and the LTP, which can be used as short-term and long-term memory, respectively, at artificial synapses[1,36,38].

Conclusion

This study proposes bottom-gate top-contact structure synaptic transistors that are gated by an organic–inorganic hybrid EDL. The CMOS-compatible patterning processes on the organic polymer chitosan electrolytes were successfully conducted through the stacking of a biodegradable chitosan electrolyte and the Ta_2O_5 high-k dielectric thin film. The value of the chitosan electrolyte-Ta_2O_5 hybrid EDL capacitance is increased by decreasing the frequency. In addition, a large capacitance $\sim 0.2\ \mu F/cm^2$ was obtained at 10^2 Hz. The on/off current ratio, V_{th}, SS, and μ_{FE} values of the chitosan electrolyte-Ta_2O_5 hybrid EDLT were 1.80×10^7, – 0.19 V, 96 mV/dec, and 3.73 $cm^2/V{\cdot}s$, respectively. In addition, they exhibit an abrupt voltage transition in the VTC and good dynamic inverting actions to the low-power square-wave input signals for the resistor-loaded inverter circuit. In terms of the biological synaptic operation, the chitosan electrolyte-Ta_2O_5 hybrid EDLT represents a linear polarisation magnitude relationship through the maximum V_G with a constant V_{th}. Finally, the EPSC is modulated by the pre-synaptic stimulus numbers and it has an increased portion of the STP and LTP because the stimulus number is increasing. As a result, the EDLT gated by the chitosan electrolyte-Ta_2O_5 hybrid EDL is expected to provide compact neural architecture systems. This can be achieved by applying a CMOS-compatible photolithography process with excellent electrical properties and synaptic operations.

Methods

Solution synthesis procedure. The solution of the chitosan electrolyte was synthesised by the sol–gel reaction of the chitosan powder and acetic acid. The dried form of the chitosan powder and the flakes are typically insoluble in distilled water. The shrimp shell-based chitosan powder with a medium molecular weight (deacetylation degree > 75%, Sigma Aldrich) was dissolved (2 wt%) in 2% acetic acid solution (> 99%, Sigma Aldrich), which was diluted with distilled water. Subsequently, the solution was mixed under 800 rpm at 50 ℃ in a constant magnetic stirring system for 6 h. Subsequently, the solution was filtered through a polytetrafluoro-ethylene (PTFE) syringe filter with 5-μm pore-size to remove the particulates.

Device fabrication procedure. The bottom-gate top-source/drain structure chitosan electrolyte-Ta_2O_5 hybrid EDLTs were fabricated as follows. The 300 nm-thick thermally grown oxide on the (100)-orientated p-type silicon wafer was used as a starting material, and it was cleaned by a standard RCA process. First, the 10-nm-thick Ti and 100 nm-thick Pt were sequentially deposited by using an E-beam evaporator for a bottom-gate (pre-synapse). Second, to form the chitosan electrolyte-Ta_2O_5 hybrid EDL, the chitosan solution was spin-coated and dried at room temperature (25 °C) for 24 h. Then, the samples were oven-baked at 130 °C for 10 min to remove the residual moisture in the chitosan electrolyte film. In sequence, an 80 nm-thick Ta_2O_5 high-k dielectric was deposited on a 130-nm-thick chitosan layer by the radio frequency (RF) magnetron sputtering system with a 20 sccm-Ar flow rate, 3.0 mTorr-working pressure, and a 75 W-RF power. Third, the 50 nm-thick IGZO channel layer was also deposited by the RF magnetron sputtering system with a 30 sccm-Ar flow rate, 6.0 mTorr-working pressure, and a 100 W-RF power. The active patterning process of the IGZO channel layer was performed by a positive type photolithography technique and a wet etching process with a 30:1 ratio for the buffer oxide etchant. Finally, 100-nm-thick Ti source/drain electrodes (post-synapse) were deposited by the E-beam evaporator and they were patterned through the lift-off method. The defined channel width and length were 20 μm and 10 μm, respectively. The fabricated chitosan electrolyte-Ta_2O_5 hybrid EDLTs were positioned at room temperature (25 °C) in a dark box to avoid light and electrical noise. The electrical characteristics and synapse operations of the fabricated devices were investigated using the Agilent 4156B Precision Semiconductor Parameter Analyser and they were pulsed by the Agilent 8110A Pulse Generator. In addition, the C-f curve characteristic of the Al/Ta_2O_5/chitosan/Pt structure EDLC was measured at the frequency range of 10^2 to 10^6 Hz by using Agilent 4284A Precision LCR Meter.

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Competing interests

The authors declare no competing interests.

Additional information

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