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Source-gated transistors for order-of-magnitude performance improvements in thin-film digital circuits

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Ultra-large-scale integrated (ULSI) circuits have benefited from successive refinements in device architecture for enormous improvements in speed, power efficiency and areal density. In large-area electronics (LAE), however, the basic building-block, the thin-film field-effect transistor (TFT) has largely remained static. Now, a device concept with fundamentally different operation, the source-gated transistor (SGT) opens the possibility of unprecedented functionality in future low-cost LAE. With its simple structure and operational characteristics of low saturation voltage, stability under electrical stress and large intrinsic gain, the SGT is ideally suited for LAE analog applications. Here, we show using measurements on polysilicon devices that these characteristics lead to substantial improvements in gain, noise margin, power-delay product and overall circuit robustness in digital SGT-based designs. These findings have far-reaching consequences, as LAE will form the technological basis for a variety of future developments in the biomedical, civil engineering, remote sensing, artificial skin areas, as well as wearable and ubiquitous computing, or lightweight applications for space exploration.

Flexible, large-area electronic (LAE) circuits are particularly attractive due to their potentially simple, low-cost of manufacturing and high throughput. Research has concentrated on improving material properties and refining device design, in order to improve power efficiency[1], speed of operation[2–5] and stability of performance during and after electrical[5,6] and mechanical[7,8] stress. New forms of air-stable semiconductor materials, which allow low-temperature deposition from solution[3,4,9–12], have been invented. Concurrently, conventional large-area technologies are being adapted to permit processing on plastic substrates with minimal performance loss[2,13]. Despite these continuing improvements, the architecture of the fundamental building-block used for LAE, the thin-film field-effect transistor (TFT, FET) has seen little development in comparison to the changes observed in nanoscale devices for ultra-large-scale integrated circuits (ULSI)[14–17]. Furthermore, many applications do not require particularly fast circuits, but current uniformity, stability and tolerance to geometric variations which are more likely to occur in low-cost large-area technologies such as printing.

The source-gated transistor (SGT)[18–21], a device suitable for LAE, allows improved energy efficiency[22], bias stress stability[23], tolerance to process variations[24] and gain[22,25,26] to be achieved in analog circuits with minimal changes to standard fabrication processes. This device concept is now being studied in a multitude of material systems[25,27–35] after first being identified as having different operation to conventional, and indeed Schottky-barrier, field-effect transistors by Shannon and Gerstner[19]. In reality, as SGT structure is very similar to a conventional FET and in many technologies it is easier to obtain a SGT than a FET, SGTs have been observed[36] without explanation[37] much earlier.

Three major aspects determine transistor operation as a SGT (Fig. 1a): the source electrode purposely comprises a potential barrier; the gate overlaps the source; and drain bias is able to deplete the semiconductor fully at the source edge[19,20]. Apart from accumulating charge at the semiconductor/insulator interface, the gate electric field also modulates the effective barrier height at the source by penetrating to the source contact in the depleted region. Current is controlled by the reverse biased source barrier (in Mode 1 through modulation of the barrier height at the edge of the source electrode closest to the drain – I_1 in Fig 1a, and in Mode 2 by the restrictive action of the JFET-like depletion region which forms under the edge of the source – I_2); the conductive ("parasitic") FET channel between source and drain plays no role as long as it is more conductive than the barrier. Electrical behaviour differs from standard FETs, with the current inevitably lower for a fixed geometry, but with important

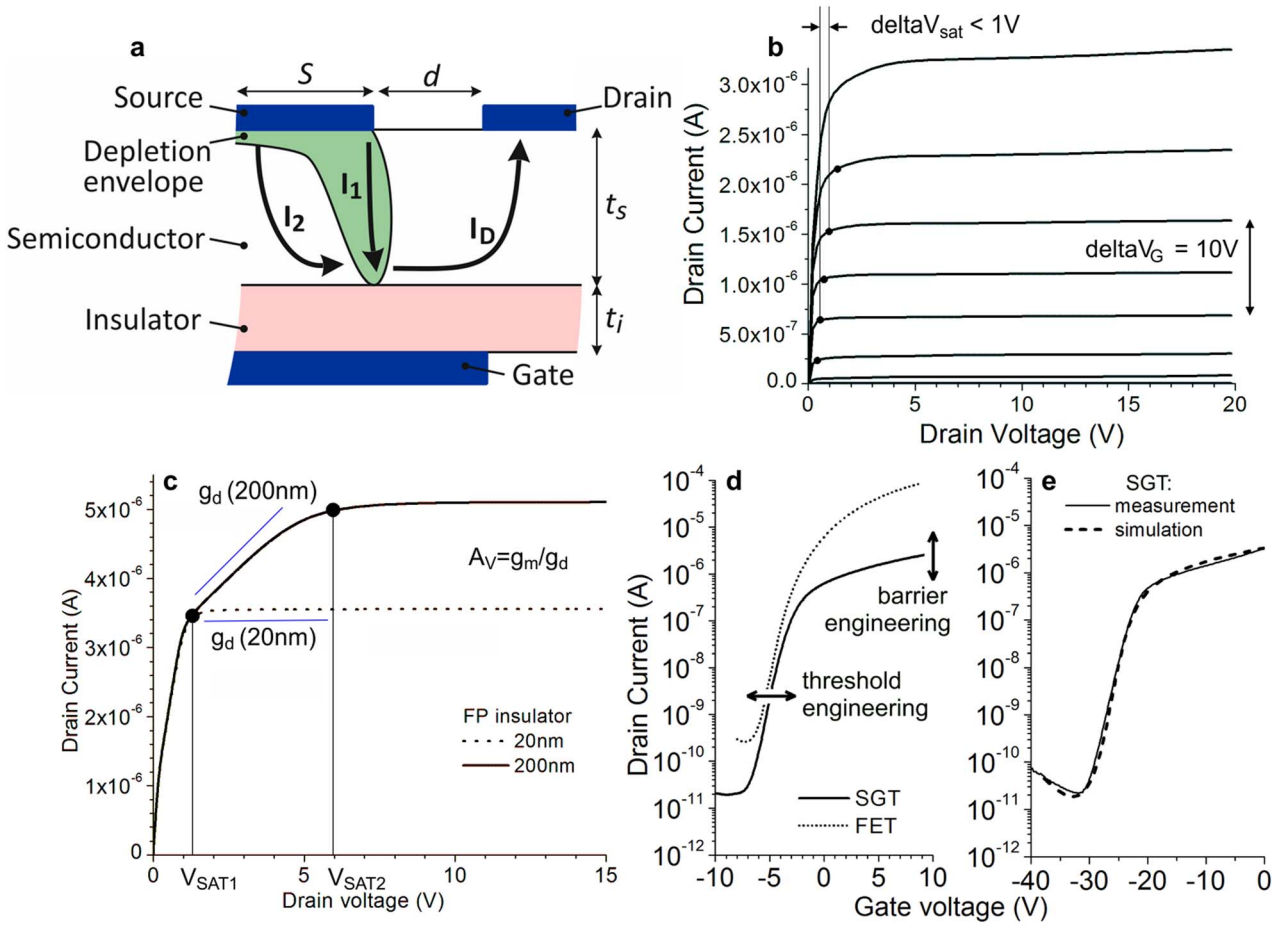

Figure 1 | Source-gated transistor operation. (a) Cross-section of the fabricated polysilicon source-gated transistor, showing device structure, design parameters, current paths and depletion envelope at the source under small drain bias; (b) Measured output characteristics of a poly-Si SGT, showing very low dV_{SAT}/dV_G and flat saturated curves. $d = 6$ μm, $S = 4$ μm, $W = 50$ μm; (c) Simulation based on the fabricated polysilicon devices. The effectiveness of the field plate increases as it is brought closer to the semiconductor and the curve becomes much flatter between V_{SAT1} and V_{SAT2}, allowing high gain to be available from very low drain voltage; (d) Measured transfer characteristics for a FET and SGT of the same geometry as (b) in polysilicon at $V_D = 5$ V. The SGT curve can be tuned by barrier engineering; (e) SGT modeling agrees well with experiment.

advantages[19–22,25–27]. Output characteristics show very early saturation and can be extremely flat (Fig. 2b), improving gain and power efficiency in analog circuits[22,26].

The source-controlled nature of the current affords important application benefits: transistors are more stable during electrical stress and the impact of process variability is minimized (registration[24], layer thickness[38], electrode gaps[35]). For large-area, low-cost electronics, such as robust current drivers or remote sensor amplifiers, these are essential features which by using SGTs come without the need for high-end, expensive specialist fabrication processes. Moreover, the SGT concept can be applied to virtually any semiconductor system and can be used in parallel with conventional FET-type devices in the same circuit without the need of complex process alterations.

Here, we demonstrate the suitability of SGTs for low-cost digital circuits, substantially increasing noise resilience and improving energy efficiency. Operation in noisy environments, with low signals, limited energy and variable supply voltage levels can be greatly improved. We envisage that applications such as remote sensors with local data processing, fabricated in low-cost technologies would benefit from this technology. Biological sensors handling weak but slow-changing signals, embedded sensors for civil engineering projects, and product identification tags with rudimentary built-in data processing, all made in low-cost, high-throughput fabrication processes, are examples of such implementations.

Results

Polysilicon source-gated transistors have been fabricated and measured as discussed in the Methods section. Figure 1a shows a typical device cross-section. These SGTs comprise a potential barrier at the source, and an ohmic drain. Measured output characteristics are illustrated in Figure 1b. The structure behaves as typical source-gated transistors, with very low saturation voltage $V_{SAT} \equiv V_{SAT1}$[19,20], very flat output characteristics (low small signal output conductance) over a wide range of drain voltage, and an almost complete absence of the kink effect[39–43]. The output conductance (g_d) can be further improved by operating the device in the "Mode II"[18,38] (in which the current is controlled primarily by the pinch-off region at the source rather than gate-field-induced barrier lowering) or by introducing a field-plate in the structure of the source electrode. For this study we have chosen the latter, as it is intrinsic to the technology. Figure 1c shows the effect of the field plate. The edge of the source is screened from the barrier-lowering effect of the drain field[22,26] and field plate effectiveness increases if close to the active layer surface. The biggest benefit occurs for V_D between V_{SAT1} (source pinch-off according to Shannon and Gerstner's dielectric model)[20] and $V_{SAT2} = V_G - V_{th}$ (conventional drain pinch-off). In Figure 1d, measured transfer characteristics are compared to that of an identically-sized FET. (By swapping the source and drain terminal, the same structure can be operated as a FET with an ohmic source and a forward-biased Schottky barrier at the drain). The SGT has lower current above threshold, as the source

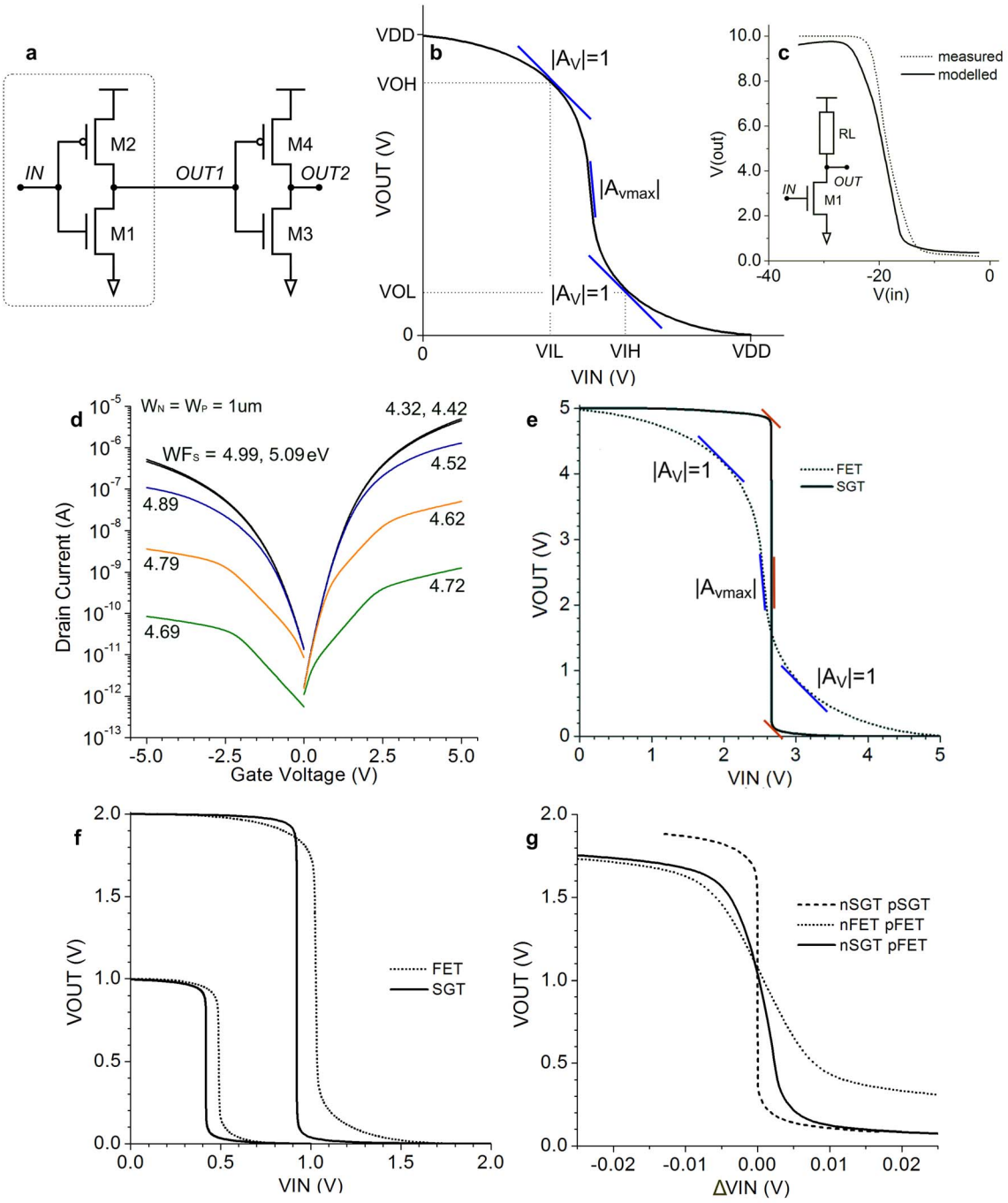

Figure 2 | Source gated transistors as building-blocks for inverters. (a) Schematic showing circuit setup and node names; d.c. simulations were performed on the circuit in the dotted area; the whole circuit was used for transient; (b) Complementary inverter transfer plot (sketch). For best noise immunity and robustness, $|Av_{max}|$, V_{OH} and V_{IL} should be increased and V_{OL} and V_{IH}, reduced; (c) SGT inverter with resistive load showing agreement between simulation and experiment; (d) Simulated transfer characteristics of *n*- and *p-type* SGTs with different source barrier heights. The curves are identified by the chosen source metal work function, which directly relates to the effective height of the source barrier. For very low barriers, both the *n*- and the *p-type* devices behave as FETs and the source barrier does not play a role. Source metals can be chosen such that the on-current of both *n*- and *p-type* devices which form an inverter is roughly similar. This ensures that the tripping voltage is in the middle of the supply range when *n*- and *p-type* devices are of the same width. (e) Simulated transfer curves for FET and SGT complementary inverters in polysilicon. Owing to low saturation voltage and flat saturated characteristics, the SGT circuit responds closer to ideal than the FET version, particularly as the FET curves are suffering from kink effect at supply voltages as low as $V_{DD} = 5$ V; (f) Comparison between FET and SGT inverters at lower supply voltages, $V_{DD} = 1$ V and 2 V; (g) magnified overlay of the transfer characteristics of FET, SGT and mixed pFET/nSGT CMOS inverters at $V_{DD} = 2$ V – for the mixed circuit, $W_{SGT} = 10$ μm and $W_{FET} = 1$ μm to account for the lower current obtained from the source-barrier limited SGT.

rather than the channel controls the current, with the magnitude of the current tuned through barrier engineering (e.g. implants in the source region and by choice of contact metal work function). A lower source barrier will yield higher current and larger transconductance (g_m). Much like with conventional devices, the threshold can be altered by choice of gate work function and by bulk doping.

A figure of merit for transistors is their intrinsic gain $A_V = g_m/g_d$, where transconductance $g_m = dI_d/dV_g$ and output conductance $g_d =$

dI_d/dV_d. Owing especially to the very flat output characteristics (extremely low g_d), in devices with field plates we have routinely measured gain values exceeding $A_V = 10^5$ [26], several orders higher than in standard FETs. These gain characteristics coupled with low-voltage saturation are of benefit not only to analog applications such as amplifiers, current drivers and active loads but also when designing logic gates. Figure 1e illustrates the agreement between the measured device and numerical model, which serves as a component for the inverter simulation.

Simple CMOS inverters comprising SGTs have been created using the mixed-mode (physical and circuit co-simulation) capabilities of Silvaco Atlas. For d.c. simulations, a single inverter was used, whereas for transient analysis the inverter studied was loaded with an identical circuit to approximate real-world operation (Figure 2a).

Discussion

Inverters are basic logic gates used extensively in digital circuits. Complementary inverters (using *n-* and *p-type* devices) have long been the standard for ULSI logic due to their negligible power draw in steady state, abrupt switching and relatively compact layout size. Emerging processes are beginning to include complementary logic gates, but difficulties related to relative carrier mobility and additional processing steps mean these technologies are still in early development.

For our proof-of-concept simulations we used a classic two-transistor complementary design (Fig. 2a) with source-gated transistors in polysilicon. Polysilicon technology is mature yet still developing. Its major drawback is the kink effect[42,43], but as we have shown, SGTs are particularly good at eliminating this undesirable characteristic even in the absence of drain-side field relief. Figure 2b shows the d.c. input-output (transfer) characteristic of such an inverter, alongside its figures or merit at d.c. or low-speed switching operation.

The polysilicon devices used in this study have been designed to operate as *n-type*. Supplementary Figure S1 shows the transfer characteristics of the same devices operated as both *n-type* and *p-type*. The associated output characteristics are illustrated in Supplementary Figure S2. As a result of the poor output characteristics and high negative turn-off voltage when working as *p-type*, these devices are unsuitable for fabricating the high-performance CMOS inverters discussed in this section (a longer channel marginally improves the characteristics for *p-type* operation as described in Supplementary Figures S3 and S4). Nevertheless, these results show that it is possible to realise *p-type* SGTs and performance should improve considerably if their architecture is optimised for the purpose.

Using Silvaco ATLAS we have modeled poly-Si SGTs with Schottky source barrier. We fitted our model to measured devices (Fig. 2c) and then tuned them to obtain small threshold voltages. We chose d = 4 μm as our source-drain gap, which is a typical value for polysilicon FET technology, in order to show the gain performance of SGT inverters compared to conventional FET-based designs. Even at this channel length conventional FETs generally would manifest short channel effects and, consequently, poor saturation characteristics, exacerbated by the kink effect. The simulated devices had field plates 1 μm long separated from the semiconductor by 20 nm of SiO_2. This metallic overhang around the contact, which extends into the channel region of the transistor is a design rule in most lithographical processes, and as such, does not lead to increased fabrication complexity. By using this overhang as a field relief structure, we improve the saturation characteristics of the SGT[22]. From Figure 2d we can see that the source barrier of *n-* and *p-type* devices can be tuned by choice of source metal. Moreover, combinations of source metals for *n-* and *p-type* devices can be chosen in order to achieve similar on-currents for both devices, leading to the possibility of using the same width for both devices in the CMOS inverters. Here we have used $W_N = W_P = 1$ μm. Naturally, this will come at the expense of reduced current in the *n-type* device, as *p-type* SGTs will inherently be limited in the maximum current they can achieve by the "FET envelope": as the source barrier decreases, the SGT (*n-* or *p-type*) transitions to operation as a conventional FET, since the barrier eventually becomes more conductive than the channel for a given gate bias condition, and irrelevant for our purposes. The figure shows that for low barriers, changing the work function of the metal does not change the device characteristic (i.e. the source barrier does not contribute to current modulation) and the devices behave like FETs. The *p-type* FET has a lower on-current than the *n-type* device. This limits the amount of current that the *p-type* SGT can achieve and also imposes a similar limit on the *n-type* SGT current if an equal device width is desired when CMOS inverters are made with these devices. FET devices of identical geometry were also modeled for reference.

In Fig. 2e, we compare SGT and FET designs at a typical supply voltage $V_{DD} = 5$ V. The improved gain and noise margin of the SGT circuit can be immediately noted visually. The improved gain is due to the low output conductance (g_d) in saturation, helped by the field relief structure of the source-gated transistor. In turn, the larger noise margin, given by the squarer shape of the inverter transfer characteristic, is a consequence of the low saturation voltage characteristic of SGTs.

Lower voltage d.c. operation is compared in Fig. 2f. Here the FET is noticeably better but still inferior to the SGT. As supply voltage is reduced to 0.5 V, the characteristics become comparable. This is expected, since at very low gate bias the SGT is in fact operating in FET mode (the semiconducting channel is less conductive than the source barrier and controls the current), thus losing the electrical behaviour derived from operation in a source-limited fashion.

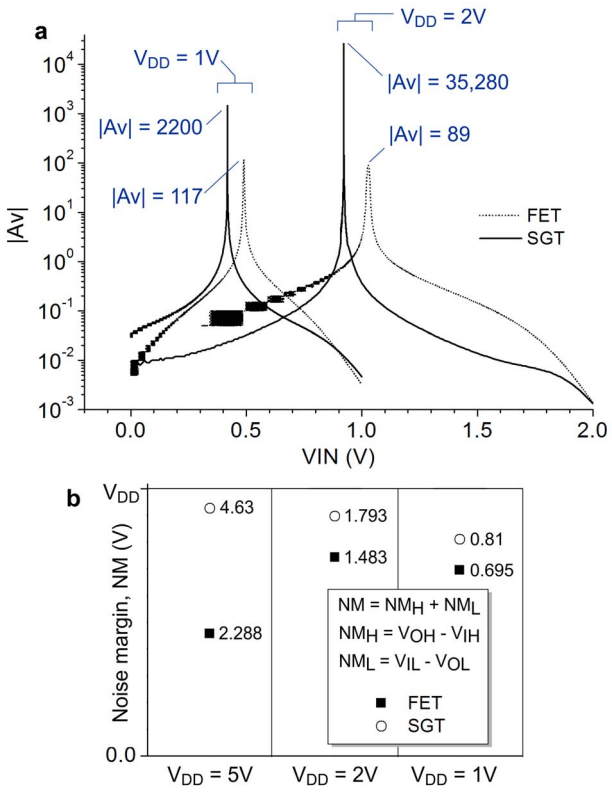

Figure 3 | SGT inverter performance: gain and noise margin. (a) Inverter gain is substantially higher in the SGT inverter. At low V_{DD}, this advantage diminishes slightly as the transistors operate in a regime which is less controlled by the barrier and more FET-like (Fig. 1d); (b) D. C. noise margin (as defined in Fig. 2b) for SGT and FET inverters at different supply voltages. At high V_{DD} the FET suffers from kink effect. At low V_{DD}, the SGT operates in a region of its transfer characteristic which is less controlled by the source barrier and thus more FET-like.

Figure 2g shows a magnified overlay of the inverter transfer characteristics around the tripping point (V_{OUT} = 1 V for V_{DD} = 2 V).

The inverter performance in curves of Figures 2e and 2f is analyzed in Figure 3a, where the gain of the SGT inverter is shown to be almost 400 times higher. The gain curves show a lower spread in the case of the SGT circuit, indicative of a narrower switching region, which should be beneficial to transient operation. Figure 3b shows a large improvement in noise margin (as defined in the inset) at V_{DD} = 5 V, where the FET begins to suffer from kink effect. As we decrease V_{DD}, the advantage of the SGT reduces as it behaves more like a FET. The large improvement in noise margin and the large noise margin as a proportion of supply voltage are essential for minimizing errors due to power supply glitches, electromagnetically coupled electrical noise and extreme operating conditions, such as large fan-out loads. Coupled with the low-cost, almost standard fabrication process, this display of circuit robustness recommends the SGT-based designs as reliable, cost-effective implementations for applications such as remote sensing and data processing.

Figure 4a compares current drawn by FET and SGT inverters during their d.c. switching cycles. The source-contact controlled current in the SGT is significantly lower, even for a comparatively low source barrier height. As a consequence, the SGT circuit will operate at lower speed. However, its more abrupt transition between logic states means that less time is spent in the high-current, transition region. In Fig. 4b we show the transient current drawn during switching with a square wave as input. The SGT inverter is indeed much slower, but since its output transition has much higher gain (Fig. 3a), switching power is lower, as is the power-delay product. Transient node voltages for the SGT circuit in Fig. 2a are given in Fig. 4c, showing adequate speed for a wide variety of large-area applications where circuit robustness, noise immunity and reliable fabrication in a low-cost process are more critical than speed of operation.

In the light of the above, digital SGT circuits show promise for large-area electronics in which robustness and noise immunity are critical as a consequence of the nature of their operating environment. Designs which incorporate SGTs may also address challenges relating to non-uniformity during patterning and physical distance between circuit segments in a large-area circuit.

We note that good d.c. inverter characteristics are observed when saturation voltage and output impedance are low. Interestingly, this happens in *n-type* organic FETs which use silicon dioxide as an insulator. The behavior, quite separate from that of the SGT, was first described by Siringhaus[44] and is based on a fundamentally different saturation mechanism than that of the SGT: semiconductor-insulator interface trapping contributes to early saturation and low or negative output resistance. Nevertheless, the effect is similar to that of SGTs when building CMOS inverters. Min et al. have fabricated[45] organic CMOS inverters from semiconducting nanowires (N2200 and P3HT : PEO-blend (80 : 20, w/w)) using SiO_2 as gate insulator. The measured output characteristics of the *p-type* transistors follow conventional FET behaviour, but the *n-type* devices show early saturation and negative output resistance (Figs. 2b and 2d, in Ref. 44, respectively). The inverters obtained using these devices (Fig. 5d in Ref. 44) show asymmetric transfer characteristics, with much better V_{OL} and V_{IH} when the *n-type* OFET, with its desirable saturation properties, acts as the load in the circuit. Moreover, the gain plot of the circuit, illustrated in the inset of the same figure, is equally asymmetric and shows a steeper slope in the switching voltage range. We note that, had both n- and p- transistors had low saturation voltage and high output impedance, the gain would have been significantly higher and V_{OH} would have also improved. As described in

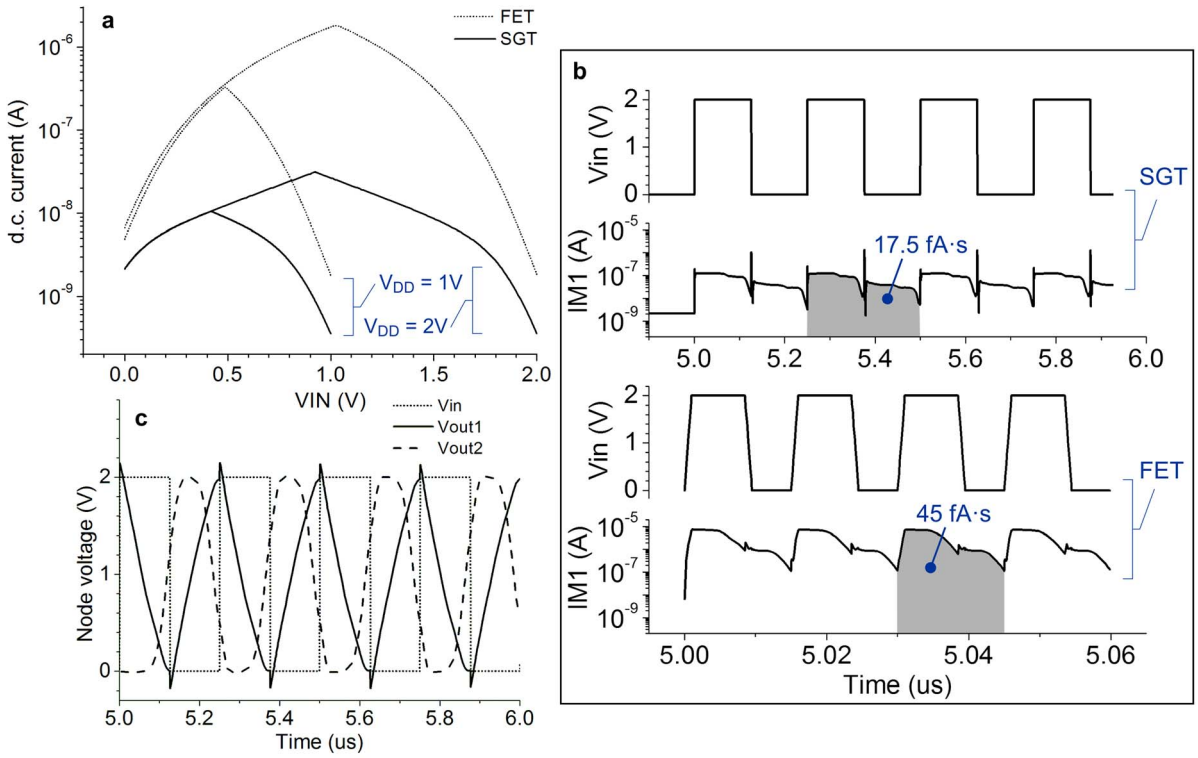

Figure 4 | Inverter power consumption and switching behavior. (a) Current consumption during a d.c. switching cycle for SGT and FET inverters without a load. The current in the SGT circuit is controlled by the source contacts and thus lower than in the FET circuit, leading to a larger time constant and reduced operating speed; (b) Transient current in transistor M_1 (Fig. 2a). The input waveform is given for reference. Highlighted areas are proportional to energy dissipated in one switching cycle (power-delay product – $PD = V_{DD} \cdot I_D \cdot t_{clock}$). The SGT switches slower but draws considerably less current leading to somewhat improved PD; (c) Transient node voltages for the SGT circuit in Figure 2 and driven with a square wave. Attainable speed is in the MHz range.

our analysis, using SGTs in inverter circuits would lead to this improvement.

Simulation of a mixed inverter, based on a *p-type* FET and an *n-type* SGT of the types considered in the present work, show the same behaviour (Figure 2g). This plot is similar to those in Figure 2e, but with $V_{DD} = 2$ V, chosen to emphasise the large gain achievable in the SGT circuit. This mixed configuration produces similar results to those discussed with respect to Reference 44. We have magnified the scale on the x-axis to better illustrate the characteristics around tripping point. The three curves show the FET, SGT and FET/SGT circuit characteristics. Specifically, for a *n-type* SGT and a *p-type* FET, ahead of the tripping point the curve has poor noise margin and low gain, following the behaviour seen in the FET-only circuit; after the tripping point, when the *n-type* SGT active, the curve has a sharper knee for improved noise margin and better gain than that of the FET circuit, approaching the SGT-only circuit characteristic.

In conclusion, we have performed numerical simulations of simple logic gates comprising source-gated transistors (SGTs) with parameters derived from measurements of fabricated structures. Poly-Si complementary inverters using SGTs exhibit important increases in noise margin (more than double at $V_{DD} = 5$ V and over 20% at $V_{DD} = 2$ V), 400 times better gain ($V_{DD} = 2$ V) and improved power-delay product than those made with FETs of identical geometry. This is due to the characteristic low-voltage saturation and flat output curves of the SGT. These findings are valid for other logic gates and should maintain similar trends in other technologies such as IGZO-based[27] or solution-processed[9,28,38] electronics. The challenge is to ensure that the device operates in Mode II[18,38], in which the current is practically insensitive to drain field, or screen the source barrier from the drain field using field-relief structures and thus improving low-V_D gain. The SGT's characteristics recommend it as an excellent analog device (low power, amplification, stability under electrical stress, uniformity of electrical characteristics with process variations) and an equally useful digital device (gain, noise margin, power-delay product). Importantly, its limited current and slower operating speed (than an identical FET), can be mitigated by the creation of hybrid FET – SGT circuits. As the fabrication of the two devices is only marginally different, designs incorporating both devices and taking advantage of their respective strengths are possible in a multitude of semiconductor material systems.

Methods

Fabrication. Source-gated transistors with drains which were self-aligned to the gate were made on glass substrates. The bottom gate metal (Cr) was patterned lithographically on the substrate. PECVD was used to deposit 200 nm SiN_x and 200 nm SiO_2 to act as gate insulator. The polysilicon active layer started as 40 nm of PECVD a-Si:H which was dehydrogenated by baking at 450°C and excimer laser crystallised. Various implants of BF_2 or P were used to give a range of doping levels. Using the gate as a mask and back exposure through the glass to define a positive resist, a high dose P implant was used to form drain contact regions aligned with the gate. After polysilicon formation, silicon islands were patterned on the substrate by dry etching. On top of the polysilicon, SiO_2 120 nm thick was deposited. Source contact windows were etched, followed by 5 keV BF2 or P implants which were used to modify the characteristics of the source contact. Thermal annealing of these implants was performed at 550°C. Chromium and AlTi metal layers were deposited and defined to form a Schottky source contact and field plate assembly. Finally, the structure was passivated using a thick layer of silicon nitiride, with openings for Cr/AlTi/Cr contact pads.

Measurement. An in-house Labview-controlled, PC-based data acquisition system was used for electrical measurements. Two Keithley 2400 source-measure units were used for applying gate and drain voltage. Source current was measured with a Keithley 6485 picoammeter. The setup was connected to manual micromanipulators with 25 μm tip Au probes, part of a Wentworth probe station with motorized XY, heated, electrically isolated stage. All measurements of polysilicon devices and circuits were performed in air at 31°C in ambient light conditions.

Simulation. Silvaco Atlas version 5.16.3.R was used to model *p-type* and *n-type* FETs and SGTs in two-dimensional cross-section.

The polysilicon model parameters were extracted from Armstrong et al.[46] and barrier and bulk doping were adjusted to match fabricated devices. Impact ionization was enabled but played a small role, as the supply/drain voltages were comparatively low. For SGTs, an ohmic drain contact (n^{++} semiconductor) was considered and a Schottky contact barrier was introduced, with both Schottky effect ($E^{0.5}$) and αE barrier lowering, where $\alpha = 3$ nm, typical of silicon. Identical FETs were created by replacing the source barrier with an ohmic contact.

Mixed-mode simulation with Silvaco Atlas used the devices (SGT and FET) connected in standard complementary inverter configuration. For d.c. simulations, only one inverter was used. To illustrate transient effects, two identical inverters were cascaded and the output of the first one was evaluated while driving the other one, as a typical load.

The mixed-mode simulation was performed in d.c. by incrementing the input voltage and recording the output voltage and current through the device. For SGT circuit simulation, the characteristic was split into three regions, with the first and last corresponding roughly to the regions where the output logic level is unambiguous. The middle section which represents the transition of the output from one logic level to the other was simulated separately with much smaller input voltage steps (in some cases 0.5 μV). This was necessary as a necessity for capturing the extremely high gain of the SGT inverter and as a consequence of convergence problems despite the use of auto-halving of the input voltage change (trap method) in this version of the simulator.

Due to differences in hole and electron mobilities, the width of the *p-type* FET device (W_P) was 3 times that of the *n-type* transistor (W_N). For SGTs, this mobility mismatch is irrelevant compared to the current densities across the respective source contacts. The barrier height and source current density can be tuned by barrier implants or choice of contact metal, in order keep the tripping voltage of the inverter in the middle of the supply voltage range in the simulation setup we used $W_P = W_N$ and chose the barrier design barrier heights for the *p* and *n* transistors as 0.36 eV and 0.4 eV, respectively.

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Author contributions

R.A.S. conceived the study, performed the measurements, simulation and data processing. J.M.S. and N.D.Y. designed the polysilicon devices. M.J.T. fabricated the polysilicon devices. R.A.S., J.M.S. and S.R.P.S. analyzed and interpreted the results and wrote the paper. All authors reviewed the manuscript.

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