www.nature.com/scientificreports

SCIENTIFIC REPORTS

OPEN

Low-voltage, High-performance Organic Field-Effect Transistors Based on 2D Crystalline Molecular Semiconductors

Received: 19 May 2017
Accepted: 10 July 2017
Published online: 10 August 2017

Qijing Wang, Sai Jiang, Jun Qian, Lei Song, Lei Zhang, Yujia Zhang, Yuhan Zhang, Yu Wang, Xinran Wang, Yi Shi, Youdou Zheng & Yun Li

Two dimensional (2D) molecular crystals have attracted considerable attention because of their promising potential in electrical device applications, such as high-performance field-effect transistors (FETs). However, such devices demand high voltages, thereby considerably increasing power consumption. This study demonstrates the fabrication of organic FETs based on 2D crystalline films as semiconducting channels. The application of high-κ oxide dielectrics allows the transistors run under a low operating voltage (−4 V). The devices exhibited a high electrical performance with a carrier mobility up to 9.8 cm^{2}V^{-1} s^{-1}. Further results show that the AlO_x layer is beneficial to the charge transport at the conducting channels of FETs. Thus, the device strategy presented in this work is favorable for 2D molecular crystal-based transistors that can operate under low voltages.

Two-dimensional (2D) molecular crystals assembled through weak van der Waals forces are a promising class of materials for molecular packing and charge transport and exhibit significant potential for electronic applications[1–7]. Efforts have been devoted to the fabrications of organic field-effect transistors (OFETs) and p-n junctions that use ultrathin crystalline films grown on 2D atomic crystals, such as graphene, boron nitride, and MoS_2. Recently, deposition of 2D molecular crystals on amorphous silicon oxide (SiO_2) has been performed successfully through solution-based processes, which is compatible with current semiconductor manufacturing[8–17]. These OFETs also yielded high carrier mobility that are comparable to polycrystalline silicon. However, a high voltage (i.e., normally over 30 V) is necessary to operate such devices, which results in extra power consumption, because of the low dielectric constant of SiO_2. Therefore, lowering the operating voltage is greatly important, particularly for portable and wearable electronics. An effective approach is to employ high-κ materials for the dielectric layers in transistor architectures, such that a low voltage can generate an adequate charge density in the conducting channel[18–21]. Therefore, producing low-operating-voltage and high-performance OFETs based on 2D molecular crystals using high-κ oxides as the dielectric layer, is noteworthy.

Herein, we demonstrate a low-voltage bottom-gate top-contact (BGTC) OFET that utilizes 2D molecular crystals as the conducting channel and AlO_x as the dielectric. The molecular crystals were solution-processed through a floating-coffee-ring-driven assembly according to the methods presented in our previous work[17]. Our devices can operate at a low gate bias of −4 V and exhibit a high carrier mobility (μ_{FET}) up to 9.8 cm^2 V^{-1} s^{-1}, a large on/off ratio of 10^5, and a small subthreshold swing of 160 mV dec^{-1}. The results demonstrate that the proposed strategy has significant potential in fabricating low-voltage and high-performance OFETs employing high-κ dielectrics and 2D molecular crystals.

Results

The p-type small-molecule semiconductor of dioctylbenzothienobenzothiophene (C_8-BTBT) exhibits a considerably high carrier mobility and thus has been used to fabricate the OFETs[22–24]. The highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) of C_8-BTBT are −5.39 eV and −1.55 eV, respectively[25]. Figure 1a illustrates the BGTC structure of the transistor device that adopts thermally deposited AlO_x with a thickness of ~18 nm as the dielectric layer. Figure 1b shows the atomic force microscopy (AFM) image

National Laboratory of Solid-State Microstructures, School of Electronic Science and Engineering, Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, 210093, China. Correspondence and requests for materials should be addressed to Y.L. (email: yli@nju.edu.cn) or Y.S. (email: yshi@nju.edu.cn)

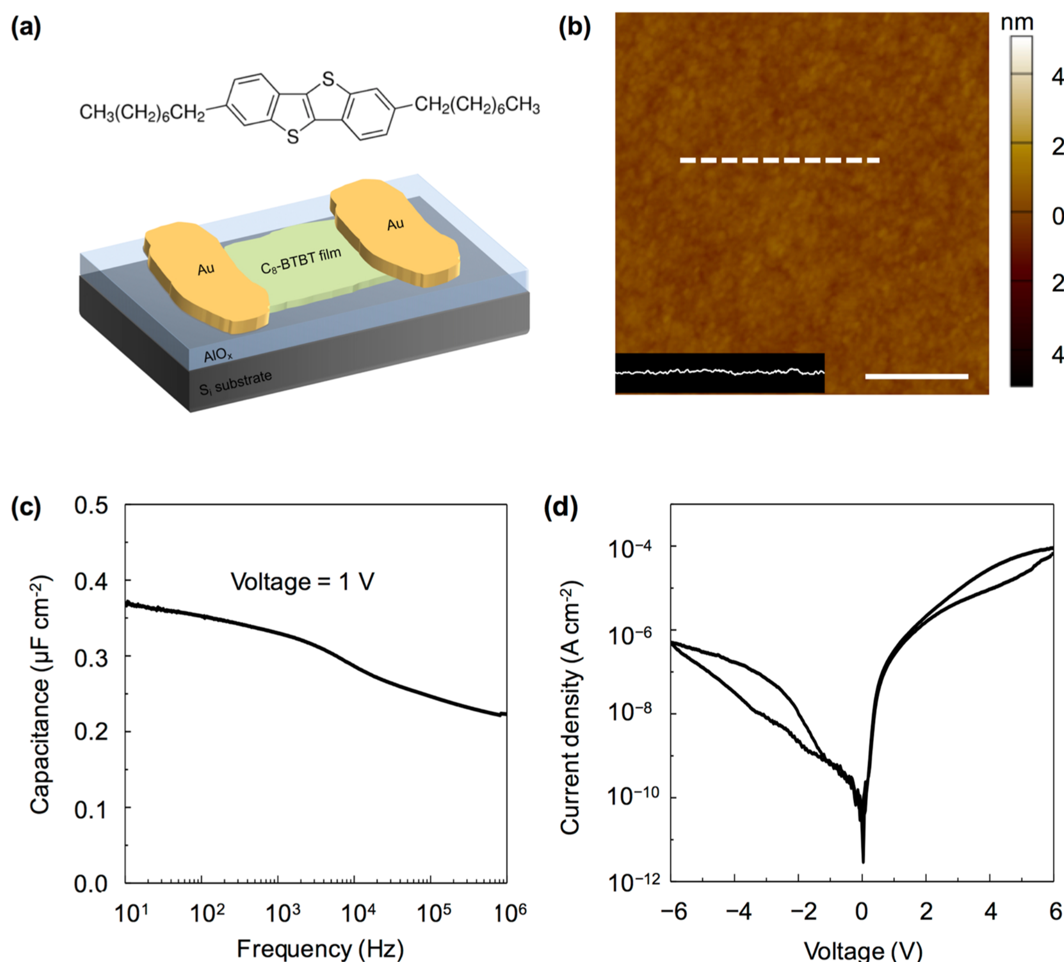

Figure 1. (**a**) Schematic of the BGTC transistor. (**b**) AFM morphology image of the AlO_x dielectric. Scale bar, 500 nm. (**c**) Capacitance per unit versus frequency (at a voltage of 1 V). (**d**) Gate leakage current versus voltage.

of the AlO_x dielectric, which illustrates a particularly smooth surface with a root-mean-square (RMS) roughness of 2.23 Å. The hydrophilicity of the AlO_x dielectric layer is enhanced through UV–ozone treatment. Improving the hydrophilicity is conducive to the subsequent solution-based process for molecular crystal growth. Besides, the surface roughness of UV-ozone-treated AlO_x is 2.75 Å (Supplementary Fig. S1). Given that the capacitance and gate leakage current are both critical to the gate dielectric in low-voltage OFETs, we employ an Au/AlO_x/Si capacitor structure. The measured capacitance and dielectric constant are 0.37 μF/cm^2 and ~9.0, respectively (measured at the voltage frequency of 10 Hz, Fig. 1c). Moreover, the AlO_x capacitance decreases from 0.37 μF/cm^2 to 0.25 μF/cm^2 when the frequency of the applied voltage increases from 10 Hz to 1 MHz. This effect is mainly due to the interfacial traps produced during the UV–ozone treatment. The dielectric capacitance of AlO_x exhibits negligible change when the applied voltage increases from −6 V to 6 V (Supplementary Fig. S2), and its leakage current is 10^{-7} A/cm^2 when the applied voltage is −4 V (Fig. 1d). Therefore, the thermally deposited AlO_x can be used as a gate insulating layer because of its superior performance as a dielectric material. The coffee-ring-driven method (Supplementary Fig. S3) is utilized for the deposition of 2D films where C_8-BTBT molecules assemble into 2D crystalline films with a large size of ~200 μm on the AlO_x surface (Fig. 2a)[17]. Supplementary Fig. S4 shows a deposited bilayer C_8-BTBT film with a large size of several millimeters. The obtained molecular films consist of different C_8-BTBT layers with step-and-terrace structures. Figure 2b and c show the AFM images of the two steps as marked by dotted squares in Fig. 2a, where the thicknesses are 2.99 and 5.21 nm, respectively. The molecules in the third layer are nearly perpendicular to the substrates with regard to the C_8-BTBT molecular length. The previous results show that C_8-BTBT molecules in first layer are more tilted to the substrate than that in upper layers, because the weak van der Waals interactions among the small molecules decrease rapidly from the dielectric surface to the upper molecular layers[6,26]. The schematic illustration of C_8-BTBT molecular packing is shown in Supplementary Fig. S5. Furthermore, the bilayer C_8-BTBT exhibits uniform thin films with atomic smoothness (RMS roughness: 1.22 Å, Fig. 2d). The crystalline properties of the bilayer C_8-BTBT are characterized through high-resolution AFM (Fig. 2e). More than 10 points are selected randomly for scanning by high-resolution AFM (Supplementary Fig. S6). The AFM images show nearly identical lattice constants, namely, $a = 6.21 \pm 0.16$ Å, $b = 8.12 \pm 0.12$ Å, and $\theta = 88.1 \pm 1.4°$. These results indicate that the bilayer C_8-BTBT films each contain a crystalline phase with highly morphologic uniformity over a large area. Similar crystalline characteristics are also

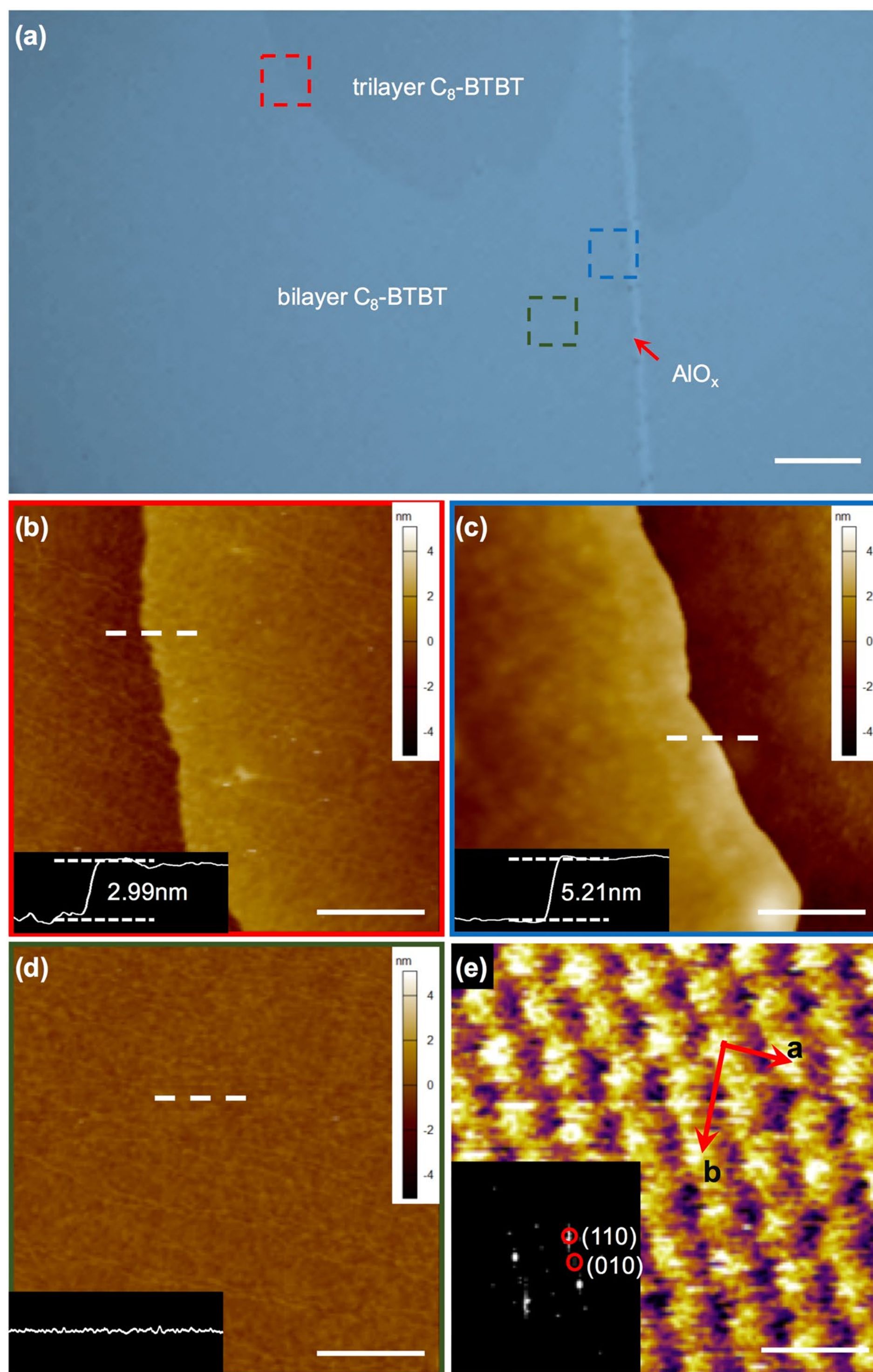

Figure 2. (**a**) Optical microscopy image of the 2D C_8-BTBT crystalline films. The bilayer and trilayer are clearly observed. Scale bar, 20 µm. (**b**) AFM morphology image of the step between bilayer and trilayer films (red square in (**a**)). Scale bar, 500 nm. (**c**) AFM morphology image of the step between bilayer films and the substrate (blue square in (**a**)). Scale bar, 500 nm. (**d**) AFM morphology image of uniform bilayer films (brown square in (**a**)). Scale bar, 500 nm. (**e**) High-resolution AFM image of the bilayer C_8-BTBT molecules on the AlO_x/Si substrate. Scale bar, 1 nm. The inset shows the corresponding fast Fourier transforms of the AFM image with lattice indices.

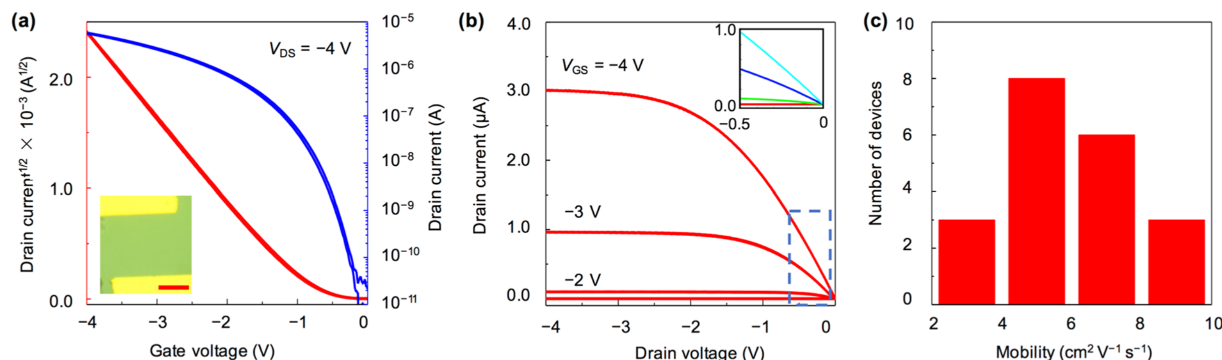

Figure 3. (**a**) Transfer characteristics at a drain voltage of −4 V. The inset shows the optical microscope image of the measured device. Scale bar, 20 μm. (**b**) Output characteristics at different gate voltages. Inset shows a linear increase in the drain currents in a small range of the drain voltage, indicating a nearly ideal ohmic contact in our devices. (**c**) Mobility distribution from 20 devices.

observed in the C_8-BTBT trilayer (Supplementary Fig. S7). The crystalline properties of our molecular crystals are summarized in Supplementary Table S1. Therefore, the AlO_x layer formed through thermal evaporation facilitates the deposition of high-quality 2D C_8-BTBT crystalline films.

Discussion

The bilayer crystalline films and AlO_x are used as conducting channels and gate dielectrics, respectively, to fabricate the planar transistors. Figure 3a and b show the typical transfer and output characteristics of a bilayer C_8-BTBT-based FET, respectively. These properties indicate that a low operating voltage (−4 V) is sufficient to operate the device properly with an evident field effect. The drain current in the output curves reaches the saturation region even at a drain voltage of −4 V. A nearly linear increase in the drain current is also observed in the small range of the drain voltage, indicating a nearly ohmic contact with an efficient charge injection from the metal contact to the conducting channel (inset of Fig. 3b). Moreover, the device exhibits a high electrical performance and yields a carrier mobility of up to 6.5 cm^2 V^{-1} s^{-1}, near-zero threshold voltage of −0.7 V, small subthreshold swing of 160 mV dec^{-1}, and large on/off ratio of >10^5. The carrier mobility value was calculated in the saturation region using the equation:

$$I_D = \left(\frac{WC_i}{2L}\right)\mu_{\mathrm{FET}}(V_G - V_T)^2 \tag{1}$$

where W and L are the channel width and length, respectively, C_i is the gate dielectric capacitance, V_T is the threshold voltage. Besides, 2D crystalline films with only several layers can greatly enhance the charge injection process by significantly decreasing the access resistance related to the charge injection from the metal/semiconductor interface to the active channel[27,28]. And the width-normalized contact resistance in our device is estimated to be ~360 Ω cm by using the Y-function method; the value is among the lowest ones for the contact resistance of organic transistors (Supplementary Figs S8 and S9). For comparison, we also fabricated BGTC FETs based on a five-molecular-layer C_8-BTBT crystal. The threshold voltage and mobility are −2.7 V and 0.98 cm^2 V^{-1} s^{-1}, respectively (Supplementary Fig. S10). Besides, the width-normalized contact resistance is 7600 Ω cm, which is much larger than that in FETs based on bilayer crystal (Supplementary Fig. S11). We observed a negligible hysteresis from the transfer curve as the applied gate voltage sweeps backwards. We also prepared 20 devices with AlO_x dielectrics, obtaining an average mobility of 4.7 ± 1.9 cm^2 V^{-1} s^{-1} (Fig. 3c). Furthermore, the highest mobility obtained is 9.8 cm^2 V^{-1} s^{-1} (Supplementary Fig. S12). To the best of our knowledge, our device exhibits a record-high value of the carrier mobility for low-voltage OFETs (Supplementary Table S2). Typical OFETs based on C_8-BTBT reported in literature are summarized in Supplementary Table S3.

Apart from low-voltage operation and high performance, suitable bias-stress stability is also significant for practical applications. Figure 4a shows the bias-stress characteristics of a bilayer C_8-BTBT-based FET. Even when tested in the ambient condition, the drain current of the device shows nearly negligible change under a prolonged operation of 10^4 s. Apart from the high-quality bilayer C_8-BTBT crystalline films, low-voltage operation generates limited heat during the electrical measurements, hence also contributes to the stability of our transistor device. Figure 4b shows that the shapes of the transfer curves before and after the bias-stress test exhibit a small shift to a more negative gate voltage. There is a negligible change in the threshold voltage during the test (~0.1 V) (Supplementary Fig. S13). The estimated carrier mobility slightly decreases from 6.3 cm^2 V^{-1} s^{-1} to 5.7 cm^2 V^{-1} s^{-1}. We also evaluated the stability by testing a device maintained in ambient condition for up to 30 days. Figure 4c shows that both the drain current and carrier mobility only decrease slightly.

Consequently, the presented results prove the promising features of thermally evaporated AlO_x as a gate dielectric for low-voltage OFETs with bilayer molecular crystals as conducting channels. For comparison, we prepared the FET samples that utilized SiO_2 and HfO_2 (Fig. 5). A large operating voltage of −20 V is necessary to operate the SiO_2-based device, and the estimated carrier mobility is 4.8 ± 2.1 cm^2 V^{-1} s^{-1}. The operating voltage can be properly lowered to −4 V, whereas the carrier mobility can be as low as 0.4 ± 0.3 cm^2 V^{-1} s^{-1} when

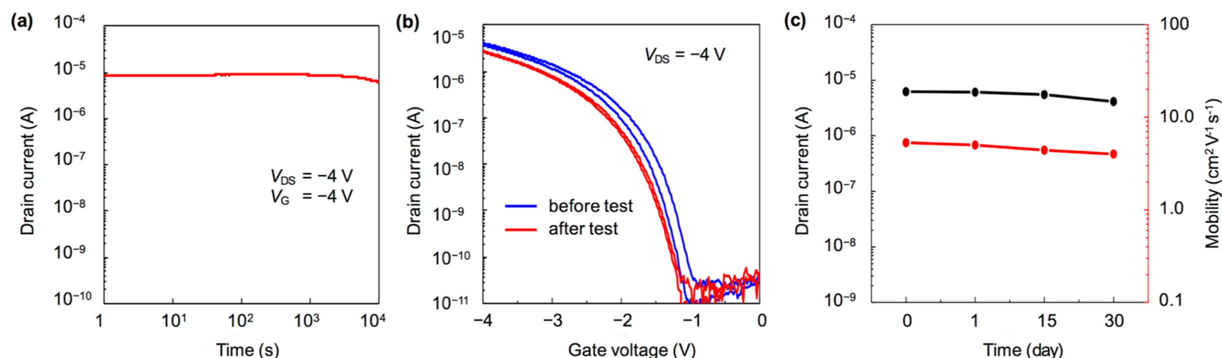

Figure 4. (**a**) Bias-stress characteristics of a C_8-BTBT-based OFET. Bias-stress measurements were conducted in the ambient condition. The drain and gate voltages were both −4 V. (**b**) Transfer curves before and after the bias-stress test. (**c**) Stability characteristics of the C_8-BTBT-based OFET.

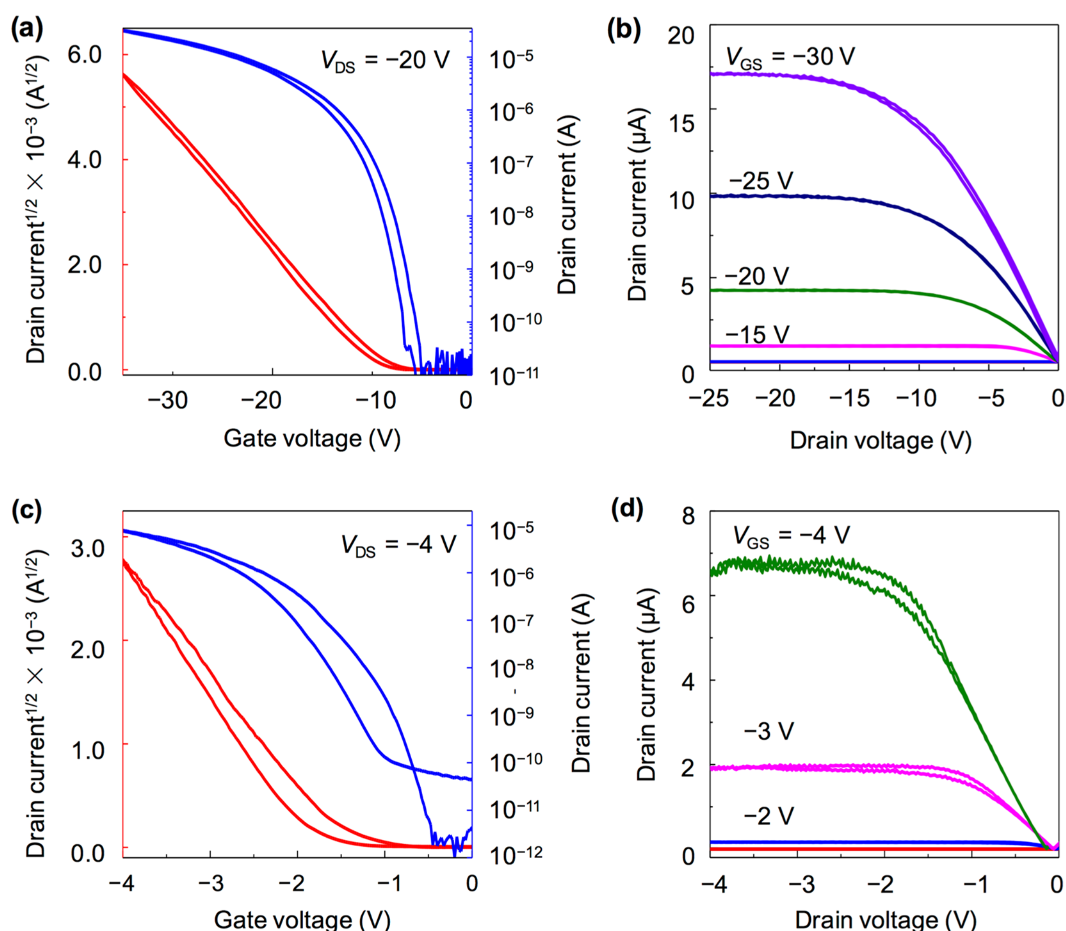

Figure 5. Electrical characteristics of the C_8-BTBT-based OFETs on SiO_2/Si and HfO_2/Si. (**a**) Transfer characteristics at a drain voltage of −20 V. (**b**) Output characteristics at different gate voltages of a device using SiO_2. (**c**) Transfer characteristics at a drain voltage of −4 V. (**d**) Output characteristics at different gate voltages of a device using HfO_2.

applying HfO_2 as the gate insulator. The decreased mobility in the device with HfO_2 is mainly due to the strong interaction at the interface between the conducting channel and high-κ dielectric[29, 30]. This interaction results in the increased localization of the charge carriers[6, 31, 32], which is consistent with the result that OFETs based SiO_2 exhibit a higher carrier mobility than that based on AlO_x. Further studies on the charge carrier properties in our ultrathin molecular crystals is of great interest. Thus, to develop a technique that allows for the fabrication of 2D-crystalline-film-based transistors that employ vacuum as the dielectric layer is necessary[29].

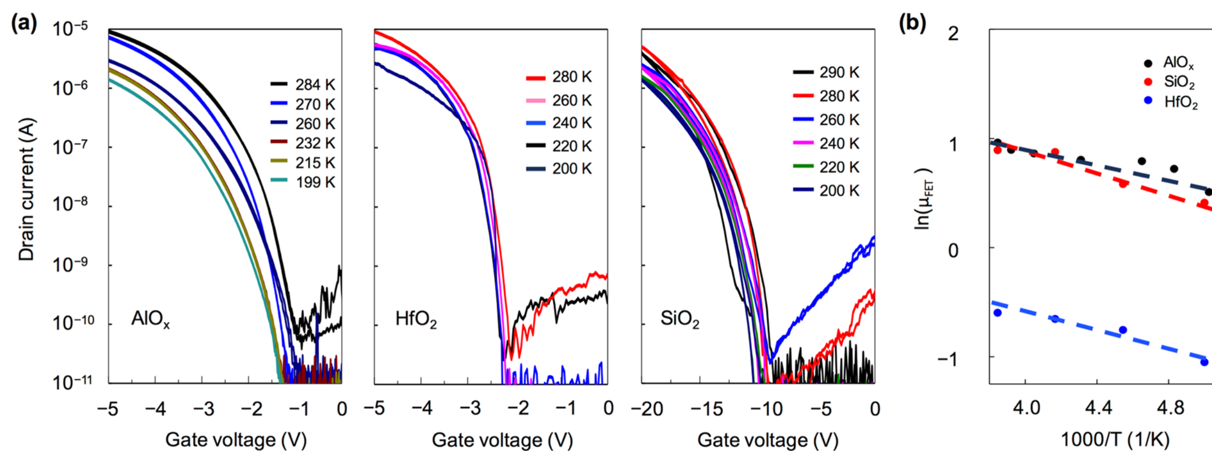

Figure 6. (**a**) Transfer curves of the C_8-BTBT-based OFETs using AlO_x, HfO_2 and SiO_2 under different temperatures. (**b**) Temperature dependence of the field-effect mobility.

Dielectric	μ_{FET} ($cm^2V^{-1}s^{-1}$)	On/Off	*SS* (mV dec^{-1})	V_T (V)	Maximum Trap Density ($\times 10^{12}$ cm^{-2})	E_a (meV)	μ_0 (cm^2 V^{-1} s^{-1})
AlO_x	4.7 ± 1.9	10^5	160	−0.7	3.9	30.8	12
HfO_2	0.4 ± 0.3	10^5	155	−1.5	4.1	36.5	4
SiO_2	4.8 ± 2.1	10^5	460	−9.0	2.3	39.6	16

Table 1. Electrical performances, including μ_{FET} (field-effect mobility), on/off ratio, *SS* (subthreshold swing), V_T (threshold voltage), maximum trap density, E_a (activation energy), and μ_0 (the trap-free mobility), of the OFETs with different dielectrics.

Note that AlO_x also has a high dielectric constant, whereas the obtained carrier mobility is similar to that of the device with SiO_2, and much higher than those of the HfO_2-based devices. The maximum density of interfacial traps (N_{trap}) is estimated from the values of the subthreshold swing (*SS*) to examine the performance, especially the carrier mobility, exhibited in the device that uses AlO_x:

$$N_{Trap}^{max} = \left(\frac{qSSlog(e)}{kT} - 1\right)\frac{C_i}{q} \tag{2}$$

where q is the electronic charge, *SS* is the subthreshold swing, *e* is Euler's number, *k* is the Boltzmann's constant, *T* is the absolute temperature, and C_i is the gate dielectric capacitance. The trap density of AlO_x is ~3.9×10^{12} cm^{-2}, which is in the same range as those of SiO_2 and HfO_2. The intrinsic charge transport behavior is determined by performing the temperature-dependent measurement on the electrical performance of the FETs with different oxide dielectrics (Fig. 6a). The carrier mobilities calculated from the transfer curves can all be fitted to linear lines in the plots of $\ln(\mu_{FET})$ versus $1/T$ (Fig. 6b), which indicates that the hopping transport dominates in all devices. Furthermore, the activation energy (E_a) can be estimated through the Arrhenius equation:

$$\mu_{FET} = \mu_0 exp(-E_a/kT) \tag{3}$$

where μ_0 is the trap-free mobility. Temperature-dependent measurements for the devices with different dielectric layers are summarized in Table 1. The device that utilizes AlO_x exhibits the lowest E_a value of 30.8 meV and a high μ_0 of 12 $cm^2 V^{-1} s^{-1}$. And E_a is considered to be related to the width of the distribution of trap states[33–35]. Therefore, the high carrier mobility obtained in the AlO_x-based device is attributed to a low energetic disorder, a narrow width for the density of trap states in the dielectric interface, and a close packing among the C_8-BTBT molecules[36–38]. The results reveal that AlO_x can provide a beneficial interface for the transport of charge carriers. Besides, despite a good structural quality of our bilayer C_8-BTBT crystals and high electrical performance obtained from the AlO_x-based transistors, the charge transport exhibits as a hopping-like rather than a band-like behavior. Similar results were also reported in literature, which imply that the property of the dielectric layer can affect the charge transport in the conducting channel[29, 38–41]. Besides, our recent results also reveal that the charge transport behavior can be greatly influenced by the contact resistance[42–44].

In conclusion, we fabricated low-voltage and high-performance OFETs that employ solution-processed bilayer molecular crystals and high-κ material of AlO_x as the conducting channels and the gate dielectrics, respectively. The devices can operate under a low applied voltage of −4 V and exhibit excellent electrical performance with the highest carrier mobility of up to 9.8 $cm^2 V^{-1} s^{-1}$. Moreover, further studies indicated that the AlO_x application in FET devices is favorable to the interfaces among the 2D molecular crystals, in which the charge carrier transport has small activation energy. The results demonstrated the advantages of the proposed strategy to attain low-voltage and high-performance OFETs.

Methods

Fabrication of the AlO_x layer: The Si substrate was sequentially cleaned by sonication in acetone and isopropanol for 10 min each. The oxide dielectric of AlO_x with a thickness of ~18 nm was thermally evaporated under a deposition speed of 0.1 Å s^{-1} with a base pressure of 10^{-5} Torr. The AlO_x was then treated by UV-ozone for 15 min.

Deposition of the 2D C_8-BTBT Crystals: The p-type organic semiconductor C_8-BTBT was supplied by Nippon Kayaku Co. and was adopted without further purification. C_8-BTBT (1.0 wt%) was dissolved in a mixture of anisole and *p*-anisaldehyde (0.5 wt%) which were the good solvent and the antisolvent, respectively. The UV-ozone-treated AlO_x was sequentially cleaned in acetone and isopropanol. Before the droplet was casted onto the AlO_x substrate, the solution was shaken for ~30 s to deposit from a homogeneous solution. A mechanical pump was then employed to vent the air through a pipe positioned ~1 mm from the droplet (Supplementary Fig. S3).

Characterizations of the C_8-BTBT Crystals: An Olympus BX51 was used to obtain the optical microscopy images. Two AFM types were performed in this work. The characterizations were performed on a Veeco Multimode 8 under the ambient conditions for the regular AFM. The experiments were then performed on an Asylum Cypher under ambient conditions utilizing Asylum ARROW UHF AFM tips for the high-resolution AFM.

Fabrication and Electrical Measurements of FETs: Few-layered C_8-BTBT was deposited onto the AlO_x substrates for the OFET fabrication, as shown in Fig. 1. Patterned Au films with a thickness of 100 nm and Au pads with dimensions of 30 μm × 100 μm were thermally evaporated under a deposition speed of 0.2 Å s^{-1}. The two Au pads were subsequently transferred to the top of the C_8-BTBT crystal to form the source and drain electrodes (Supplementary Fig. S14). Electrical measurements were performed utilizing an Agilent B1500 semiconductor parameter analyzer in a closed-cycle cryogenic probe station with a base pressure of 10^{-5} Torr.

References

1. Cai, S.-L. *et al*. The Organic Flatland-Recent Advances in Synthetic 2D Organic Layers. *Adv. Mater.* **27**, 5762–5770 (2015).
2. Huang, J., Sun, J. & Katz, H. E. Monolayer-Dimensional 5,5′-Bis(4-hexylphenyl)-2,2′-bithiophene Transistors and Chemically Responsive Heterostructures. *Adv. Mater.* **20**, 2567–2572 (2008).
3. Wu, B. *et al*. Precise, Self-Limited Epitaxy of Ultrathin Organic Semiconductors and Heterojunctions Tailored by van der Waals Interactions. *Nano Lett.* **16**, 3754–3759 (2016).
4. Mannebach, E. M. *et al*. High Hole Mobility and Thickness-Dependent Crystal Structure in α,ω-Dihexylsexithiophene Single-Monolayer Field-Effect Transistors. *Adv. Funct. Mater.* **23**, 554–564 (2012).
5. Park, B.-N., Seo, S. & Evans, P. G. Channel formation in single-monolayer pentacene thin film transistors. *J. Phys. D: Appl. Phys.* **40**, 3506–3511 (2007).
6. Zhang, Y. *et al*. Probing Carrier Transport and Structure-Property Relationship of Highly Ordered Organic Semiconductors at the Two-Dimensional Limit. *Phys. Rev. Lett.* **116**, 016602–6 (2016).
7. Asadi, K., Wu, Y., Gholamrezaie, F., Rudolf, P. & Blom, P. W. M. Single-Layer Pentacene Field-Effect Transistors Using Electrodes Modified With Self-assembled Monolayers. *Adv. Mater.* **21**, 4109–4114 (2009).
8. Chen, H. *et al*. Solution-Processable, Low-Voltage, and High-Performance Monolayer Field-Effect Transistors with Aqueous Stability and High Sensitivity. *Adv. Mater.* **27**, 2113–2120 (2015).
9. Solution-Processable Septithiophene Monolayer Transistor. 1–6, doi:10.1002/adma201103522 (2012).
10. Hutchins, D. O. *et al*. Spin cast self-assembled monolayer field effect transistors. *Organic Electronics* **13**, 464–468 (2012).
11. Shan, L. *et al*. Monolayer Field-Effect Transistors of Nonplanar Organic Semiconductors with Brickwork Arrangement. *Adv. Mater.* **27**, 3418–3423 (2015).
12. Wang, B. *et al*. Addressable growth of oriented organic semiconductor ultra-thin films on hydrophobic surface by direct dip-coating. *Organic Electronics* **24**, 170–175 (2015).
13. Li, L. *et al*. Controllable Growth and Field-Effect Property of Monolayer to Multilayer Microstripes of an Organic Semiconductor. *J. Am. Chem. Soc.* **132**, 8807–8809 (2010).
14. Jiang, L. *et al*. Millimeter-Sized Molecular Monolayer Two-Dimensional Crystals. *Adv. Mater.* **23**, 2059–2063 (2011).
15. Mottaghi, M. *et al*. Low-Operating-Voltage Organic Transistors Made of Bifunctional Self-Assembled Monolayers. *Adv. Funct. Mater.* **17**, 597–604 (2007).
16. Ringk, A. *et al*. n-Type self-assembled monolayer field-effect transistors for flexible organic electronics. *Organic Electronics* **14**, 1297–1304 (2013).
17. Wang, Q. *et al*. 2D Single-Crystalline Molecular Semiconductors with Precise Layer Definition Achieved by Floating-Coffee-Ring-Driven Assembly. *Adv. Funct. Mater.* **26**, 3191–3198 (2016).
18. Klauk, H., Zschieschang, U., Pflaum, J. & Halik, M. Ultralow-power organic complementary circuits. *Nature* **445**, 745–748 (2007).
19. Kaltenbrunner, M. *et al*. An ultra-lightweight design for imperceptible plastic electronics. *Nature Publishing Group* **499**, 458–463 (2013).
20. Majewski, L. A., Schroeder, R. & Grell, M. Low-Voltage, High-Performance Organic Field-Effect Transistors with an Ultra-Thin TiO2 Layer as Gate Insulator. *Adv. Funct. Mater.* **15**, 1017–1022 (2005).
21. Tiwari, S. P., Zhang, X.-H., Potscavage, W. J. Jr. & Kippelen, B. Low-voltage solution-processed n-channel organic field-effect transistors with high-k HfO2 gate dielectrics grown by atomic layer deposition. *Appl. Phys. Lett.* **95**, 223303–4 (2009).
22. Yuan, Y. *et al*. Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method. *Nature Communications* **5**, 1–9 (2014).
23. Minemawari, H. *et al*. Inkjet printing of single-crystal films. *Nature Publishing Group* **475**, 364–367 (2011).
24. Ebata, H. *et al*. Highly Soluble [1]Benzothieno[3,2- b]benzothiophene (BTBT) Derivatives for High-Performance, Solution-Processed Organic Field-Effect Transistors. *J. Am. Chem. Soc.* **129**, 15732–15733 (2007).
25. Kobayashi, H. *et al*. Hopping and band mobilities of pentacene, rubrene, and 2,7-dioctyl[1]benzothieno[3,2- b][1]benzothiophene (C 8-BTBT) from first principle calculations. *The Journal of Chemical Physics* **139**, 014707–8 (2013).
26. He, D. *et al*. Two-dimensional quasi-freestanding molecular crystals for high-performance organic field-effect transistors. *Nature Communications* **5**, 1–7 (2017).
27. Wang, S. D., Yan, Y. & Tsukagoshi, K. Understanding contact behavior in organic thin film transistors. *Appl. Phys. Lett.* **97**, 063307–3 (2010).
28. Minari, T., Miyadera, T., Tsukagoshi, K., Aoyagi, Y. & Ito, H. Charge injection process in organic field-effect transistors. *Appl. Phys. Lett.* **91**, 053508–3 (2007).
29. Hulea, I. N. *et al*. Tunable Fröhlich polarons in organic single-crystal transistors. *Nat Mater* **5**, 982–986 (2006).
30. Acton, B. O. *et al*. Dielectric Surface-Controlled Low-Voltage Organic Transistors via n-Alkyl Phosphonic Acid Self-Assembled Monolayers on High- kMetal Oxide. *ACS Appl. Mater. Interfaces* **2**, 511–520 (2010).

31. Liu, Q. *et al*. Low-voltage organic field-effect transistors based on novel high- κorganometallic lanthanide complex for gate insulating materials. *AIP Advances* **4**, 087140–6 (2014).
32. Su, Y. R. *et al*. A low-temperature, solution-processed high- kdielectric for low-voltage, high-performance organic field-effect transistors (OFETs). *J. Phys. D: Appl. Phys.* **46**, 095105–9 (2013).
33. Kim, S. H., Jang, M., Yang, H., Anthony, J. E. & Park, C. E. Physicochemically Stable Polymer-Coupled Oxide Dielectrics for Multipurpose Organic Electronic Applications. *Adv. Funct. Mater.* **21**, 2198–2207 (2011).
34. Jung, S., Ji, T. & Varadan, V. K. Temperature sensor using thermal transport properties in the subthreshold regime of an organic thin film transistor. *Appl. Phys. Lett.* **90**, 062105–3 (2007).
35. Knipp, D., Street, R. A., V lkel, A. & Ho, J. Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport. *Journal of Applied Physics* **93**, 347–355 (2003).
36. Pivrikas, A., Ullah, M., Sitter, H. & Sariciftci, N. S. Electric field dependent activation energy of electron transport in fullerene diodes and field effect transistors: Gill's law. *Appl. Phys. Lett.* **98**, 092114–4 (2011).
37. Kronemeijer, A. J. *et al*. Two-Dimensional Carrier Distribution in Top-Gate Polymer Field-Effect Transistors: Correlation between Width of Density of Localized States and Urbach Energy. *Adv. Mater.* **26**, 728–733 (2013).
38. Xie, W. *et al*. Temperature-Independent Transport in High-Mobility Dinaphtho-Thieno-Thiophene (DNTT) Single Crystal Transistors. *Adv. Mater.* **25**, 3478–3484 (2013).
39. Konezny, S. J., Bussac, M. N. & Zuppiroli, L. Hopping and trapping mechanisms in organic field-effect transistors. *Phys. Rev. B* **81**, 045313–12 (2010).
40. Hamaguchi, A. *et al*. Single-Crystal-Like Organic Thin-Film Transistors Fabricated from Dinaphtho[2,3- b:2′,3′- f]thieno[3,2- b]thiophene (DNTT) Precursor-Polystyrene Blends. *Adv. Mater.* **27**, 6606–6611 (2015).
41. Darmawan, P. *et al*. Optimal Structure for High-Performance and Low-Contact-Resistance Organic Field-Effect Transistors Using Contact-Doped Coplanar and Pseudo-Staggered Device Architectures. *Adv. Funct. Mater.* **22**, 4577–4583 (2012).
42. Xu, Y. *et al*. Joule's law for organic transistors exploration: Case of contact resistance. *Journal of Applied Physics* **113**, 064507–6 (2013).
43. Xu, Y. *et al*. Contacts between Two- and Three-Dimensional Materials: Ohmic, Schottky, and p– nHeterojunctions. *ACS Nano* **10**, 4895–4919 (2016).
44. Liu, C., Xu, Y., Li, Y., Scheideler, W. & Minari, T. Critical Impact of Gate Dielectric Interfaces on the Contact Resistance of High-Performance Organic Field-Effect Transistors. *J. Phys. Chem. C* **117**, 12337–12345 (2013).

Acknowledgements

This study was supported partially by 973 projects under Grant No. 2013CBA01600 and 2013CB932900, NSFC under Grant No. 61574074, NSFJS under Grant No. BK20170075, and Open Partnership Joint Projects of NSFC-JSPS Bilateral Joint Research Projects under Grant No. 61511140098.

Author Contributions

Q.J.W., Y.L., and Y.S. conceived and designed the experiments; Q.J.W., S.J., J.Q., Y.W., and L.Z. carried out the experiments; L.S., Y.J.Z., and Y.H.Z. performed the AFM characterizations; Y.Li and Q. Wang wrote the manuscript text and prepared the figures. X.R.W. and Y.D.Z. joined the discussion on the results and reviewed the manuscript.

Additional Information

Supplementary information accompanies this paper at doi:10.1038/s41598-017-08280-8

Competing Interests: The authors declare that they have no competing interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2017