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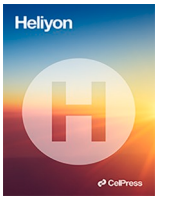

Research article

Design and numerical analysis of high contrast ratio and ultra-compact all-optical 2-bit reversible comparator

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ABSTRACT

In this paper, a novel interference-based nanostructure was designed and simulated to realize an all-optical 2-bit reversible comparator by employing a novel technique. The plane wave expansion (PWE) method was adopted to analyze the encoder design and frequency modes. Aside from downsizing, the finite-difference time-domain (FDTD) method was utilized for the simulation and numerical analysis of the design proposed herein. An ultra-compact nanostructure with a 129.8 μm^2 footprint was utilized for the all-optical 2-bit reversible comparator. One of the noteworthy characteristics of the proposed nanostructure was its excellent contrast ratio (i.e., 13.8 dB) in comparison to other nanostructures. The bitrate and delay time in this nanostructure were 3.33 Tb/s and 300 fs, respectively. Based on the findings of the simulations conducted at a central wavelength of 1.55 μm, it is recommended to employ the nanostructure proposed herein during the third telecom window. A photonic crystal nano-resonator was utilized to design the high-performance all-optical 2-bit reversible comparator, which may also be employed in integrated optical circuits (IOCs).

1. Introduction

All-optical logic gates are used in all-optical processors, optical signal processing systems, and all-optical networks, contributing significantly to these systems' operational efficiency [1–4]. All component design, modeling, and manufacturing have advanced significantly in the last several years. Photonic crystal structures are all-optical structures where the refractive index changes regularly along various directions and is generated periodically, typically in a semiconductor material [5–9]. When radiation with a frequency inside the PBG enters the structure, it is fully reflected; in other words, the PBG is the energy or frequency range within which light propagation within the PhC is restricted. The current fascination has been generated in the theoretical modeling and fabrication of all optical components using photonic crystal (PhC) as the material due to its unique properties. These components provide numerous benefits, including their small size and low power consumption [7–14]. Several pertinent discoveries in photonic crystals have been published in recent years. These consist of all-optical filters [8–11], splitters/couplers [15], logic gates [16–21], adders [22,23], optical switches [24,25], demultiplexer [26], BCD to gray converter [27], reversible logic gates [28,29], analog-to-digital converter [30–32], encoders [33–37], multifunctional logic gates [38–43], optical memory components [44], and sensors [45–47]. The maximum obtained contrast ratio (CR) is 22.06 dB approximately with the high bit rate of 7.14 Tb/s and a fast response time (RT) of about 0.14 ps for the XOR logic gate compared to all the other logic gates characterized by a single-design structure [48].

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Due to its novel uses, all-optical single-bit comparators have recently drawn much interest from researchers. In developing all-optical 1-bit comparators, extremely appropriate structures have been mentioned [49–60].

A 1-bit comparator employing an 86 × 49 photonic crystal structure relying on a silicon-in-air dielectric rod and the Kerr effect was reported by Fakouri-Farid and Andalib [49]. The supplied nonlinear 1-bit comparator structure has a footprint of 1705 μm, a delay time of about 6 ps, and a claimed contrast of around 10.5 dB [50]. Zhu et al. released a nonlinear photonic crystal structure, which continues the design of 1-bit comparator structures [51]. The delay time of the structure is stated to be 4 ps, and it is about 2 ps less than the earlier work described. The contrast ratio of both structures is in the same range, at around 10 dB, even though this structure is quicker than the earlier one.

Surendar et al. reported an all-optical single-bit comparator with a delay time of 1 ps and a footprint of approximately 702 μm^2, continuing the improvement of the single-bit comparator [52]. This was a satisfactory success for these structures regarding miniaturization and speed. Perandin et al. created an ultra-compact construction with an air bed including dielectric rods, measuring 1555 μm^2 and 5.8 dB contrast ratio, in one of the most recent publications on single-bit comparator structures [54]. The suggested single-bit comparator structures used three light source inputs in all of the previously discussed single-bit comparator structures. An all-optical single-bit comparator that relies on just two optical sources decreases the use of optical sources by 33 %, according to research by Serajmohammadi et al. Creating an ultra-compact structure with a footprint of 55 μm^2 was a noteworthy aspect of this construction. This structure's meager contrast ratio (5.2 dB) was negative.

As previously indicated, using three light sources and the decrease, in contrast, ratio when two light sources are utilized, are the drawbacks of earlier 1-bit photonic crystal comparator architectures. Furthermore, reports of 2-bit photonic crystal comparators have yet to be made up to this point, and the previously suggested architectures were only useful for a single bit. This article introduces a proposed framework for comparing two binary units and the associated quantity of light sources. The framework can compare a larger number of binary units while only increasing the number of light sources by 33 % and using four input light sources. The task will be completed.

After developing the structure and determining the propagation modes, we apply the PWE technique to solve this problem. In the next section, we will extract the necessary PBG structure based on the acquired radius by examining the PBG regions for various radii. Following creating the photonic crystal two-bit reversible comparator structure, we will use the FDTD numerical solution technique to analyze and assess the structure's performance. Finally, we execute the two-bit reversible comparator function along with other comparable tasks.

2. Designing the structure of a two-bit comparator

To create a 22 × 23 photonic crystal structure with a two-bit comparator structure incorporating silicon rods in air. The dielectric constant of silicon at the wavelength of 1550 nm is approximately 3.47 [30]. Using the PWE technique, the band gap region was determined to limit the wide range of the wavelength spectrum. The structure modes were then determined using the 2DFDTD technique and by transmitting a pulse via the light source. By applying the desired wavelength effect, which is equal to 1550 nm, to the suggested structure, the results of numerical analyses have been acquired for all modes in the following. RSoft Photonics CAD Suite version 2019.03 is used in this paper. When designing photonic crystal structures on silica substrates, the most notable point is the photonic band gap issue. As a result, when extracting the same band gap and designing the same structure, given the fact that the light speed in the silica substrate is lower than that in the air substrate, the considered structure has a very short delay time. The structure dimensions become larger due to its band gap in the silica substrate. As a result, photonic crystal structures in the air will be employed to attain a higher speed with smaller dimensions. The primary reason for the utilization of these structures is their better light conduction in comparison with the structures established on the silica substrate. From another viewpoint, the air cavity photonic crystal structures in silica substrate are characterized by a more appropriate production procedure.

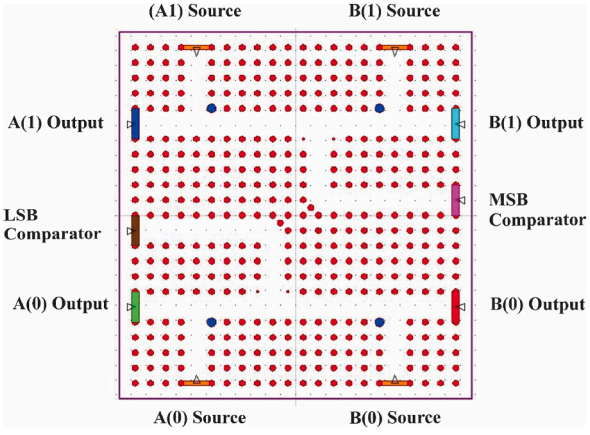

Fig. 1. The proposed all-optical 2-bit comparator.

Several waveguides and four nanoresonators with a 40 nm radius were employed to construct this device. Additionally, at the end of the waveguide that is linked to the light source, adjust rods of a 153 nm radius are employed. In Fig. 1, the suggested structure is demonstrated as previously stated; the structure's lattice constant is 510 nm, and the dielectric rods' radius is 102 nm. The area of the proposed structure will be ±5.5 μm in the Z direction and ±5.9 μm in the X direction, which will be equal to 129.8 μm^2; the total area in which the structure is included, along with a larger amount of space to achieve more accurate numerical analysis results. Using the PWE analysis, a variety of band gaps have been considered for various rod radii.

Two nanoresonators are utilized at the beginning of the O1 output, and their radius is 40 nm. The efficacy of the suggested nanostructure relies on the principle of interference. The shown structure in Fig. 1 has four inputs and six outputs. Upon traversing the input waveguide, the incident light sources encounter the central waveguide, which functions as a beam splitter, effectively diverting the light into two opposing directions around said beam splitter. The suggested structure, as demonstrated in Fig. 1, uses a Gaussian light source and has four inputs for input bits A and B applied to the structure while the light source power is set to 0.5 $W/\mu m^2$.

The structure design functions in such a way that the input sources impose the minimum destructive effect and interference on one another. In this way, if only a single input is in the logical open state, initially, the designed wave splitter directs it toward its corresponding port in the output, and eventually, it is directed toward the primary waveguide. Besides this issue, the resonator rods and the tuning rod direct the incoming light wave toward the comparator output. The use of such a method will impose the minimum destructive effect on the other output ports of the structure next to the other source of light. As a result, the waveguide structure design should present no potential damage to the other ports. In addition, when all the inputs or two logically high/low inputs are in the logically ON state, given the phase difference, the input wave is directed to the output monitor as well as the nano-resonators along with the waveguide length of the two inputs. A 180° phase difference will prevent light from entering the port of the comparator. The number of light sources can be decreased by using the monitor method corresponding to every single input next to the same input.

In addition, the optical power at the output is shown on six displays. Furthermore, the comparator depends heavily on two monitors that identify the low-value bit of the LSB and the high-value bit of the MSB.

All modes will be examined in the following to determine how well the suggested nanostructure performs. Blue monitors belong to input A(1) and green monitor belongs to input A(0). Also, the turquoise color monitors belong to input B(1) and the red color monitor belongs to input B(0). Each photonic crystal structure has its disadvantages and advantages. A variety of structures will be employed in order to discover the desirable band gap. Given the various designs presented for these structures, by scrutinizing both structures to reach a higher contrast level and an enhanced structure, the square structure was employed. In addition, given the multitude of output and input ports and the optimal guidance mode based on the interference effect, it is too difficult for a reversible structure to assume a hexagonal structure. From another viewpoint, the presence of air holes within the dielectric substrate brings about a great number of benefits, the most notable of which is the possibility of simpler construction. Essentially, given the decreased light speed in such structures, providing a shorter delay time will be impossible. However, our suggested structure is characterized by less delay time, simultaneous use of ten output and input ports, higher processing speed, and an appropriate symmetry. For this reason, this structure design has been employed.

Besides their two main ports, the earlier single-bit structures had an input port, which was employed as a bias. In order to design these structures, three input ports were employed. In addition, given the use of the above three ports and the fact that the structure has not been designed as a reversible structure (forwarding the input sources to a particular output), as a result of the interference between all three light sources in the structure, these structures showed higher losses. By employing the same method in the present paper, besides decreasing the structure losses resulting from wave interference, the light waves were forwarded toward their concerned output ports. Besides the losses issue, using the two main ports that will be compared, the structure was subjected to biasing. These considerations paved the way to decrease the number of light sources for saving purposes.

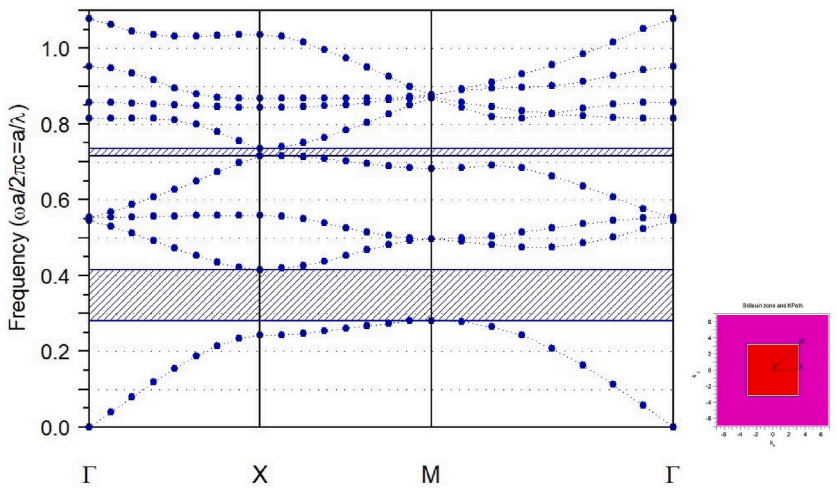

Fig. 2. TM band structure and the first Brillouin zone.

3. Photonic band-gap extraction

It is necessary to extract the emission modes of said nanostructure via the PWE technique to facilitate the construction of the suggested nanostructure. This extraction process necessitates an examination of the region associated with the photonic band gap of the nanostructure. This approach is classified as one strategy that relies on frequency analysis. Applying the PWE approach for numerical analysis, the photon band gap area for various radii in the TM mode will be produced, as illustrated in Fig. 2. In order to design the suggested structure, the structural propagation modes will be initially extracted using PWE. As soon as the unique structural modes of the whole structure are obtained, the band gap region will be determined for the TM mode. By applying this technique and designing the structure for the desired application (including the applied wavelength), one may select the structural lattice constant. Fig. 2 has been extracted by employing this analysis technique. As soon as this item is selected, one may determine the exact wavelength of the structure by solving Maxwell's equations for the same structure using the FDTD technique. After determining the mentioned wavelength and employing the numerical solution of Maxwell's equations obtained using the FDTD technique, one may analyze the structural performance. The present paper extracted the diffusion modes of the structure by employing the PWE technique. Then, by employing the FDTD technique, a full-wave numerical analysis was conducted for the structure to obtain the field distribution and time response diagrams for all possible scenarios presented in this paper.

The stop band of photons occurs within the frequency range of $0.289 < a/\lambda < 0.421$. The nanostructure under consideration has a lattice constant of 510 nm, while the silicon dielectric rods possess a radius of 102 nm. The wavelengths included within this structure's first photon stop band for transverse magnetic (TM) emission modes range from 1235 nm to 1799 nm. As mentioned above, the structure is deemed appropriate for utilization in the third communications window, namely, operating at a wavelength of 1550 nm. To determine the band gap of the desired structure, a lattice constant radius of 0.2 has been utilized. To use the structure in the third telecommunication window on the basis of the obtained band gap, it is designed in such a way that the a/λ frequency is situated within the same range, and by considering a 1550 nm wavelength, the constant value of the network is designed.

4. Numerical analysis of the proposed structure

The modeling and analysis of the multifunctional photonic crystal structure described in the paper will be covered in this part. The nanostructure has been numerically analyzed, and the analysis's findings have been obtained using the FDTD technique. Eqs. (1)–(3) express the normalized Maxwell's equations utilized in the finite-difference time-domain (FDTD) computational analysis [33]:

$$\frac{\partial \widetilde{D}}{\partial t} = \frac{1}{\sqrt{\varepsilon_0 \mu_0}} \nabla \times H \tag{1}$$

$$\widetilde{D}(\omega) = \varepsilon_r^*(\omega) \cdot \widetilde{E}(\omega) \tag{2}$$

$$\frac{\partial H}{\partial t} = -\frac{1}{\sqrt{\varepsilon_0 \mu_0}} \nabla \times \widetilde{E} \tag{3}$$

H_x and H_z are included in the aforementioned equations as the TM mode is used by the Ez nanostructure. Substituting H_x, H_z, and E_z into the equations above yields Eqs. (4)–(7) [33]:

$$\frac{\partial D_z}{\partial t} = \frac{1}{\sqrt{\varepsilon_0 \mu_0}} \left(\frac{\partial H_y}{\partial t} - \frac{\partial H_x}{\partial t} \right) \tag{4}$$

$$D_z(\omega) = \varepsilon_r^*(\omega) \cdot E_z(\omega) \tag{5}$$

$$\frac{\partial H_x}{\partial t} = -\frac{1}{\sqrt{\varepsilon_0 \mu_0}} \frac{\partial E_z}{\partial y} \tag{6}$$

$$\frac{\partial H_y}{\partial t} = \frac{1}{\sqrt{\varepsilon_0 \mu_0}} \frac{\partial E_z}{\partial x} \tag{7}$$

Eq. (8) yields the best result when medium A's impedance is almost equal to medium B's, producing a reflected wave that is almost negligible. Perfectly matched layers (PMLs) are shown to be a very flexible and effective boundary condition for integrating ABCs. The reflected wave value when propagating from medium A to medium B can be determined by [33]:

$$\Gamma = \frac{\eta_A - \eta_B}{\eta_A + \eta_B} \tag{8}$$

where, impedances of media A and B can be measured as:

$$\eta = \sqrt{\frac{\mu}{\varepsilon}} \tag{9}$$

where, ε and μ represent permittivity and permeability, respectively, which can be calculated using Eqs. (10) and (11) [33]:

$$\varepsilon = \varepsilon_0 \bullet \varepsilon_r \tag{10}$$

$$\mu = \mu_0 \bullet \mu_r \tag{11}$$

In [61,62], it is stated that to calculate space/time interval values, the relations governing these values should be used. In this paper, these relations are used. For example, it is given that Δx or Δz values can be chosen from λ/10 to λ/20. In this analysis's meshing method, the minimal size values for meshing in the z- and x-directions, Δz and Δx, are equal to λ/16. The area of the proposed structure will be ±5.5 μm in the Z direction and ±5.9 μm in the X direction. In this instance, the Δt values will be obtained as:

$$\Delta t < \frac{1}{c\sqrt{\left(\frac{1}{\Delta x}\right)^2 + \left(\frac{1}{\Delta z}\right)^2}} \tag{12}$$

As shown in Fig. 1, the comparator structure consists of 4 light sources and 6 monitors. The light sources of this structure will be divided into two parts on the left side of the structure which is considered as input A and the right side of the structure which is considered as input B of the structure. The value of the least significant bit will be considered with the lower ports of the structure, and the most significant bit will be applied to the comparator from the optical sources side of the upper structure.

In this way, A(0) and B(0) will be the lower light sources of the structure, and A(1) and B(1) will be the upper light sources of the structure. The logic used in this all-optical comparator is based on active LOW logic. This means that if two inputs are equal, the comparison result will be zero, and if the inputs are opposite, the comparison value will be equal to one. In other words, this comparator will show the differences in the inputs. In this way, the two monitors located in the center of the structure will perform the comparison. A two-bit comparator will be used to compare two-bit numbers. In other words, to realize this comparator, it is necessary to consider 2N states. For the proposed structure, 16 different modes should be checked. Another convenient feature of the structure is that, in addition to comparing two numbers, the input values of each port can be obtained by using four other built-in output ports. Due to the direction of the light source from all the input ports to the output ports as well as to the light sources, it is possible to design other devices according to the proposed structure.

Case 1. In the first case, all ports are equal to zero value and are in the logical off state. In other words, the value will be B = "00″ and A = "00". In this case, since the structure is based on active logic. The comparison of two numbers is equal to zero, which means that the two numbers are equal. Also, all other quad monitors that will display input sources will be equal to zero value. The electromagnetic field distribution diagram is shown in Fig. 3.

Case 2. In the second case, only the B(0) source will have value and the other sources will not include the optical field. In this case, the comparison of high values input values (A(1) and B(1)) will be similar to the previous case. Since the low values of the input sources are different, the difference value will be turned on at the output port of the lower comparator of the structure. Also, the monitor corresponding to the light source will have a value of B(0). The electromagnetic field distribution and time response for the second case are shown in Figs. 4 and 5. According to the time response diagram, it will reach 0.9 output power in less than 0.3 ps. In other words, the time delay for the proposed structure is about 300 fs.

Case 3. In the third case, only source A(0) will have a value and the other sources will not include the optical field. In this case, the comparison of high-value input values (A(1) and B(1)) will be similar to the first case. Since the low-value values of the input sources are different, the difference value in the output port of the lower comparator of the structure will be on. Also, the monitor corresponding to the light source will have a value of A(0). The electromagnetic field distribution and time response for the third case are shown in Figs. 6 and 7.

Case 4. In the fourth state, sources B(0) and A(0) will have value, and other sources will be off. In this case, the comparison of high-value input values (A(1) and B(1)) will be similar to the first case. Since the low-value values of the input sources are the same, the difference value in the output port of the lower comparator of the structure will be turned off. Also, the monitor corresponding to the

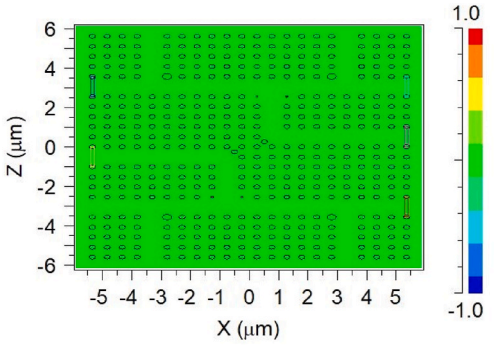

Fig. 3. The electromagnetic field distribution diagram of case 1 in which A = B = "00".

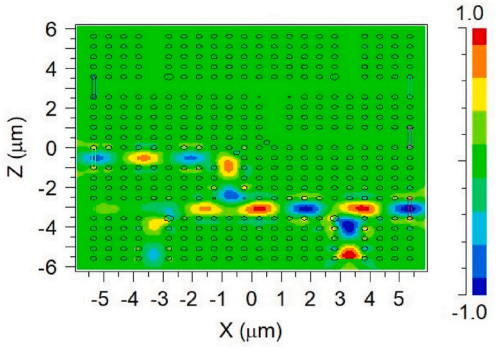

Fig. 4. The electromagnetic field distribution diagram of case 2 in which A(1) = B(1) = '0′ and A(0) = '0'<B(0) = '1'.

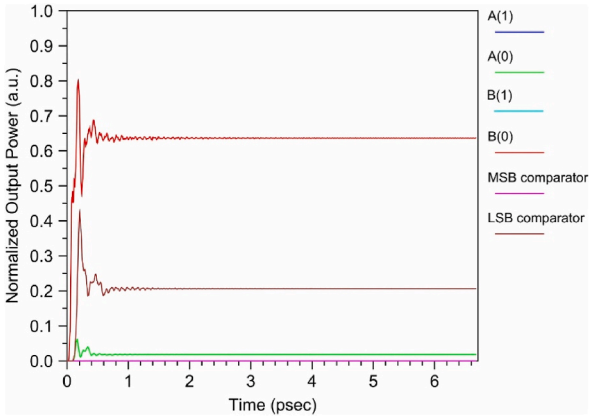

Fig. 5. The response time of Case 2.

light source will have the values B(0) and A(0). This mode will be similar to mode 1, with the difference that in mode 1, the monitors at the bottom of the proposed structure were in the off mode, but in this mode, the monitors at the bottom of the structure will be logical in clear mode. Therefore, it can be said that this structure will have access to the inputs of the structure in addition to the comparison operation, which will be very helpful for the design of more complex structures. The electromagnetic field distribution and time response for the fourth case are illustrated in Figs. 8 and 9.

Case 5. In the fifth case, only the source B(1) will have a value and the other sources will not include the optical field. In this case, the comparison of high-value input values (A(0) and B(0)) will be similar to the first case. Since the low-value values of the input sources are different, the difference value in the output port of the comparator above the structure will be on. Also, the monitor corresponding to the light source will have a value of B(1). The electromagnetic field distribution and time response for the fifth case are shown in Figs. 10 and 11.

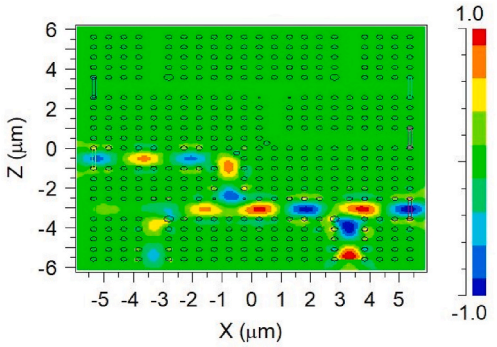

Fig. 6. The electromagnetic field distribution diagram of case 3 in which A(1) = B(1) = '0′ and A(0) = '1'>B(0) = '0'.

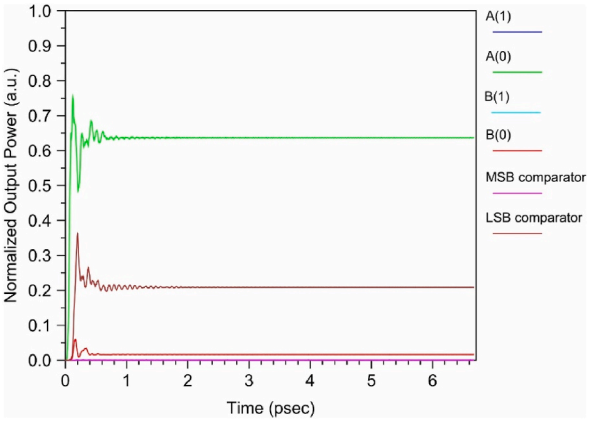

Fig. 7. The response time of Case 3.

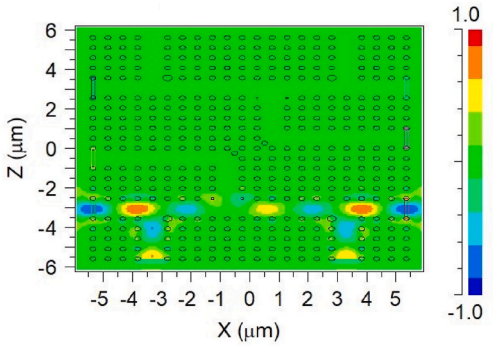

Fig. 8. The electromagnetic field distribution diagram of case 4 in which A(1) = B(1) = '0′ and A(0) = B(0) = '1'.

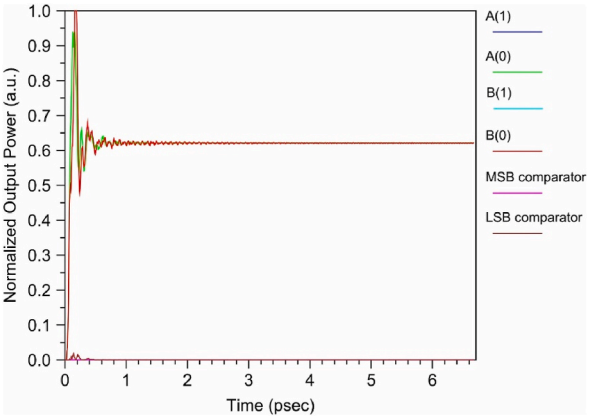

Fig. 9. The response time of Case 4.

Case 6. In the sixth case, the value of input B will be "11″, which will include the low-value and high-value bits of input B. The input value will be A = "00". Since the input values of both ports are different, both the lower and upper comparator ports will have a value. In addition to this, the monitors related to B(0) and B(1) will also have values. Since input A will be equal to zero and it is off, naturally the values related to monitor A will be equal to zero. The electromagnetic field distribution and time response for the sixth case are shown in Figs. 12 and 13.

Case 7. In the seventh case, B(0) = A(1) = 0 and B(1) = A(0) = 1. In this way, the low-value and high-value values of the input are different. In this case, the values of the monitor corresponding to each of the inputs are on, and the high-value bit comparator monitor and the low-value bit comparator monitor are logically on due to the difference between these bits. The electromagnetic field

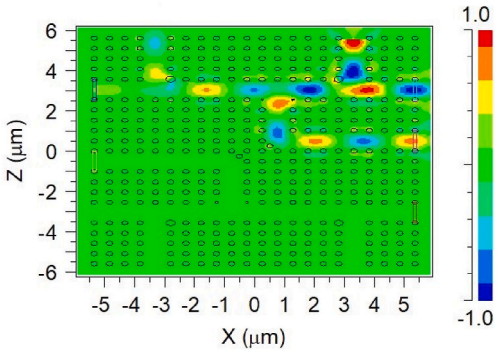

Fig. 10. The electromagnetic field distribution diagram of case 5 in which A(1) = '0'<B(1) = '1' and A(0) = B(0) = '0'.

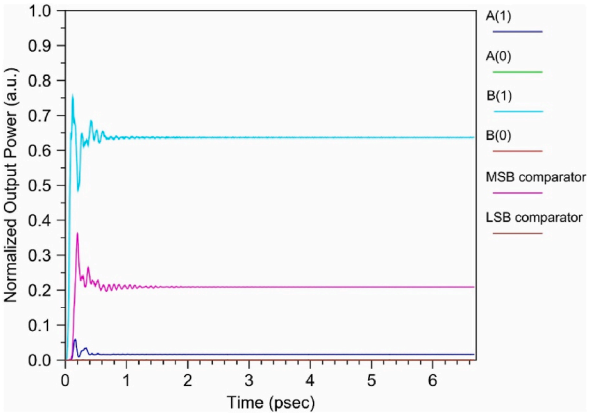

Fig. 11. The response time of Case 5.

distribution and time response for the seventh case are illustrated in Figs. 14 and 15.

Case 8. In the eighth state, the values of the low-value bits of two inputs are on, and the high-value bit of input B is equal to one and the high-value bit of input A is equal to zero. The output monitor corresponding to the low-value bit is equal to zero due to the two low-value inputs being the same, the monitors corresponding to the low-value bits will be in a logical light state due to having a light field. The high-valued comparator bit of the structure will be logically on because the input high-valued bits differ in value. The electromagnetic field distribution and time response for the eighth case are shown in Figs. 16 and 17.

Case 9. In the ninth state, all low-value ports are equal to zero and are in a logical shutdown state. Only the high-value port of input A will have a value. In this way, the comparison of two inputs for the low-value bits is similar to the initial state and for the high-value bits due to the difference, the high-value comparator port and the port corresponding to A(1) will have a value. The electromagnetic field distribution and time response for the ninth case are shown in Figs. 18 and 19.

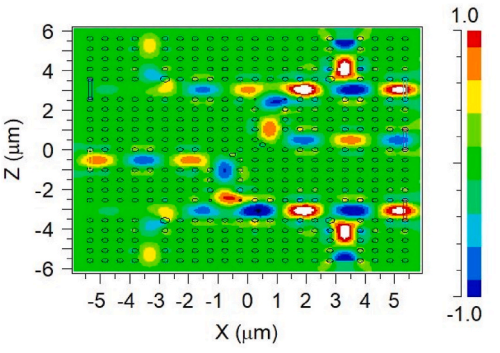

Fig. 12. The electromagnetic field distribution diagram of case 6 in which A(1) = '0'<B(1) = '1' and A(0) = '0'<B(0) = '1'.

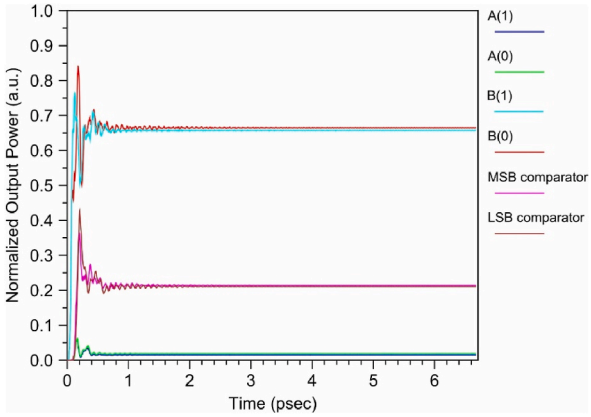

Fig. 13. The response time of Case 6.

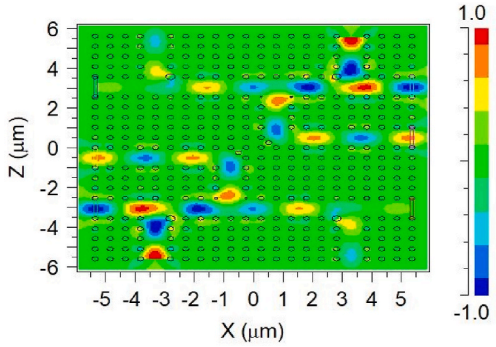

Fig. 14. The electromagnetic field distribution diagram of case 7 in which A(1) = '0'<B(1) = '1′ and A(0) = '1'>B(0) = '0'.

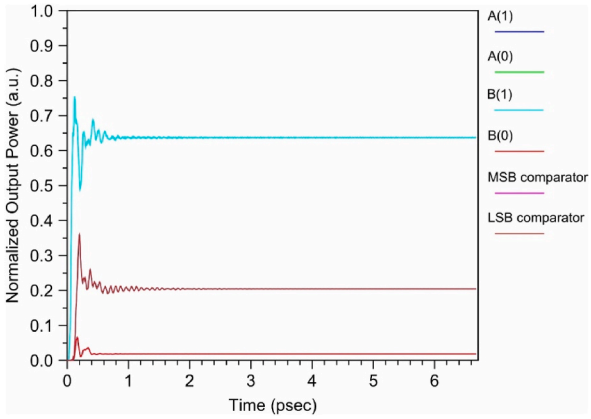

Fig. 15. The response time of Case 7.

Case 10. In the tenth state, which is the double of the seventh state, B(0) = A(1) = 1 and B(1) = A(0) = 0. In this way, the low-value and high-value values of the input are different. In this case, the values of the monitor corresponding to each of the inputs are on, and the high-value bit comparator monitor and the low-value bit comparator monitor are logically on because of the difference between these bits. The electromagnetic field distribution and time response for the tenth case are illustrated in Figs. 20 and 21.

Case 11. In the 11th state, the value of input B will be "00″, which will include the low-value and high-value bits of input B. The input value will be A = "11". Since the input values of both ports are different, both the lower and upper comparator ports will have a value. In addition to this, the monitors related to A(0) and A(1) will also have a value. Since input B will be equal to zero and it is off, naturally the values related to monitor B will be equal to zero. This double mode is the sixth mode. The electromagnetic field distribution and

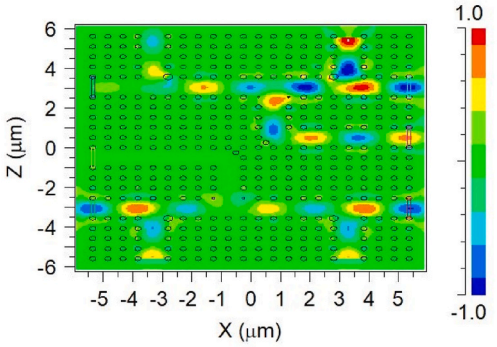

Fig. 16. The electromagnetic field distribution diagram of case 8 in which A(1) = '0'<B(1) = '1′ and A(0) = B(0) = '1'.

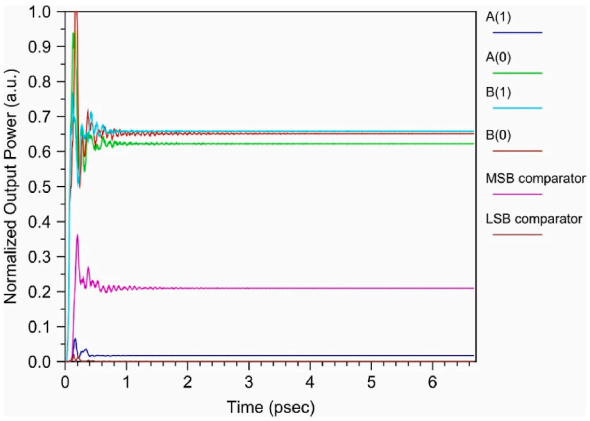

Fig. 17. The response time of Case 8.

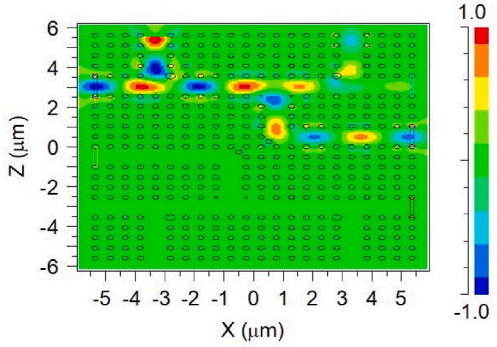

Fig. 18. The electromagnetic field distribution diagram of case 9 in which A(1) = '1'>B(1) = '0′ and A(0) = B(0) = '0'.

time response for the 11th case are shown in Figs. 22 and 23.

Case 12. In the twelfth state, all input sources except B(1) will be in a logical ON state. The low values of the two inputs are equal and the high values have different values. The low-value comparator bit is logically off and the high-value bit is logical one, which shows the difference between the two high-value bits. The monitors corresponding to all inputs except B(1) are in the logical on state. The electromagnetic field distribution and time response for the twelfth case are shown in Figs. 24 and 25.

Case 13. In the 13th state, the low-value bits of the input are in the logical off state and only the high-value bits have an optical field. Since the two numbers are equal and there is no difference, the low and high comparison bits will be equal to zero. Also, the values of monitors corresponding to high-value inputs will be logically on and monitors corresponding to low-value bits will be logically off. The electromagnetic field distribution and time response for the 13th case are shown in Figs. 26 and 27.

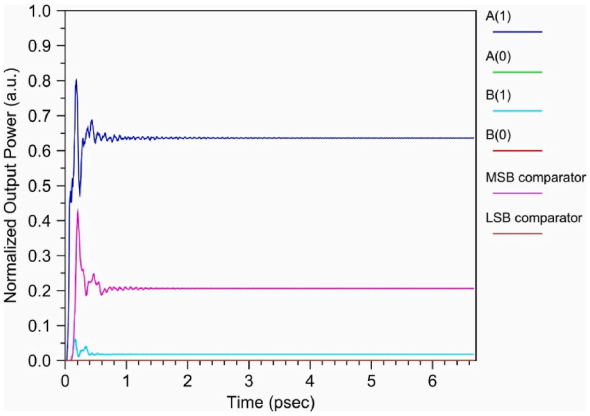

Fig. 19. The response time of Case 9.

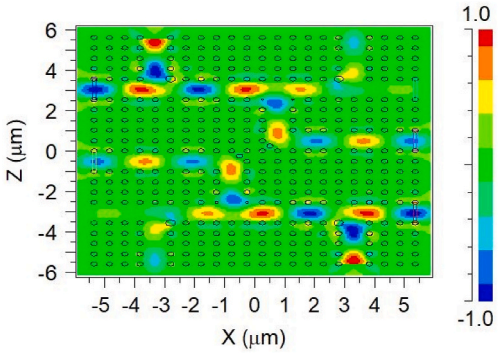

Fig. 20. The electromagnetic field distribution diagram of case 10 in which A(1) = '1'>B(1) = '0' and A(0) = '0'<B(0) = '1'.

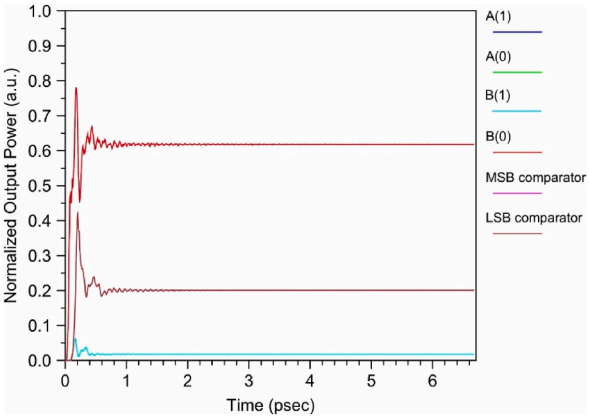

Fig. 21. The response time of Case 10.

Case 14. In the fourteenth case, the input A(0) = 0 and other input sources will have an optical field. Since the high-valued values are the same and there is no difference, the high-valued comparator is logical zero and will be in the off state. The low-valued comparator bit will be a logical one due to the difference in the input sources. Also, the monitor corresponding to each of these inputs with a value is on and in a logical state, but the monitor corresponding to A(0) is off. The electromagnetic field distribution and time response for the fourteenth case are shown in Figs. 28 and 29.

Case 15. In the 15th state, the input B(0) = 0 and other input sources will have an optical field. Since similar to the 14th mode, the high-valued values are the same and there is no difference, the high-valued comparator is equal to logical zero and will be turned off. The low-valued comparator bit will be a logical one due to the difference in the input sources. Also, the monitor corresponding to each

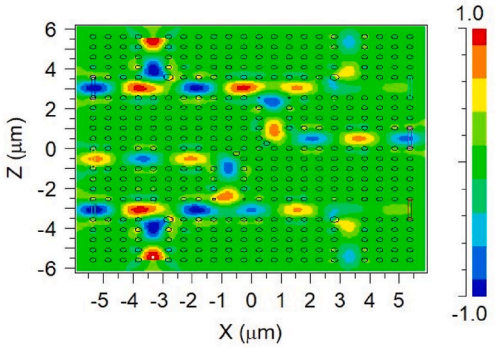

Fig. 22. The electromagnetic field distribution diagram of case 11 in which A(1) = '1'<B(1) = '0' and A(1) = '1'>B(0) = '0'.

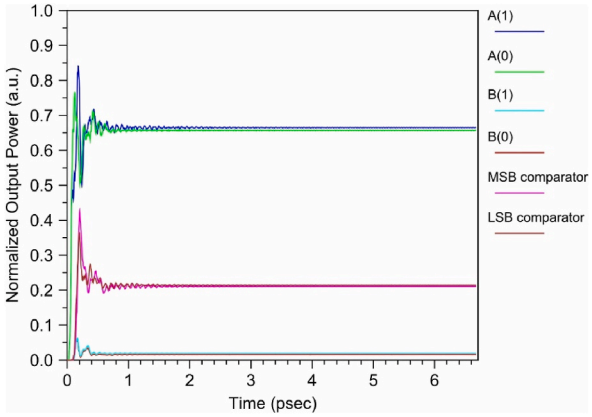

Fig. 23. The response time of Case 11.

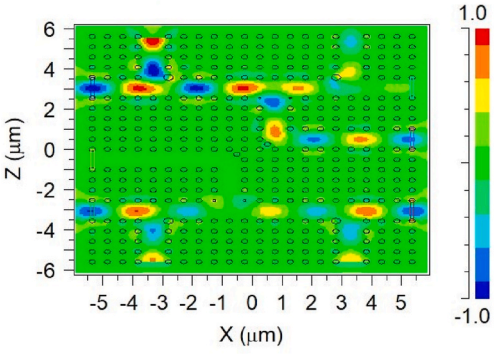

Fig. 24. The electromagnetic field distribution diagram of case 12 in which A(1) = '1'>B(1) = '0' and A(0) = B(0) = '1'.

of these inputs with a value is on and in a logical state, but the monitor corresponding to B(0) is off. The electromagnetic field distribution and time response for the 15th case are shown in Figs. 30 and 31.

Case 16. In the 16th state, all input sources have a light field. In other words, two numbers are equal. In this case, due to the lack of difference in the input values, the low-value and high-value comparator bits will be off and logically zero. The monitor corresponding to all inputs will also have a value. This mode is similar to the first mode, all values are the same. The unique feature of the proposed structure is that the input values are assigned to four corresponding output ports. In mode 1, the values of A and B were equal to zero, and the comparator bits were equal to zero due to the lack of difference, but the monitors corresponding to the inputs in these two modes, the first and sixteenth, were different. In other words, the input values of the structure can be obtained from the output of the structure. The electromagnetic field distribution diagram and response time for the twelfth case are shown in Figs. 32 and 33. According to the time response diagram, it will reach 0.9 output power in less than 300 fs. This is also the case for all the previous modes.

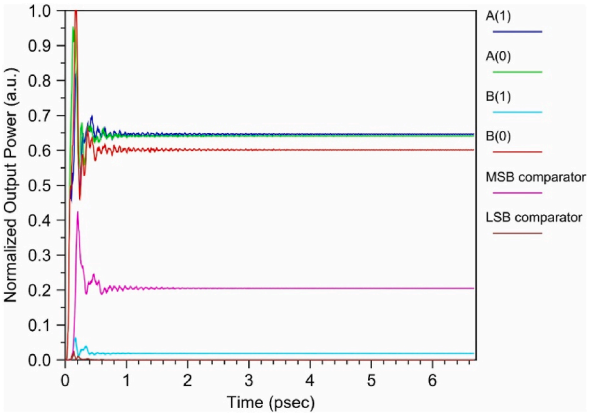

Fig. 25. The response time of Case 12.

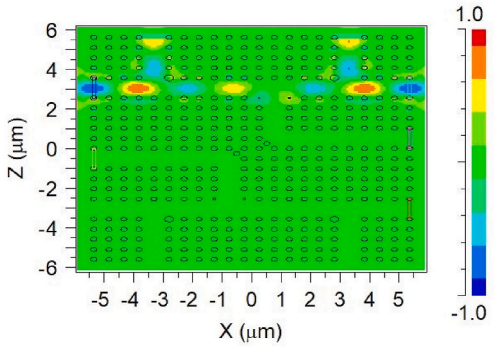

Fig. 26. The electromagnetic field distribution diagram of case 13 in which A(1) = B(1) = '1′ and A(0) = B(0) = '0'.

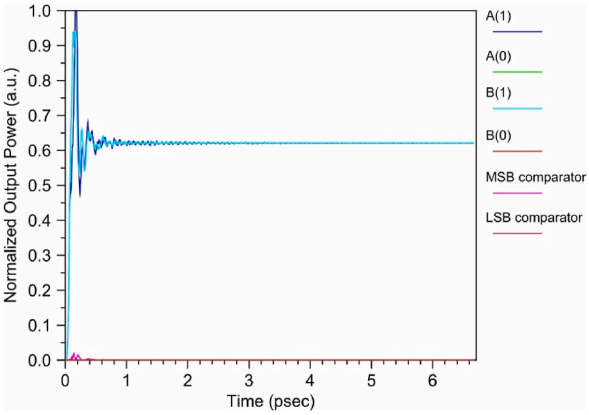

Fig. 27. The response time of Case 13.

5. Discussion and comparison of the comparator performance

5.1. Evaluation based on contrast ratio

This section introduces the contrast ratio to evaluate the suggested nanostructure's performance. The difference rate indicates the amount that separates the output power in the logical zero state from the logical one state. The greater this number, the more successfully the suggested structure has operated, and the further apart the logical one and logical zero values are, the better for output port identification. Eq. (13) gives the rate of change [33]:

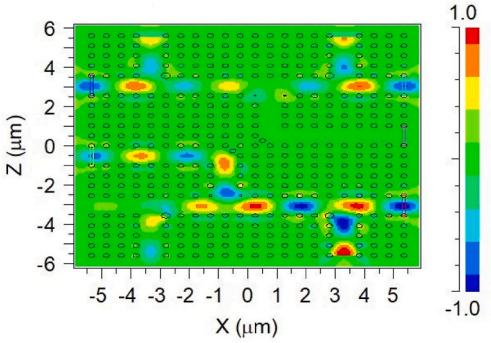

Fig. 28. The electromagnetic field distribution diagram of case 14 in which A(1) = B(1) = '1' and A(0) = '0'<B(0) = '1'.

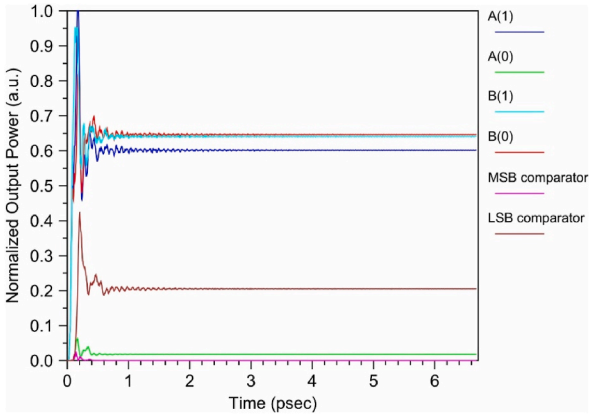

Fig. 29. The response time of Case 14.

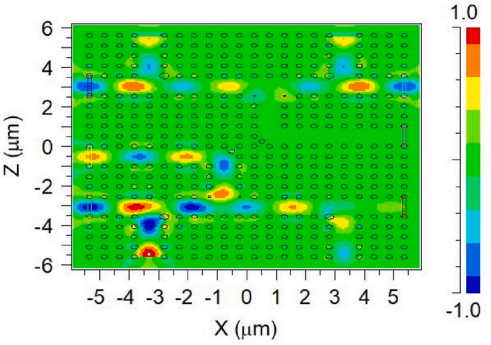

Fig. 30. The electromagnetic field distribution diagram of case 15 in which A(1) = B(1) = '1' and A(0) = '1'>B(0) = '0'.

$$\text{Contrast Ratio (dB)} = 10 \log \frac{Output(i)_{ON}}{Output(i)_{OFF}} \tag{13}$$

The minimum and maximum power intensity values in ON and OFF states are 0.25 and 0.0005 W/μm^2, respectively, for the comparator ports, namely the least significant bit (LSB) and the most significant bit (MSB). Thus, the minimum contrast ratio is 13.8 dB. The output values for all monitors along with the contrast ratios calculation. Also, for the first to fourth cases, the comparator pulse diagram is shown in Fig. 34. As mentioned in the previous section, the time delay for the proposed structure is about 0.3 ps.

5.2. *Evaluate the performance of the all-optical 2-bit reversible comparator*

The proposed all-optical 2-bit reversible comparator was compared in terms of performance with other relevant works once a

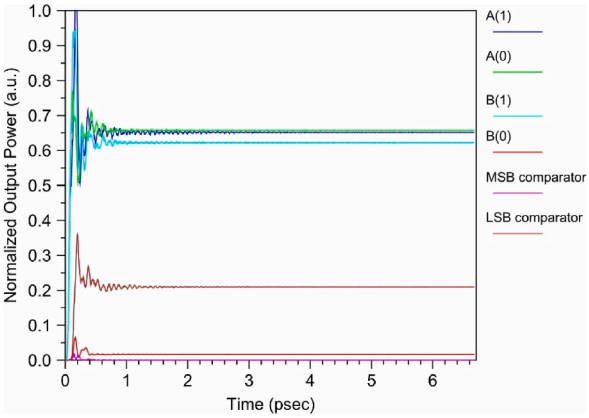

Fig. 31. The response time of Case 15.

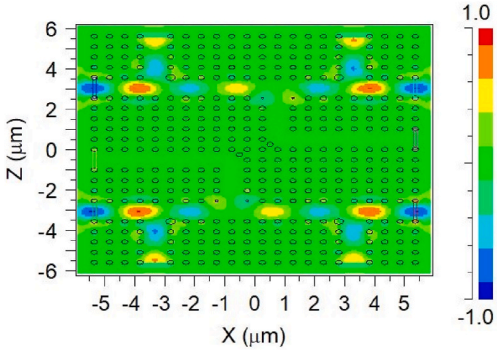

Fig. 32. The electromagnetic field distribution diagram of case 16 in which A(1) = B(1) = '1′ and A(0) = B(0) = '1'.

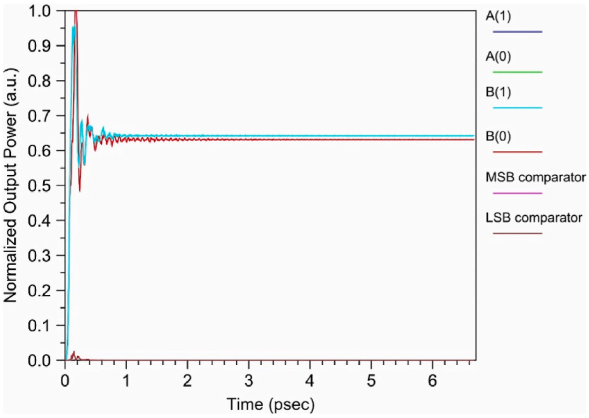

Fig. 33. The response time of Case 16.

numerical analysis was performed on its different states. Table 1 demonstrates that the proposed comparator has a good contrast ratio and that the nanostructure proposed herein performs exceptionally well in comparison to similar nanostructures. Besides, the difference between 0 and 1 is a good value, and because of the large difference between the aforementioned values, it will be useful for differentiating between the two. The proposed comparator was analyzed in both linear and nonlinear modes, yielding a contrast ratio of 11.96 dB in the latter mode, indicating highly optimal performance. Compare the proposed all-optical reversible comparator with similar is shown in Table 2.

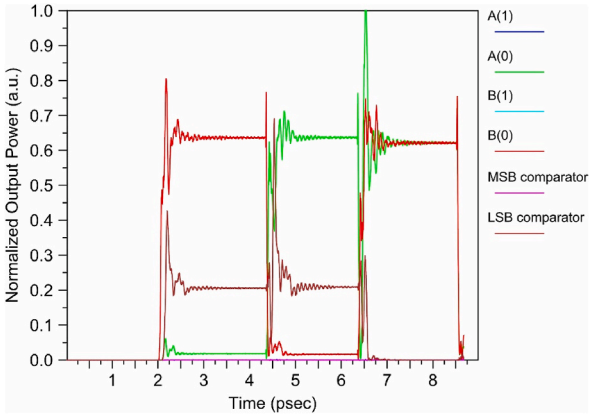

Fig. 34. Operation of the 2-bit reversible comparator in different cases.

5.3. Fabrication tolerance

Photonic crystal fabrication is a procedure by which repeating, regular structures characterized by periodic variations in the refractive index of substances are created. A number of techniques are available to fabricate photonic crystals, such as lithography techniques, e.g., nanoimprint lithography and electron beam lithography, and deposition methods, e.g., atomic layer deposition and chemical vapor deposition. Researchers use the mentioned methods to fabricate photonic crystal structures, including 3D and 2D photonic crystals [63–66].

To fabricate photonic crystals means applying a number of processing steps in order to generate a favorable pattern for the structures. This process in the lithography-based processes involves the creation of a template/mask guiding the patterning/deposition of materials onto the substrate. Then, the substrate surface treatment is carried out, which is followed by applying a photosensitive material. As soon as the exposure is completed, the intended pattern is developed using chemical processing. This is followed by deposition/etching so as to transfer the pattern onto the substrate. These methods may be applied in combination or separately in order to fabricate photonic crystals characterized by various features and structures [63].

The studies are continued so as to develop novel scalable and cost-effective fabrication methods and optimize the present methods so as to decrease the production costs and increase the throughput. In addition, applying new materials to fabricate photonic crystals and developing advanced computational modeling methods can be of great help to speed up the optimization and designing process of the photonic crystals. The recent trends and advancements in the field of photonic crystal technology structures present a solution to decrease the duration of the designing process. The major advanced approaches in the field of photonic crystal fabrication are as follows.

- Self-assembly: Using these methods, e.g., colloidal lithography or block copolymer lithography, one may fabricate crystals with a periodicity and self-organization level, which is hard to achieve using the traditional methods of lithography [65].

Table 1
Proposed all-optical 2-bit reversible comparator performance.

Case	Comparator input values				Comparator output values					
	A(1)	B(1)	A(0)	B(0)	MSB(C)	LSB(C)	A(1)	B(1)	A(0)	**B(0)**
1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	P_{in}	0	$0.25P_{in}$	0	0	$0.02P_{in}$	$0.42P_{in}$
3	0	0	P_{in}	0	0	$0.25P_{in}$	0	0	$0.66P_{in}$	$0.02P_{in}$
4	0	0	P_{in}	P_{in}	$0.0005P_{in}$	$0.0003P_{in}$	$0.0001P_{in}$	$0.0002P_{in}$	$0.65P_{in}$	$0.65P_{in}$
5	0	P_{in}	0	0	$0.25P_{in}$	0	$0.022P_{in}$	$0.65P_{in}$	0	$0.0005P_{in}$
6	0	P_{in}	0	P_{in}	$0.26P_{in}$	$0.26P_{in}$	$0.022P_{in}$	$0.68P_{in}$	$0.027P_{in}$	$0.7P_{in}$
7	0	P_{in}	P_{in}	0	$0.25P_{in}$	$0.25P_{in}$	$0.025P_{in}$	$0.65P_{in}$	$0.65P_{in}$	$0.025P_{in}$
8	0	P_{in}	P_{in}	P_{in}	$0.25P_{in}$	0	$0.025P_{in}$	$0.68P_{in}$	$0.65P_{in}$	$0.69P_{in}$
9	P_{in}	0	0	0	$0.25P_{in}$	0	$0.66P_{in}$	$0.025P_{in}$	0	0
10	P_{in}	0	0	P_{in}	$0.25P_{in}$	$0.25P_{in}$	$0.64P_{in}$	$0.002P_{in}$	$0.002P_{in}$	$0.64P_{in}$
11	P_{in}	0	P_{in}	0	$0.25P_{in}$	$0.25P_{in}$	$0.7P_{in}$	$0.002P_{in}$	$0.68P_{in}$	$0.002P_{in}$
12	P_{in}	0	P_{in}	P_{in}	$0.25P_{in}$	0	$0.67P_{in}$	$0.027P_{in}$	$0.67P_{in}$	$0.63P_{in}$
13	P_{in}	P_{in}	0	0	$0.0003P_{in}$	$0.0005P_{in}$	$0.65P_{in}$	$0.65\ P_{in}$	0	0
14	P_{in}	P_{in}	0	P_{in}	0	$0.25P_{in}$	$0.63P_{in}$	$0.67\ P_{in}$	$0.025P_{in}$	$0.67P_{in}$
15	P_{in}	P_{in}	P_{in}	0	0	$0.25P_{in}$	$0.69\ P_{in}$	$0.65\ P_{in}$	$0.68P_{in}$	$0.02P_{in}$
16	P_{in}	P_{in}	P_{in}	P_{in}	0	0	$0.66\ P_{in}$	$0.67\ P_{in}$	$0.67P_{in}$	$0.66P_{in}$
Contrast Ratio (dB)					26.9	26.9	14	14.1	13.8	14

Table 2
Comparison of the proposed all-optical reversible comparator with similar works.

Ref	Functional	Material	Number of sources	footprint (μm^2)	CR (dB)	Time delay (psec)
Ref. [49]	1-bit Comparator	Si in air	5	1705	12	1.5
Ref. [50]	1-bit Comparator	Si in air	3	2619	10	1
Ref. [51]	1-bit Comparator	Si in air	4	<1500	10.4	4
Ref. [52]	1-bit Comparator	Si in air	4	624	10.73	1
Ref. [57]	1-bit Comparator	Si in air	3	318	9.85	1.5
This work	2-bit Reversible Comparator	Si in air	4	129.8	13.8	0.3

- Reactive ion etching: One can use this technique in order to generate highly precise and deep patterns in various materials. Reactive ion etching is especially useful for the fabrication of structures with a high aspect ratio, and it is often combined with other lithography methods [66].
- Templated growth: This technique provides the opportunity to fabricate photoniccrystals featuring a high precision level using pre-patterned templates in order to guide the crystal growth. Templated growth is especially helpful for the fabrication of inorganic photonic crystals.
- Computational design: One may use computational design tools, e.g., inverse-design algorithms and finite-difference time-domain simulations, to optimize the characteristics of photonic crystals and guide their process of fabrication. Using these tools, the fabrication and designing processes of complex photonic structures become more accurate and more efficient.

Ideal items are taken into consideration for the proposed reversible comparator's nanostructure; however, fabrication tolerance affects the production process of any device. The proposed comparator's nanostructure experiences a ±1 nm [fabrication] tolerance for the radius (R) of the dielectric rods in this nanostructure. Additionally, the contrast ratio will not change significantly according to the analyses suggested in the "proposed comparator design" section, even with adjustments to the adjuster and scattering rods of 1 nm.

6. Conclusion

In this paper, the design, simulation, and evaluation of an ultra-compact ultra-fast all-optical 2-bit reversible comparator nanostructure have been presented. The proposed comparator was optimized for input light source wavelength and adjuster/scattering rod radii. The proposed comparator herein was designed using the PWE method, and the FDTD method was used to provide the numerical results and simulate the nanostructure proposed herein. The proposed ultra-compact nanostructure delay time and footprint were approximately 300 fs and 129.8 μm^2, respectively. The nanostructure proposed herein was the first with good linear mode performance among all-optical 2-bit comparator nanostructures. Among exceptional characteristics of the proposed comparator were its high contrast ratio and bitrate (3.333 Tb/s in linear mode) in comparison to other all-optical comparators. These unique features render it applicable in all-optical integrated circuits.

Data availability statement

The data that support this study are available from the corresponding author upon reasonable request.

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CRediT authorship contribution statement

Ehsan Veisi: Software, Investigation. **Mahmood Seifouri:** Writing – review & editing. **Saeed Olyaee:** Writing – review & editing, Validation, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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