SCIENTIFIC REPORTS

OPEN

SUBJECT AREAS:
ELECTRICAL AND ELECTRONIC ENGINEERING
SURFACE PATTERNING
CHARACTERIZATION AND ANALYTICAL TECHNIQUES
ELECTRONIC DEVICES

Received
30 April 2013

Accepted
30 May 2013

Published
28 June 2013

Correspondence and requests for materials should be addressed to Y.S.K. (younskim@snu.ac.kr) or C.-H.S. (ch76.shin@samsung.com)

Fast, exact, and non-destructive diagnoses of contact failures in nano-scale semiconductor device using conductive AFM

ChaeHo Shin[1], Kyongjun Kim[2], JeongHoi Kim[1], Wooseok Ko[1], Yusin Yang[1], SangKil Lee[1], Chung Sam Jun[1] & Youn Sang Kim[2,3]

[1]Memory Division, Samsung Electronics, San #16 Banwol-Dong, Hwasung-City, Gyeonggi-do 445-701, Republic of Korea, [2]Program in Nano Science and Technology, Graduate School of Convergence Science and Technology, Seoul National University, Seoul 151-744, Republic of Korea, [3]Advanced Institute of Convergence Technology, 864-1 Iui-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-270, Republic of Korea.

We fabricated a novel in-line conductive atomic force microscopy (C-AFM), which can analyze the resistive failures and examine process variance with an exact-positioning capability across the whole wafer scale in in-line DRAM fabrication process. Using this in-line C-AFM, we introduced a new, non-destructive diagnosis for resistive failure in mobile DRAM structures. Specially, we focused on the self-aligned contact (SAC) process, because the failure of the SAC process is one of the dominant factors that induces the degradation of yield performance, and is a physically invisible defect. We successfully suggested the accurate pass mark for resistive-failure screening in the fabrication of SAC structures and established that the cause of SAC failures is the bottom silicon oxide layer. Through the accurate pass mark for the SAC process configured by the in-line C-AFM analyses, we secured a good potential method for preventing the yield loss caused by failures in DRAM fabrication.

In these days, various mobile devices such as smart phones, tablet computer, and mobile personal computers have gained much interest. Consequently, the semiconductor industry has also focused on mobile components such as mobile dynamic random access memory (mobile DRAM). In general, DRAM has mainly been used in desktop or laptop computers. However, with the rapid expansion in mobile technology, the need for mobile DRAM has grown substantially, and the product ability of mobile DRAM has been a critical issue in semiconductor industry. As the structures for mobile DRAM have become much finer and more complicated, various defect factors such as discernible bridges, breaks, holes, and scratch faults in the memory cell have a serious effect on the yield performance. As the yield performance of mobile DRAM is the most critical point when attempting to secure price competitiveness in the market and cost reductions, many semiconductor companies have handled this aspect as one of paramount importance.

To enhance the yield, the number of defects should be reduced, and any faults need to be detected at an early stage during fabrication. Critically, the detection and diagnosis of invisible defects such as junction leakage, crystal defects, and gate leakage, are the key factors for improving the yield in DRAM manufacturing[1–3]. Through the monitoring of invisible defects, effective defect isolation can be successfully conducted. Especially, non-destructive and on-the-spot diagnoses of invisible defects rapidly enable the production lines to cope, resulting in effective yield enhancement in the semiconductor industry.

Currently, the most common method for non-destructive, physical-failure analysis in the semiconductor industry including DRAM analysis is the passive voltage contrast (PVC) method[4,5]. The PVC method, more precisely, is the contact-level inspection through the brightness difference in the images of a focused ion beam (FIB) or scanning electron microscope (SEM) relating to electrical resistance[6,7]. This PVC method can easily determine leakage or abnormal contact via high resistance in DRAM structures. However, as the DRAM fabrication process involves much smaller, nano-scale structures, the manufacturing parameters have extremely small values. As the transistor in DRAM is fabricated with extra-shallow junctions and the polycrystalline gate oxide only has a thickness of less than 2 nm, the extremely small area of the contact circumference is insufficiently

charged by electrons or ions. Therefore, PVC inspection is not sensitive enough to diagnose failures in these ultra-fine DRAM structures. Currently, the analysis of contact resistive failure in the interface during the in-line fabrication process is still being carried out via the PVC method using an electron beam. However, as the pattern size has now been reduced to nano-scale proportions, the semiconductor industries are concerned, as the PVC method cannot adequately analyze the effects of the failures on the yield of the semiconductor chip. In addition, the PVC method only produces a simple failure mode analysis, for example, open and short circuits, which represents the extremes, and there are considerable difficulties in setting an exact pass level and in effectively promoting the yield performance. Therefore, an alternative method for the exact inspection of contact failures is essential for the enhancement of yield performance in the semiconductor industry. Additionally, an exact diagnosis of the structures in semiconductor chips would mean high throughput fabrication and quick follow-up measures being enabled.

Recently, as an advanced, non-destructive analysis method, conductive atomic force microscopy (C-AFM) has proved attractive, because it can identify, non-destructively, the status of contacts via direct current measurement on individual contacts. Until now, C-AFM has mainly been introduced in the advanced analysis of organic electronic devices or biosensors for the investigation of the electron transport mechanism[8–14]. As C-AFM has an inherently good potential for nano-scale inspection, many researchers have tried to develop a C-AFM-based inspection tool for the nano-scale semiconductor industry[15–19]. In practical terms, C-AFM can provide useful information for both electrical failure analysis (EFA) and physical failure analysis (PFA) in semiconductor devices. In addition, C-AFM analysis can provide a large, dynamic current-detecting range from 1 pA to 10 mA, and this is inherently more accurate and sensitive than PVC analysis. Furthermore, C-AFM can be utilized as a nano-probe to provide local I-V measurements for specific features of contacts.

Thus, C-AFM is thought to be a good, alternative inspection tool for fast, exact, and non-destructive diagnoses of contact failures in various nano-scale semiconductor devices. However, in order to develop the novel in-line inspection techniques using C-AFM, a deep and integrated understanding is essential regarding the nano-scale semiconductor device structures, the electrical mechanism of C-AFM, and the complicated fabrication techniques of all the equipment. The practical analysis of the in-line process for contact failure using C-AFM with a wafer scale has not been attempted yet because of the difficulty involved in the integration of complicated systems and the insufficient understanding of C-AFM applications in DRAM device structures.

Herein, we introduce the first in-line C-AFM system for surface resistive failure analysis in DRAM device fabrication. Specially, we focused on the self-aligned contact (SAC) process in DRAM fabrication, because the failure of the SAC process is one of the dominant factors that induces the degradation of yield performance, and is a physically invisible defect in DRAM structures[20]. By comparative analysis of C-AFM images and TEM images regarding the failure of the SAC process, we observed that the formation of native oxide between the polycrystalline silicon and Si substrate in the SAC process could induce the failures of tRDL (the allowed time interval between data-in and the word-line pre-charge), which is one of the typical parameters representing DRAM cell performance in DRAM. Additionally, with this approach, we established the criterion for the pass mark for the SAC process through measuring the resistivity using C-AFM. Furthermore, in the analysis of C-AFM for the failure of the SAC process, we propose an advanced SAC process through a plasma native oxide cleaning (PNC) process. This PNC process could increase the electrical quality by removing the native oxide layer formed in the SAC process. The in-line C-AFM analysis is quite promising for failure inspection to increase the effective yield promotion in the semiconductor industry.

Results

In-line C-AFM analysis for the electrical failure of SAC structure in the wafer. In order to show the potential of the C-AFM analysis, we first manufactured in-line C-AFM for the analysis of electrical resistance failures in a whole wafer scale for the DRAM fabrication (see the supplementary information, Figure S1). This in-line C-AFM is able to move by 60 mm/sec onto a wafer using the stage with a linear motor, and to exchange a tip automatically when conductive probe-wearing has taken place. As C-AFM can simultaneously measure both the topography and the electric current variation according to resistance difference, it is able to perform both the topological failure analysis and the EFA in the investigation range. Additionally, the mapping ability of in-line C-AFM can provide good guidance on the effect of the failure on the yield of further subsequent processes.

The structure of the DRAM cell and the scheme for C-AFM analysis detection are shown in Figure 1. As the size of the DRAM cell structure shrinks, the contact between the gate spacers becomes difficult to fabricate and this is handled by using the landing pad located on between the gate structures. However, through the SAC process, which uses the selective etching ratio between the nitride layer and boron phosphorous silicate glass (BPSG) in DRAM cells, we can produce a ladder-type surface profile, which is used as the mask. In the SAC process, we made both direct contact and buried contact into the narrow window of the fine structures without a severe digging process (Figure 1a and b). The SAC process successfully reduces the burden of the DRAM process. However, the invisible structure failures of the SAC induce the critical degradation of the DRAM yield.

During the in-line C-AFM failure analysis of the SAC, when the electrical resistive layer exists at the bottom of the polycrystalline silicon in the SAC, the electrical contact between the polycrystalline silicon and the Si substrate does not show ohmic contact, inducing failures in DRAM operation (Figure 1c). Actually, during the in-line fabrication process of DRAM, this EFA of the SAC process has been conducted by the PVC method, which is used for detecting different potentials via an electron beam. However, it is difficult for the PVC method to detect the shallow resistive layer, which may be formed after a SAC process. Furthermore, we cannot determine whether this shallow resistive layer has an influence on later processes in DRAM cells, or ultimately, on the yields of chips on the DRAM wafer. Consequently, by using C-AFM, as the local current can be measured

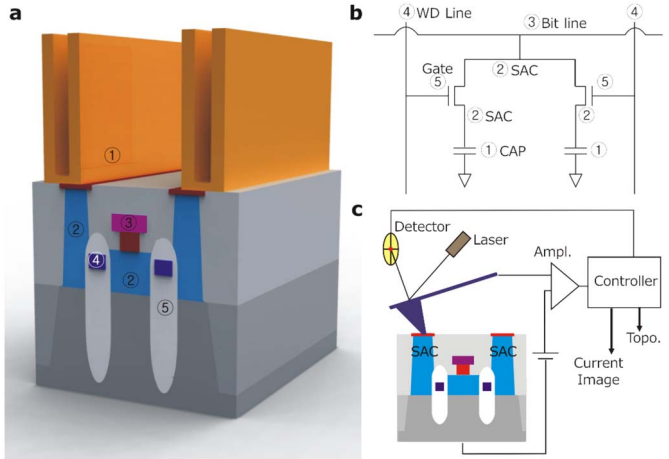

Figure 1 | C-AFM analysis in DRAM cell structure. (a) The schematics of a DRAM cell with the storage capacitors (①Capacitor ②SAC ③Bit line ④Word line ⑤Gate). (b) Equivalent circuit of the DRAM cell structure, (c) The sample structure and scheme of the C-AFM analysis in the DRAM structure.

in the pico-ampere range with nanometer-scale spatial resolution, the analysis of microscopic resistive failures is possible.

In C-AFM, the successfully fabricated SAC structures are shown in the images as follows: the topographical image of a normal SAC (Figure 2a) and the corresponding C-AFM current image with a bias of 4.0 V for a normal SAC (Figure 2b). Several process factors in forming the SAC must be carefully considered, such as cleaning before the SAC pad deposition, the concentration quality of the

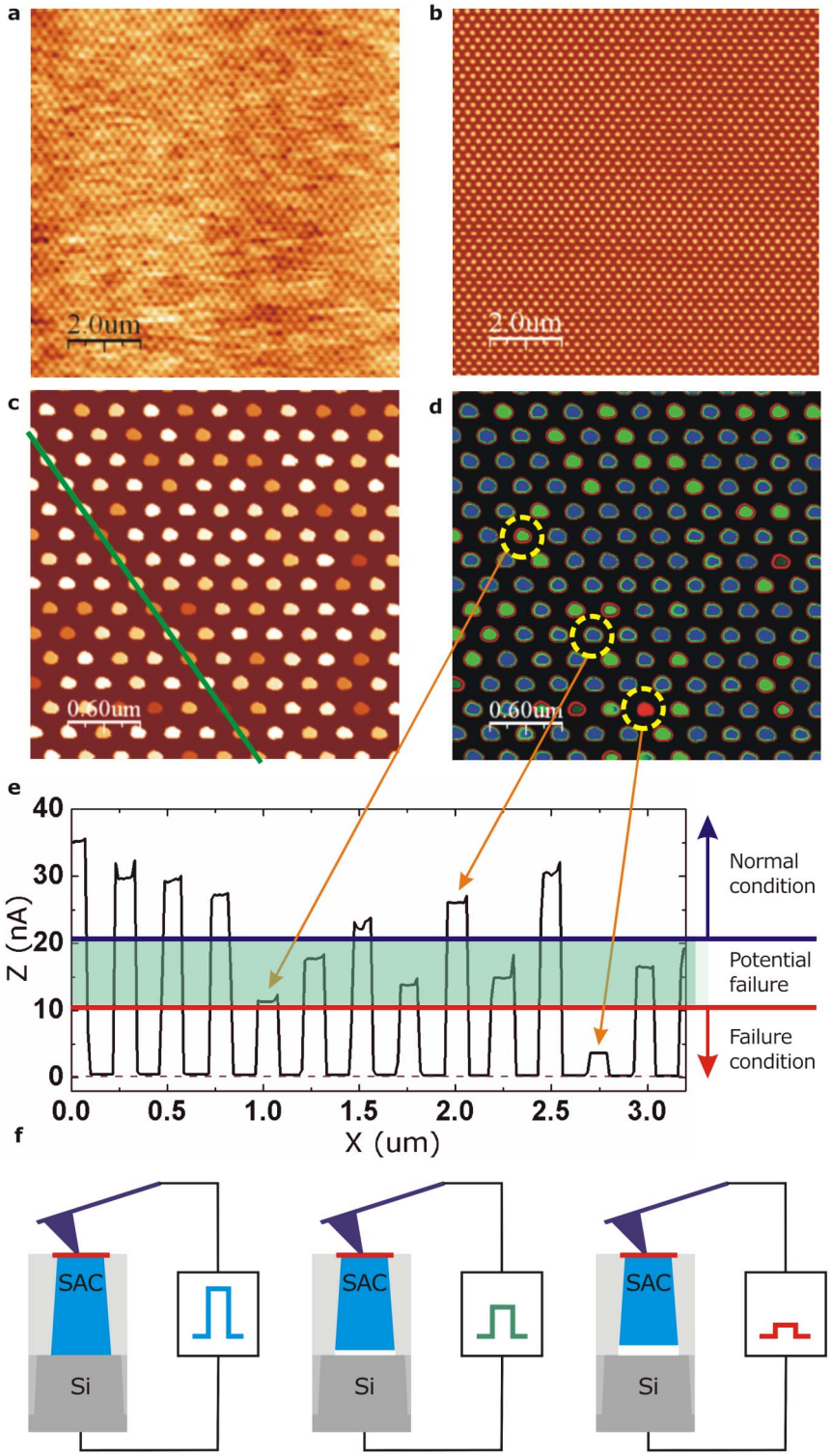

Figure 2 | Failure analysis using C-AFM in SAC structure. (a) Topography C-AFM image of a normal SAC, (b) Corresponding current image of C-AFM at a bias of 4.0 V for a normal SAC, (c) Current image of C-AFM at a bias of 4.0 V for a SAC without the PNC process, (d) Corresponding color mapping of a current image of C-AFM to define the failure criteria (blue color: normal condition, green color: marginal condition, red color: failure condition), (e) Corresponding cross-section line profile of current level with failure criteria, and (f) Schematics of C-AFM analyses for determining the cases of normal, marginal, and failed SAC structures.

SAC pad, and the etching conditions of the SAC for node separation between the gate and the SAC pad. Especially, when selective oxide etching over the gate spacer and SiN layer as a SAC stopper has been over-etched or under-etched, leakage or high resistance between the SAC and polycrystalline gate oxide occurs and induces tRDL failure.

In C-AFM analysis, the DRAM cells without resistive failure showed consistent current images such as in Figure 2b. However, in DRAM cells with resistive failures, the C-AFM image showed different current images such as in Figure 2c. To quantify the DRAM cells with failures more accurately, we mapped the current images using color categorization (Figure 2d). For the C-AFM images of the SAC surface, we categorized the status of the SAC as blue, green, or red in terms of the current level. Additionally, we defined the complete-failure threshold current level as 10 nA, the marginal current range as 10 ~ 21 nA, and the normal current threshold level as 21 nA, respectively (Figure 2e).

From these criteria, we indicated the resistive failure distributions of SAC structures in a whole wafer scale using the in-line C-AFM equipment (see the supplementary information, **Figure S1**). We scanned the 165 contact holes with a 3 μm × 3 μm sampling area for each wafer position: the center, left edge, and right edge (**Figure 3a**). The potential resistive failure ratio was calculated by the following equation:

$$\text{Potential resistive failure ratio} = (N_b + N_c)/N_t \times 100$$

N_a is the number of normal SAC structures and represents the contact holes with a current level of more than 21 nA, N_b is the number of marginal SAC structures and represents the contact holes with a current level from 10 ~ 21 nA, N_c is the number of failed SAC structures and represents the contact holes with a current level below 10 nA, and N_t is the total number of contact holes. As can be seen in **Figure 3**, in the DRAM cells of the test wafer, the failure ratios according to the wafer position were 17.6% at the center, 26.7% at the right edge, and 16.4% at the left edge, respectively. In C-AFM SAC-failure analysis, we observed how even in the same wafer, the failure ratios varied according to the position in the wafer; thus, the criteria for yield management should be determined according to the wafer position.

Study of the failure cause with TME analysis of the SAC structure. To demonstrate the good potential of C-AFM analysis, we performed a destructive TEM analysis of SAC structures to investigate the cause of the failure in SAC structures (**Figure 4**). From the TEM analysis at the center of the test wafer, we found that resistive failures between the SAC and the bottom polycrystalline Si layer did not occur in the successfully fabricated SAC structures. The crystalline SAC structures confirmed the normal resistive conditions (**Figure 4b**). However, in the abnormal cases, the morphology of the SAC structures did not exhibit contact epitaxial growth (CEG) (**Figure 4c**). Generally, the three or four SAC structures that did not produce CEG–from among the twenty SAC structures in the central region of the DRAM cell wafer–showed contact failures, which is a 15 ~ 20% failure ratio, and this value was very similar to the failure ratio of the central region of the DRAM cell wafer, 17.6%, induced by C-AFM failure analysis. Therefore, from the destructive TEM analysis, we can verify the strong potential of C-AFM analysis, and can prove the fidelity of the pass mark and failure threshold for SAC failures using C-AFM analysis.

Additionally, we analyzed the oxygen content of the TEM using EELS (Electron Energy Loss Spectroscopy) to investigate the cause of the abnormal CEG of the SAC structures. As can be seen in **Figure 4d**, the shallow silicon oxide layer was formed between the SAC and bottom Si layer. This thin silicon oxide layer hinders normal CEG, and induces the contact failure. As can be seen in the EDX (Energy-Dispersive X-ray Spectroscopy) analysis in **Figure 4e**, oxygen content in the thin silicon oxide layer was observed. In conventional PVC analysis, if this silicon oxide layer is very thin, the silicon oxide layer permits electron tunneling through the layer in the PVC analysis, which produces a faint contrast, and undermines the effectiveness of PVC failure analysis. However, C-AFM based on the current variation guarantees more accurate failure analysis than the PVC method, because the current variation shows the status of SAC conditions more precisely. In addition, by using this C-AFM analysis, we successfully fixed the criteria for SAC failures with a whole wafer scale in the in-line DRAM fabrication process.

A current-voltage (I-V) curve for invisible failure analysis to the effect of PNC process. The other important merit of the C-AFM in EFA is the possibility of analyzing physically invisible failures using the I-V curve[21–23]. Through the I-V curve of the C-AFM, the nondestructive diagnosis of the resistive level of each feature is possible. In order to verify the usefulness of C-AFM analysis, we

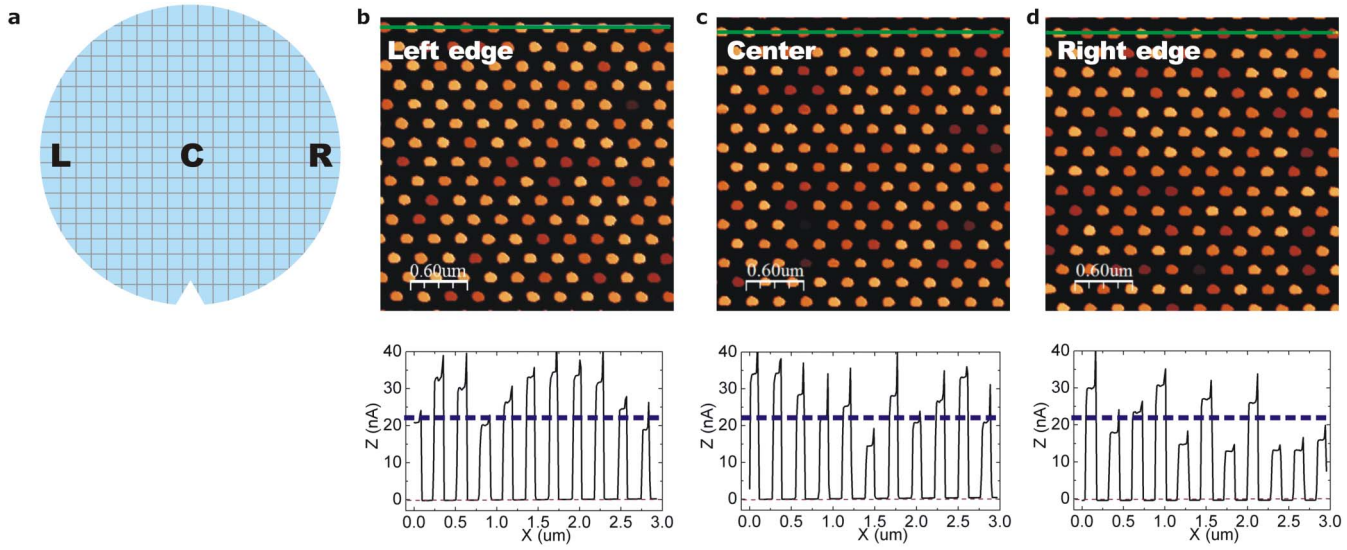

Figure 3 | C-AFM analysis images of SAC structures in a whole wafer with a bias of 4.0 V. (a) The three C-AFM measurement points according to the position in the wafer: center, left edge, and right edge of the wafer according to notch direction, (b) At the left edge of the wafer, 16.4% of the 165vcontact holes were marked as failures, (c) At the center of the wafer, 17.6% of the 165 contact holes were marked as failures, and (d) At the right edge of the wafer, 26.7% of the 165 contact holes were marked as failures.

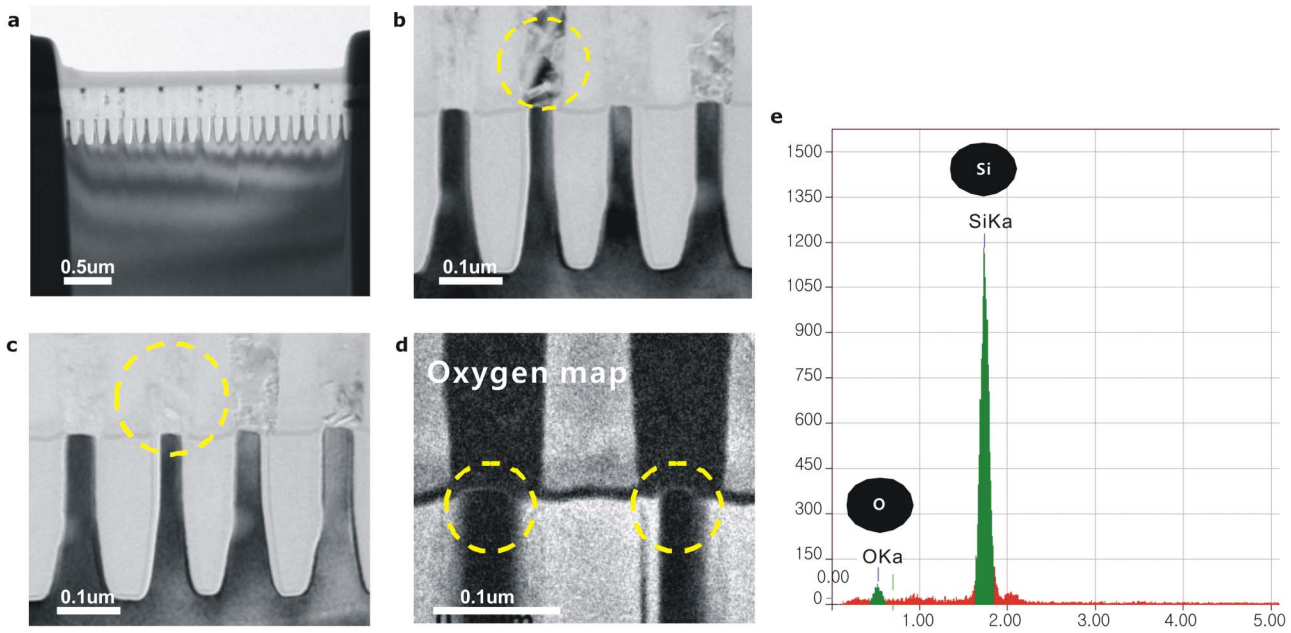

Figure 4 | TEM images and oxygen map of SAC structures on the Si bottom layer. (a) TEM image of 20 SAC structures in the central region of the DRAM cell wafer, (b) Magnified TEM image of a normal SAC structure with successful CEG, (c) Magnified TEM image of an abnormal SAC structure, (d) TEM-EELS mapping image for silicon oxide layer detection, and (e) EDX analysis on gray lines in the circled regions in (d).

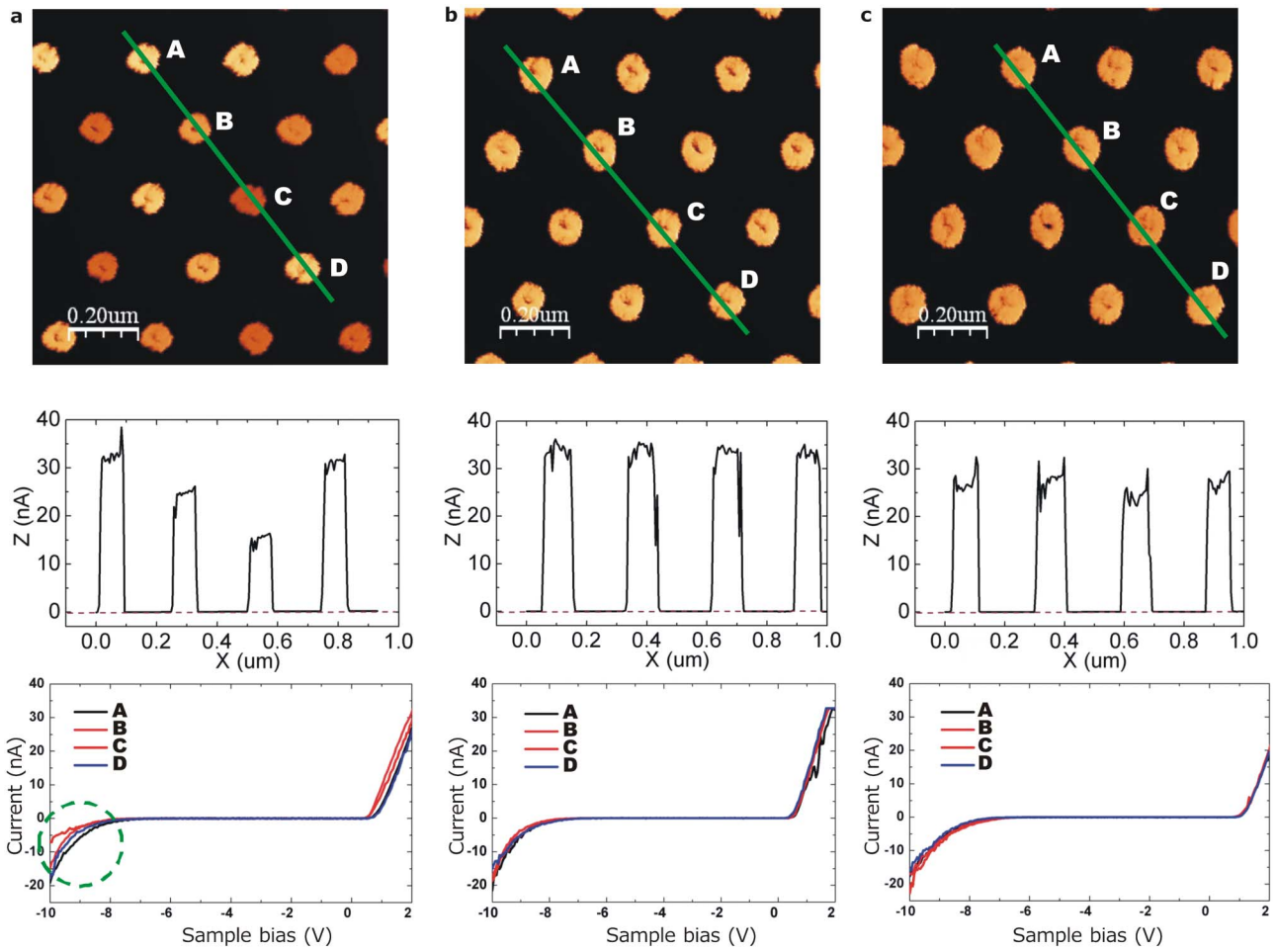

Figure 5 | Schematic illustration of I-V measurements and current image maps. (a) The case of SAC structures fabricated without the PNC process, (b) The case of SAC structures fabricated with the PNC process, and (c) The case of SAC structures fabricated with the PNC process with a 20°C higher temperature condition at 65°C.

investigated the effect of plasma native oxide cleaning (PNC) conditions on the yield of the SAC process. This successful PNC process prior to the SAC process confirms the removal of the silicon oxide layer between the SAC and Si bottom layer. As can be seen in the C-AFM image in **Figure 5a**, the SAC structures fabricated without the PNC process led to resistive failure. However, the SAC structures fabricated with the PNC process showed stable, normal resistive values (**Figure 5b**). Additionally, we analyzed the SAC structures fabricated with the PNC process at 65°C–a 20°C higher temperature condition than in the conventional PNC process. In general, the thermal conditions of the PNC process are regarded as the critical process conditions. However, in this study, we proved that the thermal condition of the PNC process is not such a critical factor when fabricating successful SAC structures (**Figure 5c**). We determined that the native silicon oxide layer on the bottom Si surface induced by the heat budget is a decisive cause of SAC failure and the PNC process is required for the removal of the silicon oxide layer.

In addition, to deduce the type of the failure more accurately, we performed I-V curve measurement analysis on the SAC using C-AFM. From the investigation of the I-V curves for the SAC, SACs without the PNC process showed different edge tails for each measurement in the negative bias region, which seems to be another marker for the classification of SAC contact failure (see the circle in **Figure 5**). Consequently, through the current map image and I-V curve analysis using C-AFM, we successfully performed a precise diagnosis of the SAC resistive failures induced by several causes, such as by the native silicon oxide layer, junction leakage, crystal defects, and gate leakage.

Discussion

We introduced a new, non-destructive diagnosis for resistive failure in SAC structures induced by a bottom oxide layer using an in-line C-AFM. Specially, we fabricated a novel, in-line C-AFM in the DRAM fabrication process, which can analyze the resistive failures and examine process variance with an exact-positioning capability across the whole wafer scale. In these in-line C-AFM analyses, we successfully suggested the accurate pass mark for resistive-failure screening in the fabrication of SAC structures and established that the cause of SAC failures is the bottom silicon oxide layer. Additionally, we found that the PNC process for the removal of the bottom oxide layer is crucial in determining the electrical quality of the SAC structures, and the native oxide layer causes electrical failure. Through the accurate pass mark for the SAC process configured by the in-line C-AFM analyses, we secured a good potential method for preventing the yield loss caused by tRDL failure in the SAC process. We expect that electrical analyses using in-line C-AFM will help the yield enhancement in the semiconductor industry, and may even help to realize the mass production of the emerging IT devices such as biosensors and organic electronic devices.

Methods

C-AFM fabrications. The in-line C-AFM module was fabricated by Nanofocus Inc. Korea. The probe used in the experiment has a force constant of 2.8 N/m and a resonance frequency of 75 kHz (CDT-FMR, Nanoworld, Switzerland). In addition, it was coated with 100-nm thick polycrystalline diamond on the tip-side for stable and non-destructive wear resistance during C-AFM operation. The electrical conductivity was measured through an electric current amplifier. This in-line C-AFM had a current noise level below 10 pA RMS roughness and a large dynamic current-detecting range from 1 pA to 10 mA.

C-AFM observations. The in-line C-AFM observation and electrical measurements were carried out in ambient conditions at room temperature. We applied positive 1 ~ 5 DC voltage on the conductive tip. Especially, we prevented the formation of the oxide layer on the wafer by applying a constant low voltage, ~4 V, during the scanning. The observation of the local current versus bias voltage (I-V) characteristics was achieved by sweeping from −10 V to +10 V. In order to produce acceptable data from the I-V curve, we measured the same area of 1.2×1.2 μm^2 by ten times, which corresponds to the pixel resolution less than 10 nm.

1. Shafai, C. *et al.* Delineation of semiconductor doping by scanning resistance microscopy. *Appl. Phys. Lett.* **64**, 342 (1994).
2. Kim, D. C. *et al.* Improvement of resistive memory switching in NiO using IrO_2. *Appl. Phys. Lett.* **88**, 232106 (2006).
3. Kim, D. C. *et al.* Electrical observations of filamentary conductions for the resistive memory switching in NiO films. *Appl. Phys. Lett.* **88**, 202102 (2006).
4. Sakai, T., Oda, N. & Yokoyama, T. Defects isolation and characterization in contact array/chain structures by using voltage contrast effect. *IEEE international Symposium.* 195–198 (1999).
5. Li-Lung, L., Gao, H. & Xiao, H. Surface effect on SEM voltage contrast and dopant contrast. *ISTFA 2009 Proceedings.* 202–207 (2009).
6. Yuan, C. & Li, S. Gray method of failure site isolation for flash memory device using FIB passive voltage contrast techniques. *ISTFA 2005 Proceedings.* 202–205 (2005).
7. Ruediger, R. Failure localization with active and passive voltage contrast in FIB and SEM. *J. Mater Sci: Mater Electron* **22**, 1523–1535 (2011).
8. Kelley, T. W., Granstrom, E. L. & Friesbie, C. D. Conducting Probe Atomic Force Microscopy: A Characterization Tool for Molecular Electronics. *Adv. Mater.* **11**, 261 (1999).
9. Sakaguchi, H. *et al.* Determination of performance on tunnel conduction through molecular wire using a conductive atomic force microscope. *Appl. Phys. Lett.* **79**, 3708 (2001).
10. Ionescu-Zanetti, C. *et al.* Simultaneous imaging of ionic conductivity and morphology of a microfluidic system. *J. Appl. Phys.* **93**, 10134 (2003).
11. Cristian, I.-Z. *et al.* Semiconductive Polymer Blends: Correlating structure with Transport Properties at the Nanoscale. *Adv. Mater.* **16**, 385 (2004).
12. Xu, D. *et al.* Electrical Conductivity of Ferritin Proteins by Conductive AFM. *Nano Lett.* **5**, 571 (2005).
13. Laura, A. & Salvatore, C. Conductive atomic force microscopy study of plastocyanin molecules adsorbed on gold electrode. *Surface Science* **598**, 68 (2005).
14. Josep, P.-L. *et al.* Supramolecular Conducting Nanowires from Organogels. *Angew. Chem. In. Ed.* **46**, 238 (2007).
15. Alexander, O., Bernd, E. & Christian, B. Conducting atomic force microscopy for nanoscale electrical characterization of thin SiO2. *Appl. Phys. Lett.* **73**, 3114 (1998).
16. Tanaka, I. *et al.* Imaging and probing electronic properties of self-assembled InAs quantum dots by atomic force microscopy with conductive tip. *Appl. Phys. Lett.* **74**, 844 (1999).
17. Todd, D. K. & Louis, E. B. Charge, Polarizability, and Photoionization of Single Semiconductor Nanocrystals. *Phys. Rev. Lett.* **83**, 4840 (1999).
18. Tan, S., Tang, Z., Liang, X. & Kotov, N. A. Resonance Tunneling Diode Structures on CdTe Nanowires Made by Conductive AFM. *Nano Lett.* **4**, 1637 (2004).
19. Chun, L., Yoshio, B. & Dmitri, G. Current Imaging and Electromigration-Induced Splitting of GaN Nanowires As Revealed by Conductive Atomic Force Microscopy. *ACS Nano* **4**, 2422 (2010).
20. Kim, J. *et al.* Exposed area ratio dependent etching in a submicron self-aligned contact etching. *J. Vac. Sci. Technol. B* **20**, 2065 (2002).
21. Wolf, P. D. *et al.* Characterization of a point-contact on silicon using force microscopy-supported resistance measurements. *Appl. Phys. Lett.* **66**, 1530 (1995).
22. Lee, J. C. & Chuang, J. H. A novel application of C-AFM: Deep sub-micron single probing for IC failure analysis. *Microelectronics Reliability* **43**, 1687–1692 (2003).
23. Lin, K., Zhang, H. & Lu, S. Conductive Atomic Force Microscopy Application for Semiconductor Failure Analysis in Advanced Nanometer Process. *ISTFA 2006 Proceedings.* 12–16 (2006).

Acknowledgements

This work was supported by Basic Research Program (2011-0018113) and Center for Advanced Soft Electronics under the Global Frontier Research Program (2011-0031635) of National Research Fund (NRF) funded by Korea government (MEST).

Author contributions

C.S. performed and designed the major part of the experiments. Y.S.K. and K.K. performed the analyses of C-AFM experiments. K.K. performed the TEM analysis. C.S., J.H.K., W.K. and Y.Y. performed the measure of C-AFM. All authors discussed the results. Y.S.K. and C.S. wrote the manuscript based on discussion with all authors. Y.S.K., S.K.L. and C.S.J. supervised the project direction.

Additional information

Supplementary information accompanies this paper at http://www.nature.com/scientificreports

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Shin, C. *et al.* Fast, exact, and non-destructive diagnoses of contact failures in nano-scale semiconductor device using conductive AFM. *Sci. Rep.* **3**, 2088; DOI:10.1038/srep02088 (2013).