MATERIALS SCIENCE

Rhombohedral-stacked bilayer transition metal dichalcogenides for high-performance atomically thin CMOS devices

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Van der Waals coupling with different stacking configurations is emerging as a powerful method to tune the optical and electronic properties of atomically thin two-dimensional materials. Here, we investigate 3R-stacked transition-metal dichalcogenides as a possible option for high-performance atomically thin field-effect transistors (FETs). We report that the effective mobility of 3R bilayer WS_2 (WSe_2) is 65% (50%) higher than that of 2H WS_2 (WSe_2). The 3R bilayer WS_2 n-type FET exhibits a high on-state current of 480 μA/μm at V_{ds} = 1 V and an ultralow on-state resistance of 1 kilohm·μm. Our observations, together with multiscale simulations, reveal that these improvements originate from the strong interlayer coupling in the 3R stacking, which is reflected in a higher conductance compared to the 2H stacking. Our method provides a general and scalable route toward advanced channel materials in future electronic devices for ultimate scaling, especially for complementary metal oxide semiconductor applications.

INTRODUCTION

Two-dimensional (2D) transition metal dichalcogenides (TMDs) have great potential applications in advanced electronic devices due to their atomic thicknesses, suitable bandgap, and high carrier mobility, which could extend Moore's law to ultimate scaling (*1*, *2*). To improve the electrical performance of TMD transistors, tremendous efforts have been devoted to increasing the mobility of monolayer channel materials, including high-quality epitaxy growth on sapphire by chemical vapor deposition (CVD), chemical doping, and dielectric engineering (*3*–*5*). However, monolayer TMDs suffer from two intrinsic limitations that constrain the realization of high-performance field-effect transistors (FETs). First, monolayer semiconductors exhibit a large bandgap due to quantum confinement, which results in a high Schottky barrier height and contact resistance (*6*). In addition, monolayer samples are susceptible to fabrication-induced damage, causing Fermi-level pinning (*7*, *8*). This strongly limits the on-state current density, especially in short-channel devices. Second, the density of states of monolayer TMDs is lower than that of their multilayer counterparts, indicating low carrier mobility (*9*). Moreover, because of the ultrathin thickness of monolayer semiconductors, carriers are highly susceptible to extrinsic disorder arising from gaseous adsorbates, which severely degrade mobility (*2*, *3*).

To address the above challenge, bilayer TMDs with a high density of states and carrier mobility have attracted tremendous interest for realizing high-performance electronic devices (*3*, *10*). It is well known that the electronic structures of 2D materials are sensitive to the stacking orientation between two monolayers (*11*, *12*). For example, the Bernal configuration of trilayer graphene is a semimetal, while the rhombohedral configuration is a semiconductor (*13*, *14*). For group 6 bilayer TMDs MX_2 (M = Mo, W; X = S, Se, Te), the most stable stacking configurations are hexagonal 2H and rhombohedral 3R, which can be scalable grown by the CVD process due to their favorable energy (*15*, *16*). Figure 1 (A and B) shows the typical atomic structures of bilayer TMD polytypes. For 2H stacking (60°), all metal (M) atoms in one layer are vertically aligned with the chalcogen (X) atoms in the other layer. In contrast, 3R stacking (0°) has a staggered arrangement, with the second layer having an in-plane shift with respect to the first layer (*17*). Previous studies have shown that 3R stacking TMDs break the inversion symmetry and exhibit a rich variety of exotic physical phenomena, including superconductivity, ferroelectricity, and valleytronics (*18*–*20*). However, the potential of 3R bilayer TMDs for electronic applications remains to be explored, and shedding light on the basic physics mechanism of carrier transport in 3R bilayer TMDs for both n- and p-type transistors could pave the way toward the realization of TMD-based complementary metal-oxide semiconductor (CMOS) circuits, which is still the missing piece in 2D electronics.

RESULTS

Here, we report an effective approach to achieve high-performance atomically thin FETs using CVD 3R-stacked bilayer WS_2 and WSe_2. We find that the effective mobility (μ_{int}) of 3R bilayer WS_2 (WSe_2) is ~65% (50%) higher than that of its 2H counterpart, which is also demonstrated by theoretical calculations. The high mobility of 3R bilayer WS_2 channels allows it to achieve a record low on-state resistance R_{on} of 1 kilohm·μm. The 3R bilayer WS_2 nFET exhibits a high on-state current (I_{on}) of 480 μA/μm at V_{ds} = 1 V, far exceeding previous results.

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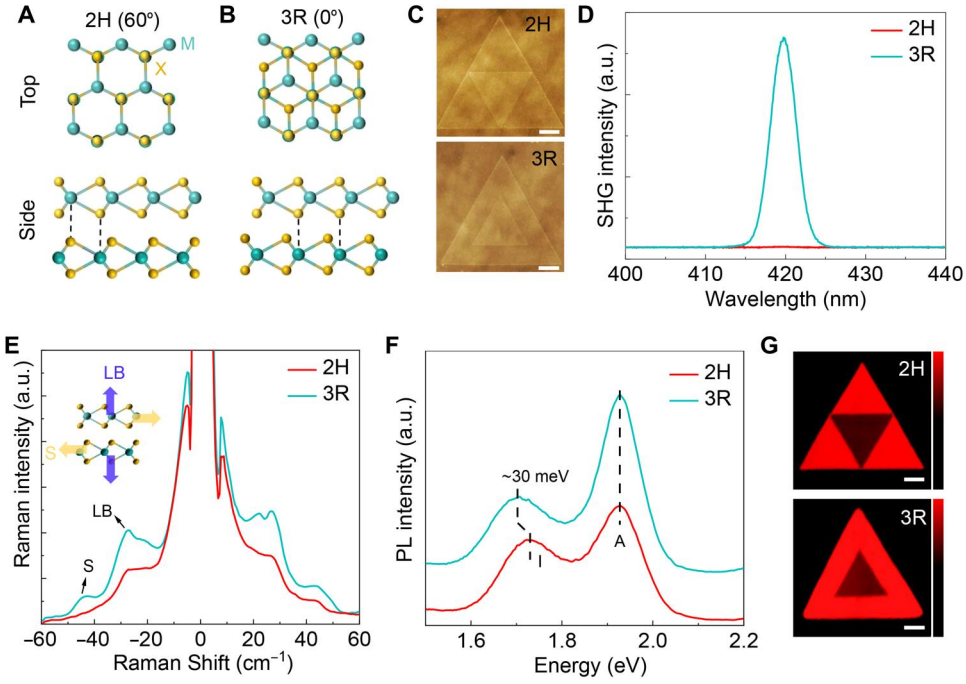

Fig. 1. The interlayer stacking of bilayer WS_2. The crystalline structure of bilayer 2H (**A**) and 3R (**B**) MX_2 polytypes. Green and yellow spheres represent tungsten and sulfur (selenium) atoms, respectively. The top (bottom) column shows the top (side) view of the crystals. (**C**) Atomic force images of bilayer WS_2 with 2H and 3R stacking. Scale bars, 2 μm. (**D**) SHG spectra of bilayer WS_2 with 2H and 3R stacking. (**E**) Experimental LF Raman spectra for 2H and 3R bilayer WS_2. The inset shows the shear and interlayer breathing vibration behaviors of bilayer WS_2. (**F**) Photoluminescence (PL) spectra of 2H- and 3R-stacked bilayer WS_2. (**G**) PL intensity mapping of bilayer WS_2 with 2H and 3R stacking. Scale bar, 2 μm. a.u., arbitrary units.

Stacking configuration

Bilayer WS_2 samples were grown by CVD on sapphire and transferred to 100-nm SiO_2/Si substrates for optical studies. Bilayer WS_2 typically shows two kinds of microscopic shapes, one with a twist angle of 60° between the two layers (2H stacking) and the other with a twist angle of 0° (3R stacking) (fig. S1). Figure 1C shows the typical atomic force microscopy (AFM) of bilayer WS_2 with 2H and 3R stacking, exhibiting a similar thickness of ~1.4 nm. Then, we use the second-harmonic generation (SHG) to distinguish the stacking order of bilayer WS_2, as shown in Fig. 1D. As expected, the SHG signal of 2H bilayer WS_2 is fully suppressed due to its inversion symmetry, while 3R bilayer WS_2 exhibits a strong SHG signal owing to its broken inversion symmetry (*21*). As shown in the inset of Fig. 1E, the low-frequency (LF) interlayer modes arise from the in-plane shear (S) and out-of-plane layer breathing (LB) phonon modes with lateral and vertical rigid layer displacement, respectively, which is exquisitely sensitive to interlayer coupling and to the number of layers (*17*). Figure 1E shows a typical Raman spectrum in the LF range (−60 to 60 cm^{-1}) for bilayer WS_2 with 2H and 3R stacking. 3R stacking exhibits two obvious peaks, which are assigned to the S mode at 27.5 cm^{-1} and the LB mode at 44 cm^{-1} (*22*). The 2H stacking has much weaker peaks at 27.5 and 44 cm^{-1}, indicating less strong interlayer coupling. In contrast to the LF Raman modes, the high-frequency modes do not exhibit stacking dependence (fig. S2). Figure 1F shows the photoluminescent (PL) spectra of bilayer WS_2 with 2H and 3R stacking. Both polytypes exhibit a prominent peak located at ~1.93 eV (peak A). In addition, the emergence of new peaks at lower energy (peak I) belongs to an indirect bandgap due to interlayer electronic coupling (*23*). The peak I energy (indirect transition) of 3R stacking is 30 meV lower than that of 2H stacking, showing stronger interlayer coupling for 3R bilayer WS_2 (*21*). This is consistent with the LF Raman mode results. Moreover, the redshifted indirect bandgap transition in 3R bilayer WS_2 is independent of temperature (fig. S3). Figure 1G shows the PL intensity mapping of the 2H- and 3R-stacked bilayer WS_2 domains recorded at 1.93 eV, further confirming the good uniformity and high quality of the bilayer WS_2.

Stacking-dependent device performance in bilayer WS_2 nFETs

Figure S4 shows a schematic of the transfer length method (TLM) structure in this work, and the contact length and the channel width are 1 μm. Figure 2A shows the representative transfer characteristics of back-gated bilayer WS_2 FETs with 2H and 3R polytypes on 100-nm SiO_2 gate dielectrics at a 2-μm channel length (L_{ch}). Both devices show n-type behaviors and high on/off ratios of 10^9. The field-effect mobility (μ_{FE}) of bilayer WS_2 was extracted using the equation $\mu_{FE} = g_m L_{ch}/WC_{ox}V_{ds}$, where g_m, C_{ox}, and V_{ds} are the transconductance, gate oxide capacitance per unit area of the dielectric layer, and drain voltage, respectively (*10*). The μ_{FE} of 2H and 3R bilayer WS_2 FETs is calculated to be 17 and 25 $cm^2\ V^{-1}\ s^{-1}$, respectively. The corresponding output characteristics of the two devices are shown in Fig. 2B. The drain current of 3R bilayer WS_2 is more than 90% higher than that of the 2H devices at similar carrier densities. Similar behavior was found for 1- and 0.5-μm devices (fig. S5). To exclude the effect of oxide substrates, the transfer characteristics of 2H and 3R WS_2 FETs on 6-nm HfLaO gate dielectrics are also shown in Fig. 2C, with positive threshold voltages and on/off

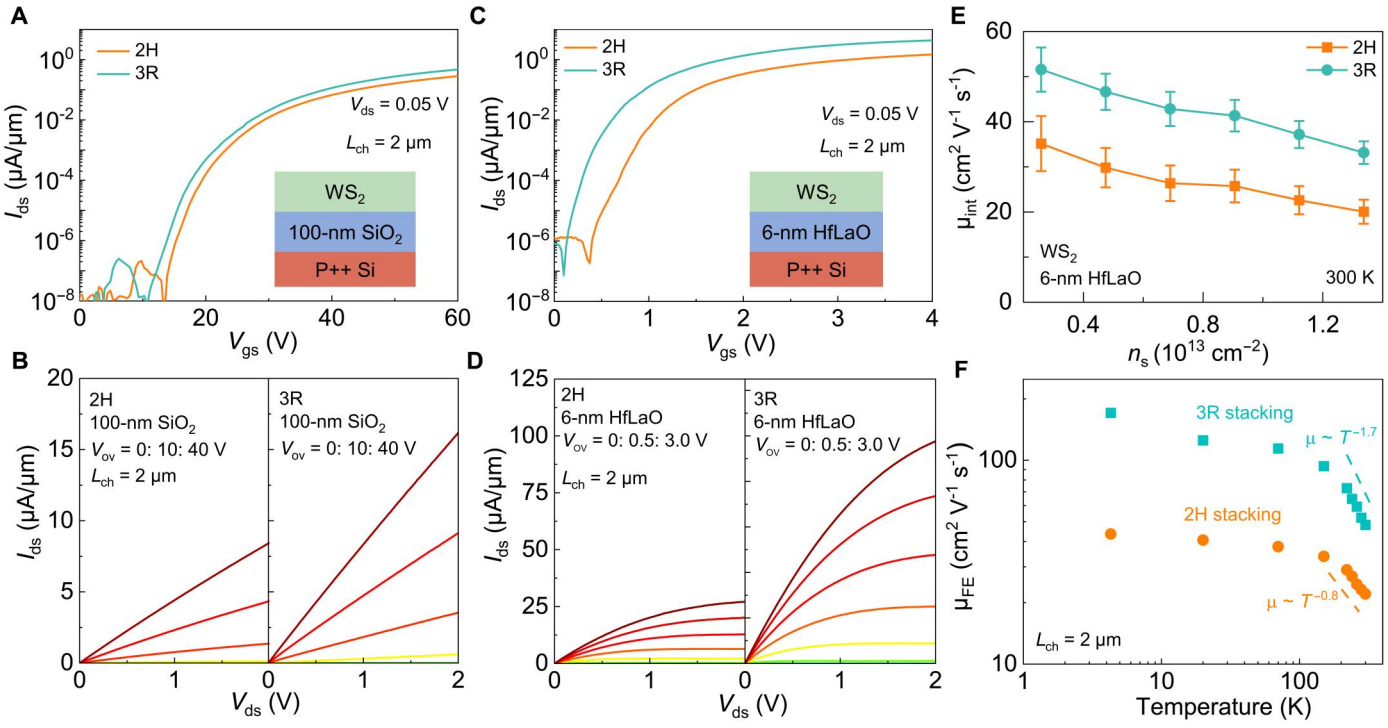

Fig. 2. Device characterization of 2μm-long bilayer WS_2. (**A**) Transfer characteristics for bilayer WS_2 FETs with 2H and 3R stacking at V_{ds} = 0.05 V. The gate dielectrics are 100-nm SiO_2. The channel length and width are 2 and 1 μm, respectively. (**B**) Corresponding output characteristics of bilayer WS_2 FETs in (A). V_{OV} ranges from 0 to 40 V with steps of 10 V. (**C**) Transfer characteristics for bilayer WS_2 FETs with 2H and 3R stacking at V_{ds} = 0.05 V. The gate dielectrics are 6-nm HfLaO. (**D**) Corresponding output characteristics of bilayer WS_2 FETs in (C). V_{OV} ranges from 0 to 3 V with steps of 0.5 V. (**E**) Effective mobility (μ_{int}) versus channel carrier density for bilayer WS_2 with 2H and 3R stacking at 300 K. (**F**) Extracted μ_{FE} of 2H- and 3R-stacked bilayer WS_2 as a function of temperature from two-probe measurements. The solid lines are fits to the model $\mu_{FE} \sim T^{-\gamma}$ in the 200 to 300 K temperature range.

ratios up to 10^8 (5). As expected, the μ_{FE} of 3R WS_2 is as high as 48 cm^2 V^{-1} s^{-1}, which is 2.7 times higher than that of 2H WS_2. Figure 2D compares the output drain current of both devices with an L_{ch} of 2 μm, with strongly improved I_{ds} for 3R WS_2 transistors up to 97 μA/μm at V_{ds} = 2 V and V_{ov} = 3 V (overdrive voltage $V_{OV} = V_{gs} - V_t$, V_t is the threshold voltage). Figure S6 shows the statistical distribution of I_{on} from 31 2H-stacked WS_2 and 33 3R-stacked WS_2 FETs with 6-nm HfLaO. The I_{on} values of the 2H and 3R WS_2 transistors are 24 ± 3 and 40 ± 3.5 μA/μm, respectively. To exclude the effect of contact resistance on carrier mobility, we extract effective mobility (μ_{int}) using $\mu_{int} = 1/(qn_sR_{sh})$, where q is the elementary charge, n_s is the carrier concentration, and R_{sh} is the sheet resistance (*24*). Sheet resistance (R_{sh}) is extracted from the slope of the TLM plots (figs. S7 and S8). Figure 2E compares μ_{int} versus carrier density for bilayer WS_2 with two different stackings. The μ_{int} of 3R-stacked WS_2 is 65% higher than that of 2H-stacked WS_2 at $n_s = 1.33 \times 10^{13}$ cm^{-2}. μ_{int} decreases with increasing n_s, probably due to the increased electron scattering with the oxide surface roughness (*24*). Figure 2F shows the temperature dependence of the field-effect mobility μ_{FE} for the 2H and 3R devices. The drop in mobility from 150 to 300 K can be attributed to charged-impurity scattering that dominates at high temperatures, and the temperature dependence roughly follows the power law $\mu_{FE} \propto T^{-\gamma}$ (Fig. 2F) (*25*). The exponent γ is found to be close to ~0.8 and ~1.7 in the 2H and 3R devices, respectively. These results show that 3R WS_2 is a more promising channel material to achieve high-performance nanoscale transistors for next-generation electronics.

Short-channel bilayer WS_2 nFETs

We also fabricated short-channel devices to demonstrate the performance potential of the 3R WS_2 transistors, as illustrated in Fig. 3A. The transistor consists of 40-nm Ni as the contact metal, 3R bilayer WS_2 as the channel material, and 6-nm HfLaO as the dielectric. The device has a channel width of 1 μm for all channel lengths. The cross-sectional high-resolution transmission electron microscopy (HRTEM) image shown in Fig. 3B reveals that uniform bilayer WS_2 is on the 6-nm HfLaO gate dielectrics with a thickness of ~1.4 nm, which is consistent with the AFM measurements. L_{ch} is measured to be 50 nm in this device. The magnified HRTEM image of the Ni/WS_2 contact region shows good adhesion of Ni to the bilayer-WS_2 channel with no noticeable damage from the metal deposition process, indicating good contact quality (fig. S9). Figure 3C shows the transfer characteristics of a 50-nm-long 3R WS_2 device at 300 and 4.3 K, showing a high on/off ratio over 10^8 at V_{ds} = 1 V and nearly zero drain-induced barrier lowering. The excellent short-channel behavior is mainly attributed to its relatively large bandgap, ultrathin channel, and ultrathin gate dielectric. Figure S10 shows the transfer characteristics obtained using dual gate voltage sweeps for 3R bilayer WS_2 devices with L_{ch} = 50 nm. The clockwise hysteresis window is mainly attributed to charge trapping near the interface of the channel and the gate dielectric,

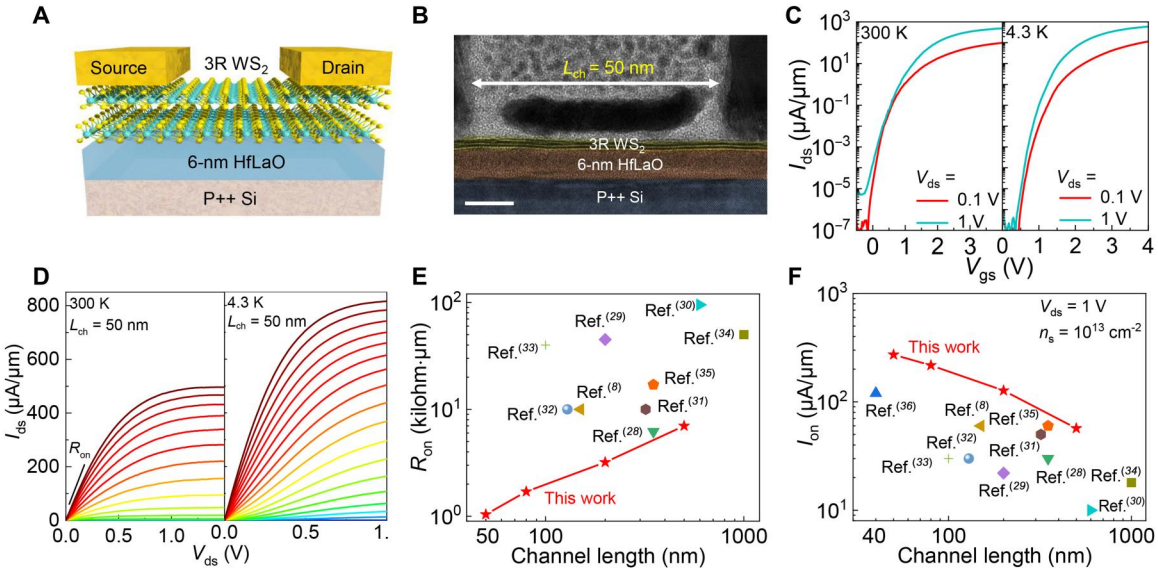

Fig. 3. Device characterization of short-channel 3R-stacked bilayer WS_2 nFETs. (**A**) Schematic illustration of a bilayer WS_2 device with a 6-nm HfLaO insulator in this work. (**B**) TEM image of a 50-nm bilayer WS_2 transistor with Ni contact. Scale bar, 10 nm. (**C**) Transfer characteristics of 3R-stacked bilayer WS_2 devices with a channel length of 50 nm at 300 and 4.3 K. (**D**) Corresponding output characteristics of bilayer WS_2 FETs in (C). The linear output characteristics of the channel current at low V_{ds} at 4.3 K indicate that quasi-ohmic contacts are formed using the conventional process of e-beam–evaporated Ni metal. V_{gs} is from 0 to 4 V with steps of 0.25 V. Benchmark of on-state resistance R_{on} (**E**) and on-state current I_{on} (**F**) as a function of channel length for CVD WS_2 transistors at room temperature. The carrier density is fixed at $n_s = 10^{13}$ cm^{-2}.

which can be further improved by annealing or surface passivation. The corresponding output characteristics at 300 and 4.3 K are shown in Fig. 3D. It is evident that the 50-nm WS_2 device exhibits a high maximum I_{ds} of 480 μA/μm under V_{ds} = 1 V with good saturation behavior. Meanwhile, an ultralow on-state resistance R_{on} of 1 kilohm·μm at 300 K is obtained for the 50-nm WS_2 device. By decreasing the temperature to 4.3 K, the drain current increases to 815 μA/μm under V_{ds} = 1 V without obvious Schottky barrier behavior, indicating excellent contact quality between Ni and bilayer WS_2 (*26*, *27*). It is well known that the extraction of device parameters (such as carrier mobility and contact resistance) is usually associated with uncertainties or errors (*2*). Therefore, we chose figures of merit of R_{on} and I_{on} to provide a more direct and reliable method to evaluate the potential of 3R bilayer WS_2 (*2*, *24*). Figure 3 (E and F) compares the R_{on} and I_{on} of WS_2 transistors in the literature with our results. 3R bilayer WS_2 transistors exhibit the lowest R_{on} of 1 kilohm·μm and the highest I_{on} at V_{ds} = 1 V and $n_s = 10^{13}$ cm^{-2}, among CVD WS_2 to the best of our knowledge (*28*–*36*).

Physical origin of the stacking-dependent device performances

To understand the physical origin of the stacking-dependent device performances, we investigate the two different stackings by means of a multiscale approach, which combines density functional theory (DFT) calculations with electron transport simulations using the nonequilibrium Green's function formalism. Figure 4 (A and B) reports the DFT band structure and the projected density of states (PDOS) for bilayer WS_2 with 2H and 3R stacking configurations, respectively, obtained by means of the Quantum-Espresso suite including spin-orbit coupling (SOC) (*37*). For the 3R stacking, band splitting can be observed for both valence and conduction bands at the K and Q points in the Brillouin zone. This is not observed in the 2H case. The band splitting is also reflected in the PDOS, which is different for the two stackings, particularly in the energy range close to the minimum of the conduction band. To quantitatively estimate the contribution of the stacking order to band splitting, we repeat the band structure calculations without SOC and measure the band splitting induced by interlayer coupling (*38*, *39*). In the insets of Fig. 4 (A and B), we show a zoom of the bottom of the conduction bands without SOC. For the 2H stacking, we obtain an interlayer coupling of Δ < 2 meV, while for the 3R case Δ = 61 meV, thus confirming the stronger interlayer coupling already found experimentally for the 3R stacking. To quantify the effect of interlayer coupling on the transport characteristics of the different WS_2 bilayer-based devices, we compute the vertical transmission across the layers for the two different stacking configurations considering several overlapping lengths for each stacking (fig. S11). In Fig. 4C, we computed the vertical conductance averaged over the different overlapping lengths used for each stacking. We can clearly observe that the 3R stacking has a higher conductance, specifically in the energy range close to the minimum of the conduction band, as reported in the inset of Fig. 4C.

On the basis of these results, we propose the transport mechanism reported in Fig. 4D to explain the higher mobility for 3R bilayer WS_2 devices compared to 2H devices. In Fig. 4D, we depict two different paths for the current in the top-contacted bilayer WS_2 device: (i) In path (1), carriers are injected from the source, go through the top layer, and are collected at the drain; (ii) in paths (2) to (4), carriers are injected from the source, jump from the top layer to the bottom layer (2), flow through the bottom layer (3), and lastly are collected at the drain by jumping back from the bottom layer to the top layer (4). Because the in-plane transport in the top (1) and bottom (3) layers is independent of the stacking configuration, the only difference can arise from vertical transport

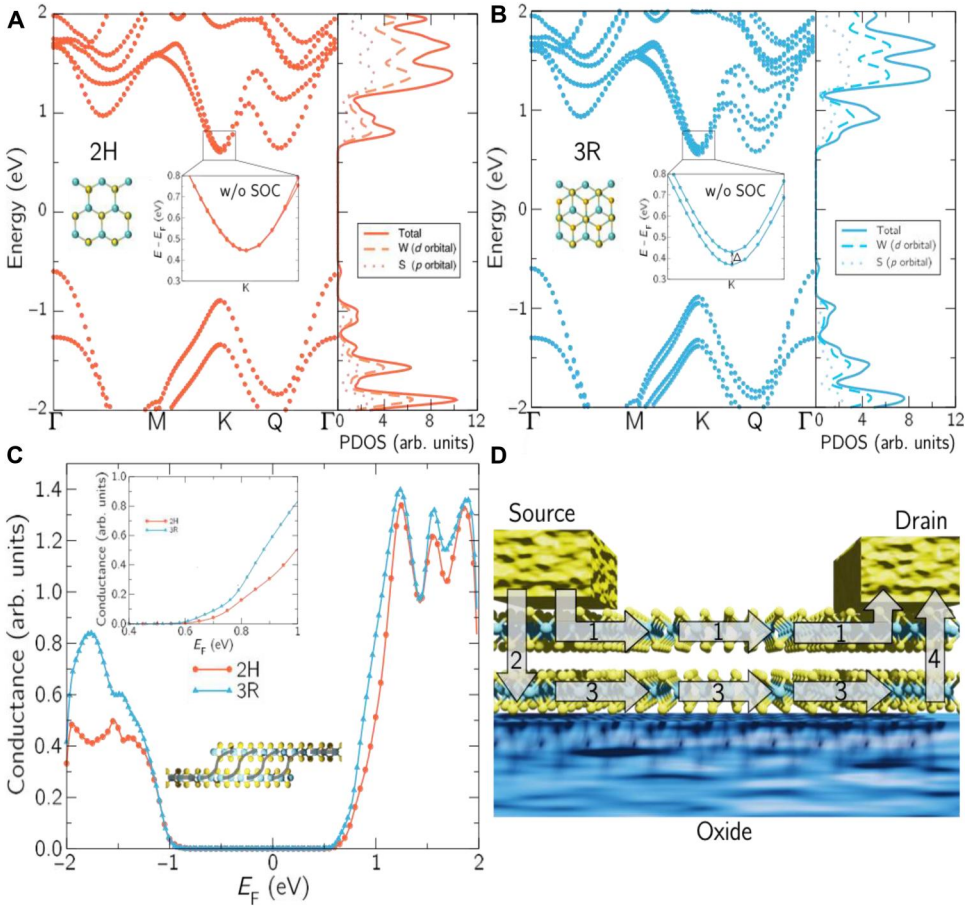

Fig. 4. Theoretical calculations of the transport in bilayer WS_2 with two different stackings. Band structure with the inclusion of SOC and PDOS for the 2H (**A**) and 3R (**B**) stackings. In the insets of (A) and (B), a sketch of the simulated crystalline structure and a magnified view of the bottom of the conduction band around K without SOC are shown. (**C**) Average conductance as a function of the Fermi level for the two different stackings. (**D**) Sketch of the device depicting the possible path of the current from source to drain.

(2) and (4). In this regard, our DFT and transport calculations have demonstrated a stronger interlayer coupling and a higher vertical conductance across the layers for the 3R configuration. In addition, all the devices reported in the present work have a back gate that modulates the carrier concentration in the channel, implying that more carriers are expected to be induced in the bottom layer, closer to the gate, than in the top layer. Having more carriers in the bottom layer implies more current passing through it, thus having more current in the paths (2) to (4) than in path (1).

Stacking engineering for bilayer WSe_2 pFETs

Aside from n-type bilayer WS_2, high-performance p-type devices based on TMDs channel materials with high drain current are of great importance for future CMOS applications. Therefore, we further investigated the electrical properties of p-type bilayer WSe_2 with different structures grown by CVD on SiO_2 substrates (see Materials and Methods for details). We can determine twist angles of 60° (2H stacking) and 0° (3R stacking) of bilayer WSe_2 by comparing the orientation between the first and second monolayers in optical images (fig. S12). The thickness of bilayer WSe_2 was identified by AFM with a typical thickness of ~1.6 nm (fig. S13). We further explore the crystal structures of bilayer WSe_2 with the 2H and 3R phases using LF Raman mode, and the results are shown in Fig. 5A. The 2H stacked bilayer WSe_2 shows a sharp shear mode at 16.2 cm^{-1} and a broad breathing mode at 28 cm^{-1}, consistent with previous works (*22*). The LB mode (26.2 cm^{-1}) and shear mode (15 cm^{-1}) of the 3H phase are lower in frequency than those of the 2H phase, indicating that the 3R layers are less strongly bound than the 2H layers. Moreover, the breathing-mode peak intensity is ~76% (~500%) of the shear-mode intensity for the 2H (3R) WSe_2 bilayers. In addition, by analyzing the temperature-dependent PL spectra of bilayer WSe_2, the peak B energy (indirect transition) of 3R stacking is always lower than that of 2H stacking from 300 to 100 K, showing stronger interlayer coupling for 3R bilayer WSe_2 (fig. S14) (*21*). Figure 5B presents the transfer characteristics of 2H- and 3R-stacked bilayer WSe_2 transistors on 100nm SiO_2 with a channel length of 2 μm. The maximum I_{ds} of 2H and 3R WSe_2 are 110 and 185 μA/μm under $V_{OV} = -70$ V and $V_{ds} = -2$ V, respectively. The statistical distribution of I_{on} from 2H- and 3R-stacked WSe_2 FETs with 100 nm SiO_2 is shown in fig. S15, indicating a higher current for the devices with 3R stacking. The corresponding transfer characteristics at $V_{ds} = -0.05$ V are shown in Fig. 5C. Both devices show high on/off ratios of ~10^8 and p-type transport behavior. Figure 5D compares μ_{int} versus carrier density for bilayer WSe_2

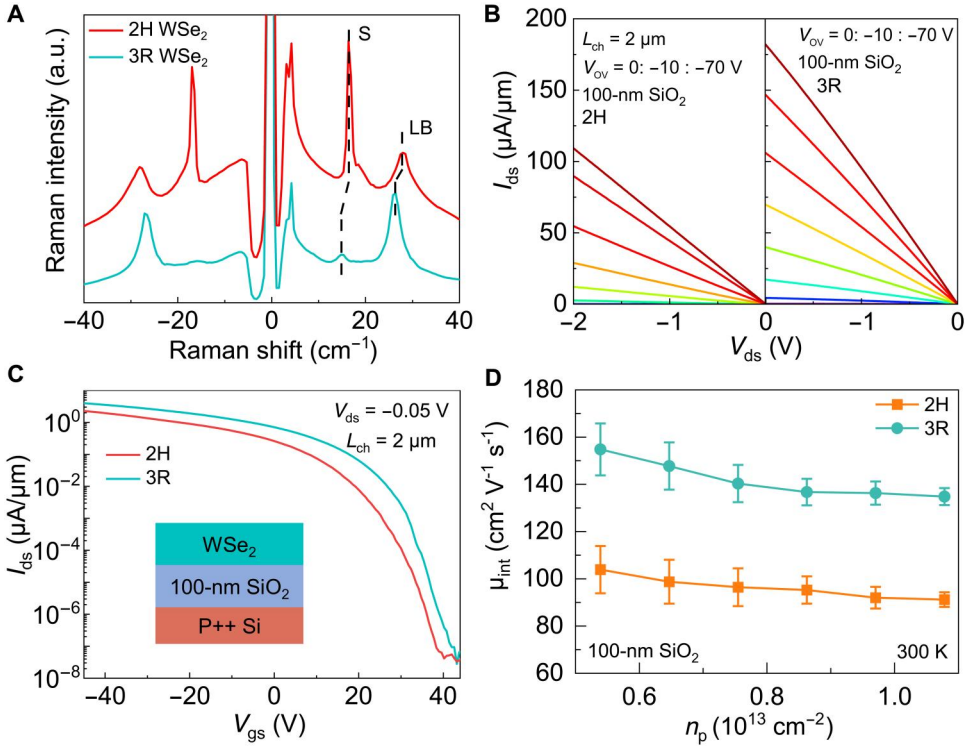

Fig. 5. Device characterization of bilayer WSe_2 pFETs. (**A**) Experimental LF Raman spectra for 2H and 3R bilayer WSe_2. (**B**) Output characteristics of bilayer WSe_2 FETs with 2H and 3R stacking. The gate dielectrics are 100-nm SiO_2. (**C**) Corresponding transfer characteristics for bilayer WSe_2 FETs at $V_{ds} = -0.05$ V. (**D**) Effective mobility (μ_{int}) versus n_p for bilayer WSe_2 with 2H and 3R stacking at 300 K.

with two different stackings. The μ_{int} of 3R-stacked WSe_2 is ~50% higher than that of 2H-stacked WSe_2 at $n_p = 1.0 \times 10^{13}$ cm^{-2}. This improvement is mainly attributed to the vertical transmission calculations evidencing a higher transmission in the valence band (p-type) for the 3R stacking compared to the 2H (*40*). The TLM study also shows lower contact resistance and sheet resistance for bilayer WSe_2 with 3R stacking (figs. S16 and S17).

DISCUSSION

In conclusion, we have carried out a comprehensive experimental and theoretical investigation of the electrical properties of CVD-grown 2H and 3R bilayer TMD atomic layers. The 3R stacking with broken inversion symmetry exhibits higher carrier mobility due to a stronger interlayer coupling compared to the 2H stacking configuration, which substantially enhances the vertical conductance. Contrary to an earlier study on bilayer MoS_2 (*3*), we demonstrate substantial improvement in mobility and I_{on} for n-type WS_2 and p-type WSe_2 transistors using the 3R phase, which is consistent with other studies (*41*, *42*). Our results show that 3R-stacked bilayer TMDs offer a promising pathway toward realizing high-performance nanoscale transistors for CMOS applications, which calls for efforts to obtain large-area bilayer samples with pure 3R phase. It could be realized in the foreseeable future after in-depth understanding of the fabrication technology and developing new growth mechanisms.

MATERIALS AND METHODS

WS_2 and WSe_2 growth by CVD

WS_2 and WSe_2 were grown on sapphire and SiO_2/Si substrates under low pressure in a one-zone CVD system, respectively. Before growth, the sapphire substrates were cleaned sequentially with acetone, isopropanol, and deionized water in an ultrasonic environment. The SiO_2 substrates were cleaned with a standard RCA-1 process. A sapphire or SiO_2 substrate was faced down and placed on a corundum boat filled with 40 mg of WO_2 (99.98%; Sigma-Aldrich) and 1.5 mg of KCl (99.999%; Sigma-Aldrich) mixed powder. The 200 mg of S (99.99%; Sigma-Aldrich) or Se (99.99%; Sigma-Aldrich) powder was placed in a quartz boat loaded upstream of the furnace. The CVD furnace was heated and maintained at 890°C for 15 min. In the growth stage, Ar/H_2 (105/10 sccm) was used as the carrier gas.

Material characterization

Raman and photoluminescence characterizations of WSe_2 and WS_2 were obtained by confocal Raman spectroscopy (LabRAM HR800) with a 532-nm laser wavelength. AFM (Shimadzu SPM-9700) was used to measure surface topology. The SHG experimental system mainly includes a femtosecond laser (Coherent Mirra 900F), electron multiplying charge-coupled device (Andor Newton 970), and spectrometer (Andor 500i). Scanning electron microscopy (SEM; SU8010) and transmission electron microscopy (TEM; Thermo Fisher Scientific Tecnai F20) were used to observe the structure of the devices.

Device fabrication and measurements

All devices based on WS_2 and WSe_2 were fabricated side by side with the same fabrication process and measured at the same time for a valid comparison. WSe_2 pFETs were fabricated directly without transfer based on as-grown CVD WSe_2 on 100-nm SiO_2/Si substrates. Bilayer WS_2 was transferred onto a 100-nm SiO_2/Si or 6-nm HfLaO/Si substrate using the heat release tape/poly(methyl methacrylate) (PMMA)–assisted transfer method. Then, lithography and inductively coupled plasma were used to define the channel region. The substrates with etched WS_2 or WSe_2 were annealed at 300°C in an argon atmosphere to remove any PMMA residues. Next, e-beam–evaporated 20/60-nm Ni/Au (Pt/Au) was deposited for the source/drain (S/D) contact metal of WS_2 (WSe_2). Last, the WSe_2 devices were annealed in an Ar/O_2 atmosphere for 2 hours at 300°C. All electrical measurements were measured using a semiconductor parameter analyzer (Agilent B1) with a Lakeshore probe station in a vacuum.

Theoretical calculations

DFT calculations were performed with the Quantum-Espresso suite (*37*). We use projector augmented-wave pseudopotentials within the Perdew-Burke-Ernzerhof approximation for the exchange-correlation functional. The bilayer WS_2 geometry was relaxed until all forces were smaller than 0.051 eV/Å. Grimme-D2 correction is used to include van der Waals forces during relaxation. For the electronic structure calculations, we use an energy convergence threshold of 10^{-6} Ry and an $8 \times 8 \times 1$ gamma-centered k-mesh grid. The calculations are carried out in the presence and absence of spin-dependent interactions, as explained in the main manuscript. The wannierization procedure was performed with the Wannier90 code on an $8 \times 8 \times 1$ k-mesh grid projecting on the d-orbitals of W and p-orbitals of S (*43*). Transport simulations were performed using NanoTCAD ViDES (*44*), which exploits the nonequilibrium Green's function formalism. The multiscale procedure used for computing the transmission coefficients for the vertical transport across the bilayer is taken from (*40*).

Supplementary Materials

This PDF file includes:

Figs. S1 to S17

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