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Valley-engineered ultra-thin silicon for high-performance junctionless transistors

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Extremely thin silicon show good mechanical flexibility because of their 2-D like structure and enhanced performance by the quantum confinement effect. In this paper, we demonstrate a junctionless FET which reveals a room temperature quantum confinement effect (RTQCE) achieved by a valley-engineering of the silicon. The strain-induced band splitting and a quantum confinement effect induced from ultra-thin-body silicon are the two main mechanisms for valley engineering. These were obtained from the extremely well-controlled silicon surface roughness and high tensile strain in silicon, thereupon demonstrating a device mobility increase of ~500% in a 2.5 nm thick silicon channel device.

Wearable electronics have received huge attention as the next wave of electronic products. The demand for wearable or flexible electronic devices has encouraged researchers to look into two-dimensional (2D) materials such as graphene and transition metal dichalcogenide (TMD) materials such as molybdenum disulfide[1–4]. These materials can be used as channel materials for field effect transistors (FET) or sensors by exploiting their thin nature. Graphene, the representative 2D material, shows high mobility however it could be used in limited application due to its zero bandgap property[1,2]. TMD materials such as MoS_2 could be a good candidate to demonstrate flexible electronics and it shows reasonable device performance[3]. However, TMD channel devices have shown inferior performance than silicon channel devices in terms of sub-threshold swing, channel mobility and interface state density. Black phosphorus has a great potential for the future electronics which shows acceptable on/off ratio and high mobility[5]. However, material synthesis in a large scale with good uniformity as well as the low defect density required for electronic device applications is still a challenge. Silicon can provide a practical solution to circumvent such problems, as an industrially mature technology is in place for silicon based electronics[6–9]. Extremely thin silicon show good mechanical flexibility because of their 2-D like structure and enhanced performance by the quantum confinement effect[10–15]. Here, we experimentally demonstrate a junctionless FET revealing a room temperature quantum confinement effect (RTQCE) by using a valley-engineered 2D-like silicon. Strain-induced band splitting[16–18] and a quantum confinement effect induced from ultra-thin-body silicon[19–21] are the two main mechanisms for valley engineering. The term "valley engineering" has been used to express the control of sub-band separation energy to achieve higher performance of silicon device[22,23]. Low effective mass of the carrier in the transport direction is achieved, together with suppression of scattering-inducing components, resulting in enhanced device performance. These advantages were obtained by careful control of the silicon surface roughness and complexity, and high tensile strain in silicon, thereupon demonstrating a device mobility increase of ~500% in a 2.5 nm thick silicon channel device.

Results

In order to make ultra-thin-body silicon, a thinning process was conducted by repetitive low temperature oxidation of silicon at 750 °C, followed by wet chemical etching of the oxide. Silicon was thinned to 2.5, 5, and 7 nm. The surface of the silicon was carefully controlled so that root mean square (RMS) surface roughness of around ~0.13 nm could be achieved. Tight control of the surface roughness is important to maintain the 2D density of state (DOS) of silicon since a RTQCE can only be observed in ultra-thin-body silicon with a sharp DOS when the RMS surface roughness is smaller than 0.4 nm[10].

Figure 1a,b respectively present a schematic drawing and a high-resolution TEM image of the fabricated silicon junctionless FET. The TEM image shows that a 2.5 nm silicon is uniformly formed in the channel region. The device is designed to be operated using a back gate electrode as the main controlling gate, while the front

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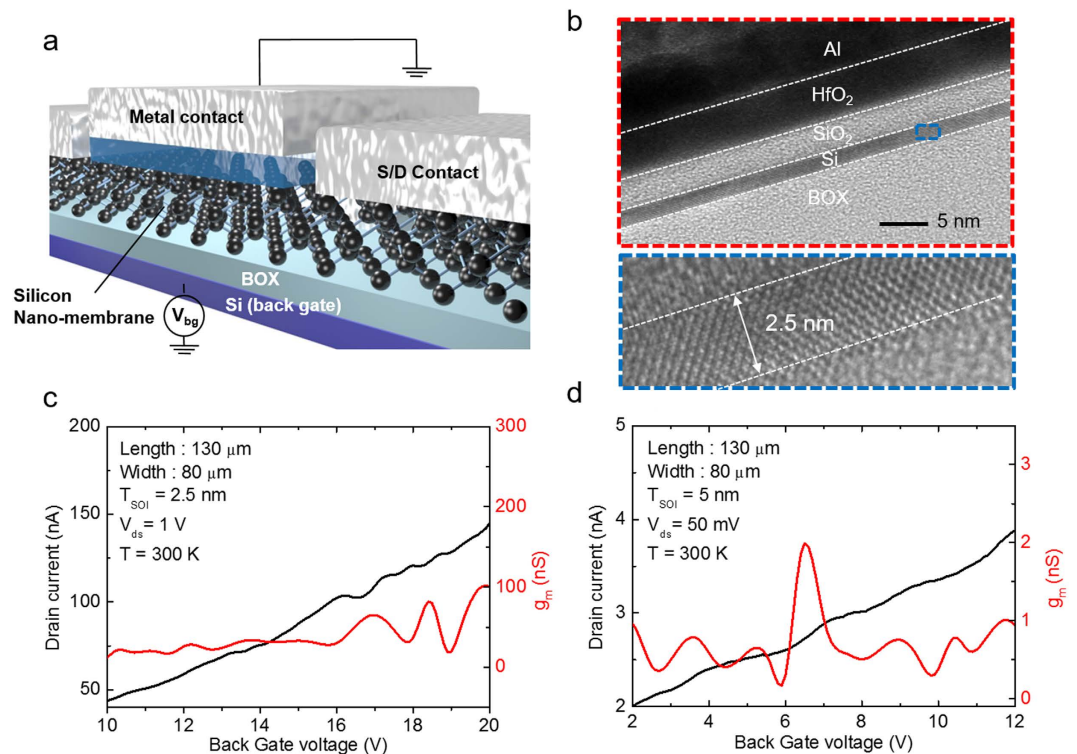
Figure 1. (**a**) Schematic drawing of the device structure. (**b**) TEM image of the fabricated device. It shows an ultrathin silicon layer with excellent thickness uniformity. The magnified image shows a 2.5 nm thick single crystal silicon. (**c**) Transfer characteristics of a silicon transistor when the silicon thickness is 2.5 nm. The drain current shows step-like increments and the trans-conductance is oscillated, implying RTQCE. (**d**) Transfer characteristics of a silicon transistor when the silicon thickness is 5 nm. The device also reveals RTQCE.

gate stack (metal electrode and high-K gate dielectric) is used only for passivation, and for this the front gate is grounded during device operation. Such operation is meant to minimize the effect of the access resistance that exists due to the physical gap between the front gate and the source/drain region where the silicon resistance is not modulated by the front gate. The accumulation mode conduction mechanism by adopting a junctionless FET structure was used. The silicon was moderately n-type doped, for both the channel and source/drain region. Figure 1c,d show the transfer characteristics of the fabricated device under a bias of $V_D = 1\,V$ at room temperature when the body thicknesses is 2.5 nm and 5 nm, respectively. Step-like increments of the drain current are observed throughout the whole sweep range of the gate voltage. Oscillation of the trans-conductance is clearly observed, indicating that RTQCE occurs. Since the body thicknesses of the devices are thinner than the thermal de Broglie wavelength of silicon at room temperature, that is, 12 nm, RTQCE is clearly observable[10].

To investigate the governing mechanism of RTQCE in the silicon, the lattice structure of the ultra-thin silicon was carefully analyzed using TEM. The ultra-thin silicon shows up to 2.2% tensile strain when the thickness of the silicon is thinned to 2.5 nm. This high tensile stress is attributed to our thinning process, which involves repetitive low-temperature (750 °C) oxidation of silicon and stripping the silicon dioxide layer. Silicon dioxide formed by the low-temperature oxidation process has high viscosity. Stress caused by the oxidation process is proportional to the product of the growth rate and oxide viscosity. Successive oxidation below the glass transition temperature, which is 960 °C, results in high biaxial tensile strain without viscoelastic relaxation[24,25]. Tensile strain is also in the transport direction because strain is generated biaxially. Strain in silicon was quantified through the sequence shown in Fig. 2a,d. First, high-resolution TEM images of 2.5 nm, 6.5 nm, and 22 nm thick silicon were obtained and an image of the bulk silicon was captured as a reference. A Fast Fourier Transform (FFT) was conducted, followed by applying a mask to the FFT image. To reconstruct the atomic arrangement for calculating the lattice distance, an inverse FFT was conducted. The lattice distance was acquired via the white line in Fig. 2d and was revealed to be 0.3832 nm for the 22 nm thick silicon. The same process was performed for the 2.5 nm and 6.5 nm thick silicon, as well as the bulk silicon, yielding a lattice distance of 0.3916 nm, 0.3858 nm, and 0.3831 nm, respectively. As a result, 2.2% tensile stress in [110] the transport direction was measured in the 2.5 nm thick silicon. This amount of strain in the silicon is much higher than that of the commercial strained silicon wafer by using a SiGe strained layer (about 1%)[26]. Both the nature of the ultra-thin-body (2.5 nm) and the high tensile strain (2.2%) lead to splitting valleys of the silicon energy band, which suppresses inter-valley scattering. In addition, this strain-induced valley splitting also has advantages in terms of maintaining low transport mass since most electrons are occupied in a two-fold valley of the strained ultra-thin-body silicon at room temperature[8,19].

Figure 3 shows the surface roughness measured by non-contact mode AFM. AFM was performed on the top surface of thinned silicon on a SOI wafer over an area of $10\,\mu m \times 10\,\mu m$. The RMS values of the surface
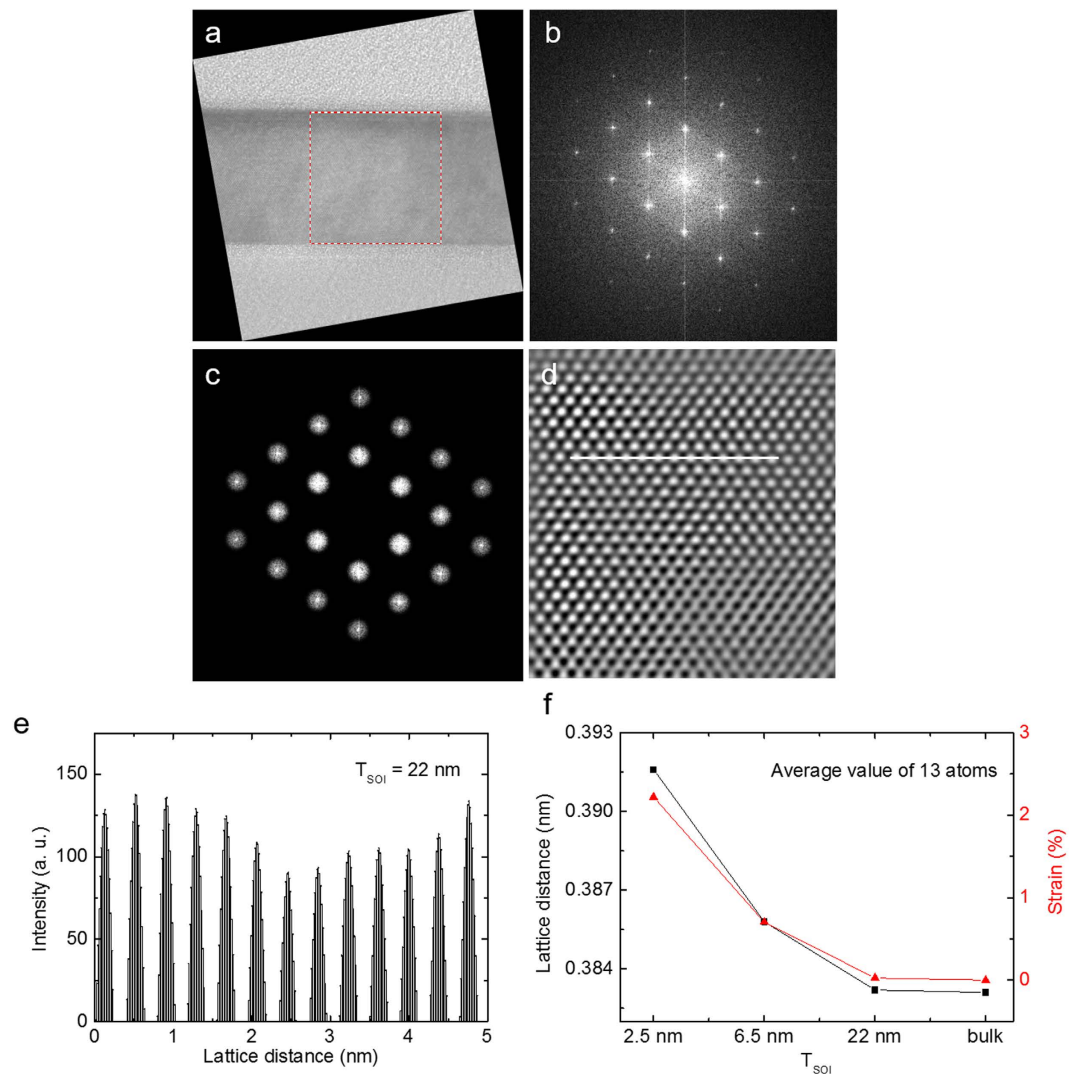
Figure 2. (**a**) High-resolution TEM image of a 22 nm thick top silicon. (**b**) FFT image (**c**) A mask was applied to the FFT image to utilize the information. (**d**) A reconstructed inverse FFT image was used to analyze the lattice distance in the silicon. (**e**) Intensity of lattice distance from the inverse FFT image. (**f**) Extracted lattice distance versus silicon thickness. The calculated tensile strain along the transport direction is plotted together against the silicon thickness.

roughness after 1, 2, and 3 iterations of the thinning process (low temperature oxidation and stripping the oxide) are 0.164 nm, 0.153 nm, and 0.138 nm, respectively, which are almost identical to the RMS roughness of graphene, a 2D material[27]. The height histogram of the thinned samples is shown in Fig. 3a. As the number of thinning processes increases, the RMS roughness tends to slightly decrease, which is correlated with the strain, as higher strain causes a smoother surface[28]. As the RMS roughness slightly decreases when the number of thinning iterations increases, the fractal dimension, which indicates the flatness and complexity of the surface, decreases to 2.338. This high level of flatness indicates that it could be an excellent choice for a 2D-like substrate for high performance electronic devices.

Further analyses of the electrical characteristics of valley-engineered silicon transistors are presented in Fig. 4. As mentioned earlier, in this measurement, the top gate electrode on the HfO_2 passivation layer was grounded for accurate measurement[29]. Buried oxide (BOX) underneath the silicon was used as a gate dielectric, the thickness of which was 140 nm. Figure 4a shows the drain voltage (V_D) dependence of the conductance oscillation for $V_D = 0.05$ V, 1 V, and 2 V. The average peak-to-peak voltage in conductance oscillation shows no clear correlation to the drain voltage. However, the conductance oscillation has a strong and clear dependence on the silicon thickness, as shown in Fig. 4b. As the silicon thickness decreases, the inter-peak voltage is enlarged. These results are expected and also evidence that the oscillation is from the sub-band splitting, because the drain voltage does not affect sub-band splitting whereas the decrease of the silicon thickness will increase the sub-band separation. Sub-band separations, the amount of valley splitting, were calculated using the measured inter-peak voltage. (See Supplementary Information Part 3) Fig. 4c shows the calculated sub-band separation with respect to the drain voltage and silicon thickness. The amount of sub-band separation in the 2.5 nm thick silicon channel device is
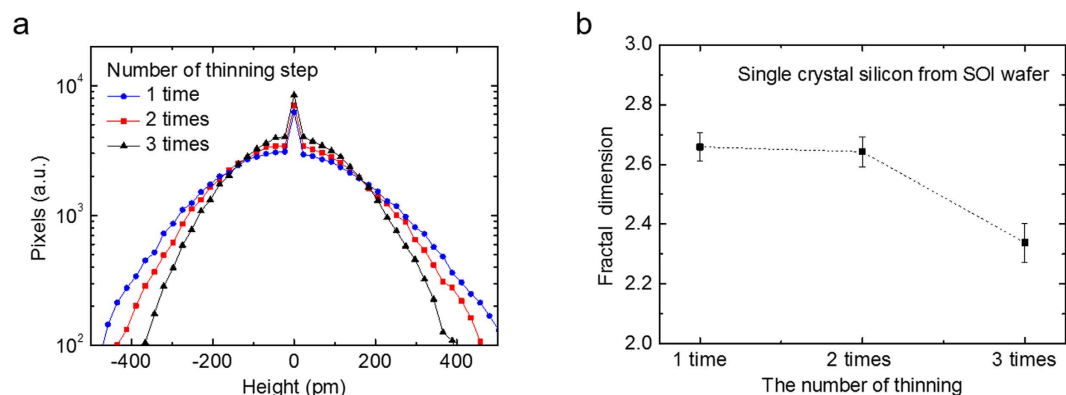
Figure 3. Surface roughness measured by non-contact mode AFM. (**a**) Height histogram graph of the thinned sample with respect to the number of iterations of the silicon thinning process. The distribution of heights tends to narrow as the thinning cycle increases. In order to clearly show the difference in the height histograms, the y-axis uses a log scale. (**b**) The fractal dimension of thinned samples is calculated by XEI, showing the complexity and flatness of the surface. The three-times-thinned sample shows the lowest value, 2.338, which implies that its flatness level is similar to a 2-D material.

70.2 meV, which is larger than the typical Brillouin zone end phonon energy (~ 60 meV in Si)[10]. This large amount of sub-band separation is critical because the inter-valley scattering in narrow valleys is greatly suppressed when valley splitting is larger than 60 meV. The extracted field effect mobility in Fig. 4d,e also verifies the relation between mobility and sub-band separation. When, calculating mobility, the transconductance was used when $V_{ds} = 0.05$ V. In mobility versus gate voltage, the mobility curve has several peaks because of the conductance oscillation caused by quantum confinement effect. The peak mobility in Fig. 4e indicates the mobility value of the highest peak, while the average mobility in the same figure means the average value taken from the top 5 highest peaks. The reason to plot the average mobility together with the peak mobility is to ensure the general trend of the mobility behavior against silicon thickness variation. The mobility of the 2.5 nm thick silicon channel device shows a sudden increase, and is almost 5 times higher than that of the 7 nm thick silicon channel device. The mobility of the 5 nm and 7 nm thick silicon channel devices is similar at around 50 cm^{2}V^{-1}s^{-1}. The main reasons of low mobility for these silicon thicknesses are the junctionless mode of device operation mechanism and high resistance because of ultra-thin silicon thickness. High channel doping of junctionless transistor results in lower mobility compared to inversion mode transistor. High series resistance in S/D region also contributed to the low mobility. Although the amount of sub-band separation increases almost linearly as the body thickness decreases, the mobility increases sharply only in the 2.5 nm thick silicon channel device. This result confirms that the sub-band separation in 2.5 nm thick silicon is indeed larger than the Brillouin zone end phonon energy (60 meV in silicon). The combination of these two mechanisms – a quantum confinement effect due to nanoscale thickness and a strain effect – lead to enhanced performance via engineering valleys in the silicon.

In summary, valley engineering of silicon was conducted by a silicon thinning process using repeated low-temperature oxidation and stripping the oxide. By carefully controlling the silicon surface it was possible to achieve an extremely smooth surface, reaching an almost single atomic level roughness of ~0.13 nm. The repeated low temperature oxidation achieved a high tensile strain of 2.2% in silicon channel. These techniques result in larger sub-band separation in the 2.5 nm thick silicon channel device than the Brillouin zone end phonon energy. The results presented in this paper demonstrate that transistor performance can be dramatically enhanced by the valley engineering of silicon together with RTQCE. These findings are expected to contribute to the advancement of low dimensional silicon device technology, which can open a pathway for realizing high performance flexible electronic devices with strong potential for commercialization.

Methods

Silicon preparation and device fabrication. The silicon was fabricated by starting with a commercially available silicon-on-insulator (SOI) wafer. The SOI thickness of the starting wafer was 100 nm. First, high-temperature furnace oxidation at 1000 °C and stripping the oxide were repeated until the SOI thickness reached approximately 10 nm. Low-temperature oxidation at 750 °C for 25 min and stripping the oxide were then repeated until the SOI thickness decreased to 7 nm, 5 nm, or 2.5 nm. Each low oxidation cycle can remove silicon thickness of 2.5 nm. To fabricate a junctionless transistor, a wafer was uniformly doped by arsenic implantation with an energy of 3 keV and a dose of 5×10^{13} cm^{-2}, followed by rapid thermal annealing at 1000 °C for 10 sec. To uniformly spread dopants throughout the entire silicon on insulator, additional furnace annealing at 1000 °C for 10 hour was performed in a N$_2$ ambient. A dumbbell-shape active region was defined by a standard lithography process. Device isolation was achieved by removing the silicon on insulator in the non-active region through a dry etching process. HfO$_2$ was deposited on the silicon channel region for passivation. A Ni/Al stack was deposited to form a top gate electrode. The high work function of nickel helps to deplete the highly-doped silicon channel. The source-drain contact was made by aluminum deposition. Post-metallization annealing was carried out at 410 °C for 30 minutes in a 10% H$_2$ ambient to lower the interface state density.
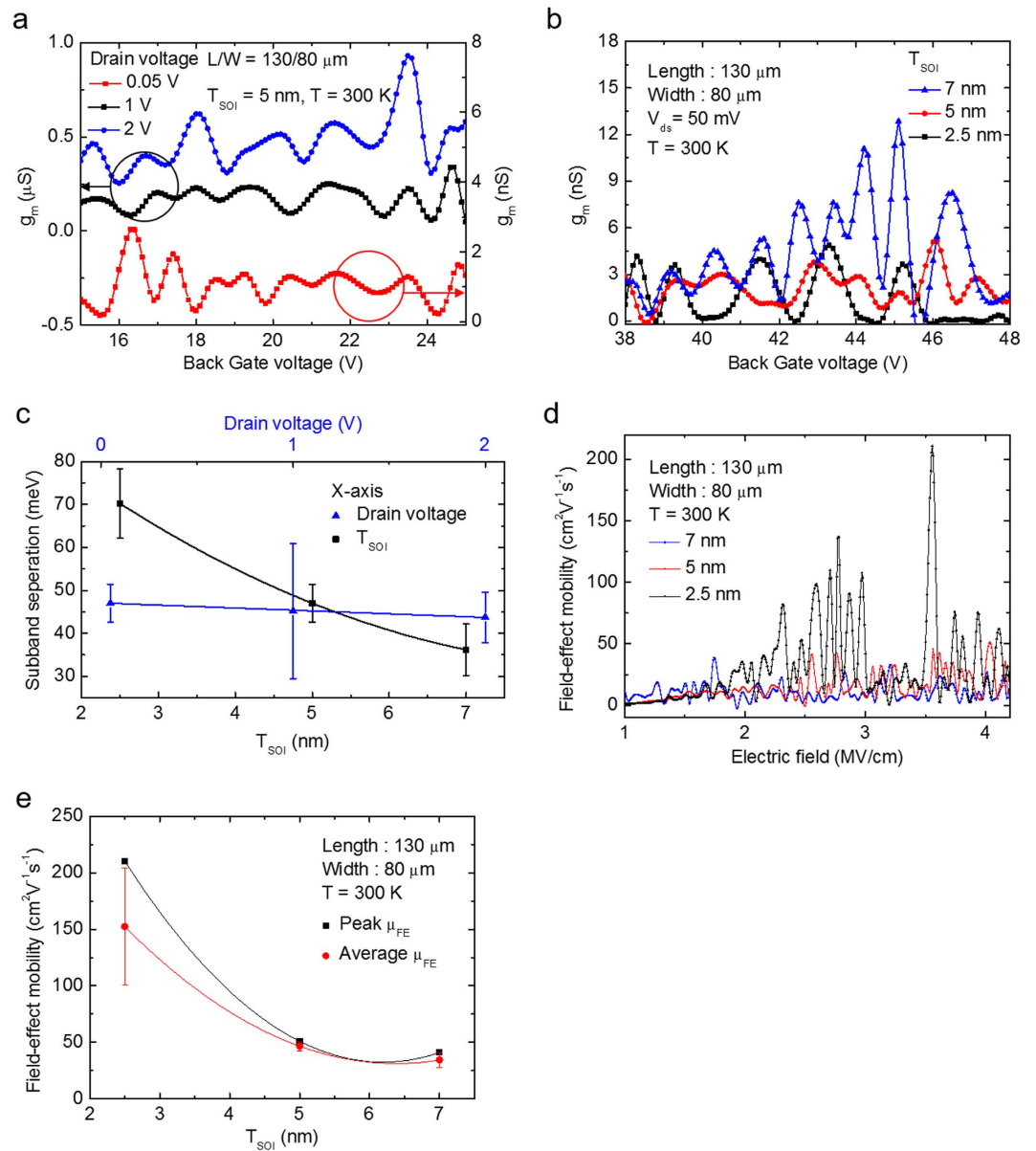
Figure 4. (**a**) Trans-conductance oscillation for different drain voltages. Room temperature quantum confinement (RTQCE) is observed regardless of the drain voltage. The inter-peak voltage indicates the amount of sub-band separation. (**b**) Conductance oscillation was clearly shown when the top silicon thickness is below 7 nm. The voltage interval between peaks clearly increases as the top silicon thickness decreases. (**c**) Calculated sub-band separation. 70.2 meV valley splitting was obtained in the 2.5 nm thick device. Since valley splitting is greater than the Brillouin zone end phonon energy, at about 60 meV, inter-valley phonon scattering is suppressed, which directly affects the mobility. (**d**) Field effect mobility versus electric field. (**e**) Field effect mobility versus top silicon thickness. A fivefold increment in field effect mobility was obtained in the 2.5 nm thick silicon device compared to that of the 7 nm thick device, as the amount of sub-band separation in the 2.5 nm thick silicon channel device is larger the typical Brillouin zone end phonon energy.

Device characterization and measurement. The fabricated back-gated junctionless transistor was measured using a semiconductor parameter analyzer and a probe station. To characterize the mobility of the junctionless transistors, the field effect mobility was calculated from the conventional trans-conductance method, using the equation $\mu_{FE} = \frac{L\,G_m}{W C_{ox} V_{ds}}$, where L and W are the channel length and width, respectively, and G_m is the trans-conductance, C_{ox} the gate capacitance, and V_{ds} the drain-to-source voltage. Atomic force microscopy, NX10 model manufactured by Park Systems, was used to characterize the surface roughness of the silicon with a new tip. The XY resolution is 0.05 nm and Z resolution is 0.015 nm. A scan area of $10\,\mu m \times 10\,\mu m$ was analyzed using the XEI program to assess the RMS surface roughness, height histogram, 1D/2D power spectral density, and fractal dimensions. The fractal dimension was calculated by the triangulation method with a linear interpolation.

References

1. Geim, A. K. & Novoselov, K. S. The rise of graphene. *Nature Mater.* **6,** 183–191 (2007).
2. Liao, L. *et al.* High-speed graphene transistors with a self-aligned nanowire gate. *Nature* **467,** 305–308 (2010).
3. Kang, K. *et al.* High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520,** 656–660 (2015).
4. Li, T. *et al.* Silicene field-effect transistors operating at room temperature. *Nature nanotech.* **10,** 227–231 (2015).
5. Li, L. *et al.* Black phosphorus field-effect transistors. *Nature nanotech.* **9,** 372–377 (2014).
6. Colinge, J.-P. *et al.* Nanowire transistors without junctions. *Nature nanotech.* **5,** 225–229 (2015).
7. Ryu, H., Kim, J. & Hong, K.-H. Atomistic study on dopant-distributions in realistically sized, highly P-doped Si nanowires. *Nano Lett.* **15,** 450–456 (2014).
8. Barral, V. *et al.* Strained FDSOI CMOS technology scalability down to 2.5 nm film thickness and 18 nm gate length with a TiN/HfO$_2$ gate stack. *Tech. Dig. IEDM* 61–64, doi: 10.1109/IEDM.2007.4418863 (2007).
9. Weber, O. *et al.* High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding. *Tech. Dig. IEDM* 245–248, doi: 10.1109/IEDM.2008.4796663 (2008).
10. Chen, F. *et al.* Quantum confinement, surface roughness, and the conduction band structure of ultrathin silicon membranes. *ACS Nano* **4,** 2466–2474 (2010).
11. Wang, T. *et al.* Size-dependent energy levels of InSb quantum dots measured by scanning tunneling spectroscopy. *ACS Nano* **9,** 725–732 (2015).
12. Park, J.-T., Kim, J. Y., Lee, C.-W. & Colinge J.-P. Low-temperature conductance oscillations in junctionless nanowire transistors. *Appl. Phys. Lett.* **97,** 172101 (2010).
13. Li, X. *et al.* Low-temperature quantum transport characteristics in single n-channel junctionless nanowire transistors. *IEEE Electron. Dev. Lett.* **34,** 581–583 (2013).
14. Yi, K. S. *et al.* Room-temperature quantum confinement effects in transport properties of ultrathin Si nanowire field-effect transistors. *Nano Lett.* **11,** 5465–5470 (2011).
15. Trivedi, K., Yuk, H., Floresca, H. C., Kim, M. J. & Hu, W. Quantum confinement induced performance enhancement in sub-5-nm lithographic Si nanowire transistors. *Nano Lett.* **11,** 1412–1417 (2011).
16. Ang, K. W. *et al.* Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions. *Tech. Dig. IEDM* 1069–1071 (2004).
17. Weman, H., Monemar, B., Oehrlein, G. S. & Jeng, S. J. Strain-induced quantum confinement of carriers due to extended defects in silicon. *Phys. Rev. B* **42,** 3109–3112 (1990).
18. Kash, K. *et al.* Observation of quantum confinement by strain gradients. *Phys. Rev. Lett.* **67,** 1326–1329 (1991).
19. Takagi, S.-I. *et al.* Sub-band structure engineering for advanced CMOS channels. *Solid state elec.* **49,** 684–694 (2005).
20. Uchida, K., Koga, J., Ohba, R., Numata, T. & Takagi, S.-I. Experimental evidences of quantum-mechanical effects on low-field mobility, gate-channel capacitance, and threshold voltage of ultrathin body SO1 MOSFETs. *Tech. Dig. IEDM* 633–636, doi: 10.1109/IEDM.2001.979588 (2001).
21. Uchida, K. *et al.* Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm. *Tech. Dig. IEDM* 47–50, doi: 10.1109/IEDM.2002.1175776 (2002).
22. Ding J. *et al.* Engineering quantum anomalous/valley hall states in graphene via metal-atom adsorption: an ab-initio study. *Phys. Rev. B* **84,** 195444 (2011).
23. Li X. *et al.* Superlattice valley engineering for designer topological insulators. *Sci. Rep.* **4,** 6397 (2014).
24. Kao, D.-B., Mcvittie, J. P., Nix, W. D. & Saraswat, K. C. Two-dimensional thermal oxidation of silicon-II. Modeling stress effects in wet oxides. *IEEE Trans. Electron. Dev.* **35,** 25–36 (1988).
25. Moselund, K. E. *et al.* The high-mobility bended n-channel silicon nanowire transistor. *IEEE Trans. Electron. Dev.* **57,** 866–876 (2010).
26. Ang, K.-W. *et al.* Lattice strain analysis of transistor structures with silicon-germanium and silicon-carbon source/drain stressors. *Appl. Phys. Lett.* **86,** 093102 (2005).
27. Ishigami, M., Chen, J. H., Cullen, W. G., Fuhrer, M. S. & Williams, E. D. Atomic Structure of Graphene on SiO$_2$. *Nano Lett.* **7,** 1643–1648 (2007).
28. Urena, F., Olsen, S. H., Escobedo-Cousin, E., Minamisawa, R. A. & Raskin, J.-P. Roughness analysis in strained silicon-on-insulator wires and films. *J. Appl. Phy.* **116,** 124503 (2014).
29. Chen, F., Xia, J., Ferry, D. K. & Tao, N. Dielectric screening enhanced performance in graphene FET. *Nano Lett.* **9,** 2571–2574 (2009).

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Author Contributions

S.-Y.K. fabricated the samples and performed measurements. S.-Y.K., S.-Y.C., W.S.H. and B.J.C. analyzed the data and discussed the results. S.-Y.K., S.-Y.C., W.S.H. and B.J.C. wrote the manuscript.

Additional Information

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