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Two-dimensional BN buffer for plasma enhanced atomic layer deposition of Al$_2$O$_3$ gate dielectrics on graphene field effect transistors

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Here, we investigate the use of few-layer metal organic chemical vapor deposition (MOCVD) grown BN as a two-dimensional buffer layer for plasma enhanced atomic layer deposition (PE-ALD) of Al$_2$O$_3$ on graphene for top gated field effect transistors (FETs). The reactive nature of PE-ALD enables deposition of thin (2 nm) dielectrics directly on graphene and other two-dimensional materials without the need for a seed or functionalization layer; however, this also leads to significant oxidation of the graphene layer as observed by Raman. In FETs, we find this oxidation destroys conductivity in the graphene channel. By transferring thin (1.6 nm) MOCVD BN layers on top of graphene channels prior to PE-ALD, the graphene is protected from oxidation enabling BN/Al$_2$O$_3$ layers as thin as 4 nm. Raman and X-ray photoelectron spectroscopy on BN films show no significant oxidation caused by PE-ALD of Al$_2$O$_3$. Inserting the BN layer creates an atomically abrupt interface significantly reducing interface charges between the graphene and Al$_2$O$_3$ as compared to use of a 2 nm Al buffer layer. This results in a much smaller Dirac voltage (− 1 V) and hysteresis (0.9 V) when compared to FETs with the Al layer (V_{Dirac} = − 6.1 V and hysteresis = 2.9 V).

Devices based on two-dimensional (2D) materials offer great possibilities for applications requiring mechanical flexibility[1], ultra-low power[2], heterogeneous integration[3], and extreme scaling[4]. The layered structure of these materials, with strong in-plane bonding and weak van der Waals inter-planar bonding, provides the ability to thin and stabilize them down to a single layer. Although, these materials have fully compensated surfaces with no dangling bonds; they are quite sensitive to the surrounding environment, including the substrate, ambient adsorbates, and in devices, the addition of component layers like-contacts, gate dielectrics, and passivation layers[5–10]. These can lead to oxidation, doping, and charge scattering severely degrading properties. In graphene, the effects of these surrounding elements have been shown to greatly impact basic transport properties and devices performance. To mitigate the effects of the substrate and adsorbates, a thin van der Waals (vdW) buffer layer, like hBN[11,12], has shown to be extremely effective at preserving the properties of graphene.

The progression toward high performance 2D devices necessitates the integration with high quality thin dielectrics, for gates, tunneling barriers, etc.[13–15]; for which, atomic layer deposition (ALD) is ideally suited. However, 2D materials present a significant challenge to depositing ultra-thin, high quality, high-κ dielectrics due to the inherent lack of reactive surface nucleation sites[16]. To overcome these nucleation challenges, various surface functionalization and seeding layers have been used to promote ALD deposition. Surface functionalization by treatment with reactive species like ozone[17], XeF$_2$[18], and H$_2$, O$_2$, or N$_2$ plasma[19–21] produce functional surface groups and defects that provide nucleation sites. However, these functionalization methods partially convert sp^2 C bonds in graphene to sp^3 degrading properties, which can be in some cases recovered through annealing[19]. Nucleation can also be improved by functionalization with physisorbed molecules like H$_2$O[22] and NO$_2$[23] followed by low temperature thermal ALD. Zheng et al.[22] found the low temperature Al$_2$O$_3$ ALD layer to be low density and have low dielectric constant requiring deposition of a second higher temperature high quality layer. On the other hand, seeding-layers consisting of thin polymers[24], metal-oxides[25,26], or metals[27] can be deposited by low impact methods, like evaporation, that minimize damage to the graphene layer. Functionalizing the graphene surface or inserting a seed layer between graphene and the ALD dielectric can introduce interfacial charges and traps, reduce the total dielectric constant of the gate stack, and limit the minimum equivalent oxide
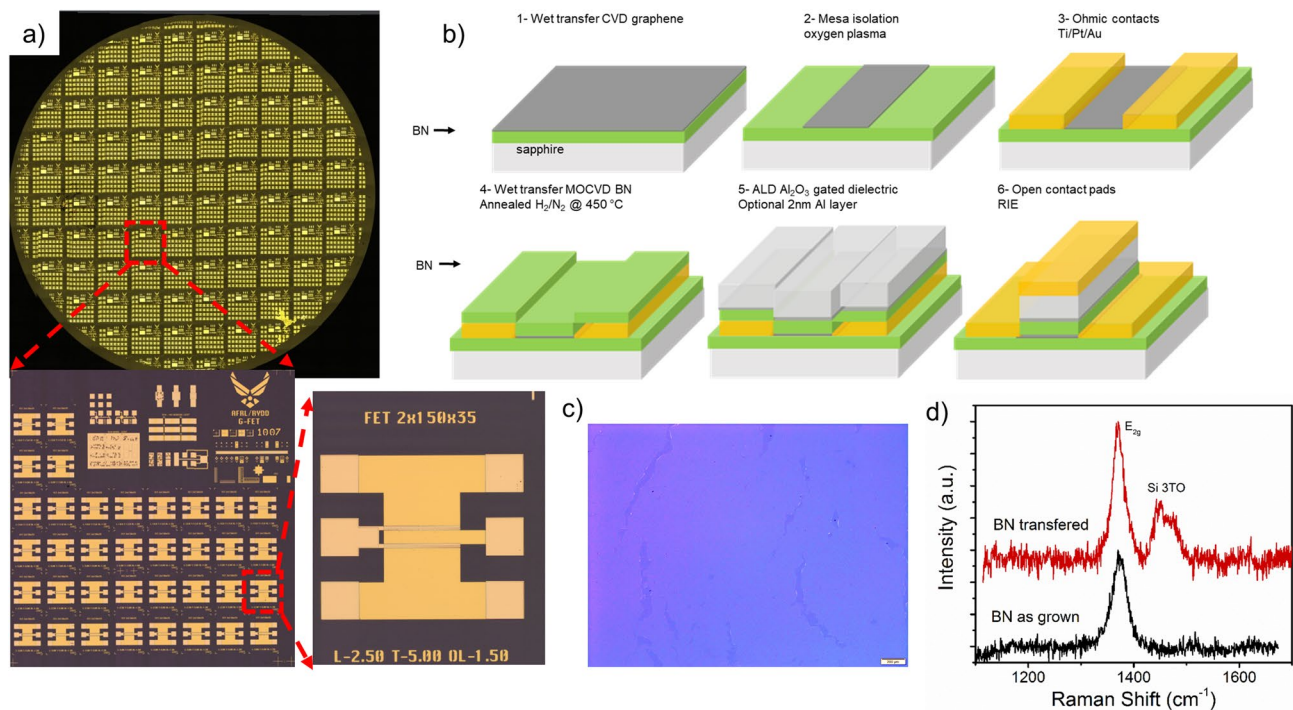
Figure 1. Graphene FET fabrication process. (**a**) Optical images of a full 2″ wafer, reticle, and single FET. (**b**) Process flow for device fabrication. (**c**) Optical image of MOCVD BN layer transferred to SiO2/Si and (**d**) Raman spectra of BN before and after transfer. The full 2″ wafer in (**a**) is a stitched image from multiple 5× images created using MetaMorph imaging software ver. 7.10 (www.moleculardevices.com).

thickness (EOT)[4,22,28]. One alternative is to use a 2D buffer layer on top of the graphene to protect the interface during ALD[29,30].

In this paper, we investigate the use of 2D BN grown by metal organic chemical vapor deposition (MOCVD) as a thin buffer layer for plasma enhanced (PE) ALD of Al_2O_3 on graphene for top gated field effect transistors (FETs). PE-ALD offers a number of advantages over thermal ALD for deposition of dielectrics on 2D materials. Generally, the high reactivity of the plasma species allows for a wider range of materials to be produced, with higher quality, higher density, and at lower temperatures than thermal ALD[31]. Plasma species can also modify the surface promoting nucleation and greatly reducing nucleation delay critical for reducing gate thickness[32]. Additionally, PE-ALD enables more exotic coating and high-*k* dielectric that can reduce (EOT) even further[33]. For graphene and other 2D materials the plasma species can serve as in-situ functionalization eliminating the need for ex-situ functionalization or seeding required for thermal ALD of ultra-thin high quality layers; however, this occurs at the cost of damaging the 2D layer[29,34]. By transferring a thin (1.6 nm) BN layer on top of the graphene FET channel prior to PE-ALD of the Al_2O_3 gate dielectric, we demonstrate a weakly interacting 2D buffer layer that protects the graphene layer during PE-ALD. We find that depositing directly on graphene with no seed layer causes significant oxidation destroying the graphene channel, while devices with a BN buffer layer are preserved. These BN devices also have significantly lower shift in the Dirac point and lower hysteresis due to reduced interfacial doping at the BN/graphene vdW interface.

Results

Top-gated graphene FETs were fabricated on chemical vapor deposition (CVD) graphene films transferred to 2″ MOCVD grown BN on sapphire substrates. A variety of FETs with gate lengths from 2.5 to 10 μm were used to investigate electrical characteristics of devices with different buffer layers for PE-ALD Al_2O_3 gate dielectric, Fig. 1a. For this investigation, devices with four different buffer layers prior to deposition of 20 nm Al_2O_3 were explored: (1) no seed layer—PE-ALD directly on graphene, (2) transferred 2D BN on graphene followed by PE-ALD, (3) 2 nm e-beam evaporated Al seed layer followed by PE-ALD, and (4) transferred 2D BN layer followed by 2 nm e-beam evaporated Al seed layer and PE-ALD. Figure 1b shows the process flow for device fabrication. In this process, graphene mesas were defined by O_2-plasma etching followed by e-beam deposition of Ti/Pt/ Au ohmic contacts. An O_2 plasma power of 200 W was used to selectively remove the graphene, while leaving the BN layer intact. For devices with the 2D BN layer a 1.6 nm thick BN layer was wet transferred on top of the defined graphene channel and contacts. BN layers were grown on 2″ sapphire wafers by MOCVD under self-terminating growth conductions, similar to the BN layer used on the substrates side, providing a large-area, highly reproducible and uniform 1.6 nm thick layer[35,36]. Figure 1c,d shows an optical image and Raman spectra from representative BN layers transferred to SiO_2/Si. After, the BN is transferred, the PMMA is removed, and the stack annealed to improve the graphene BN interface and clean the BN surface prior to ALD. Next, a 2 nm
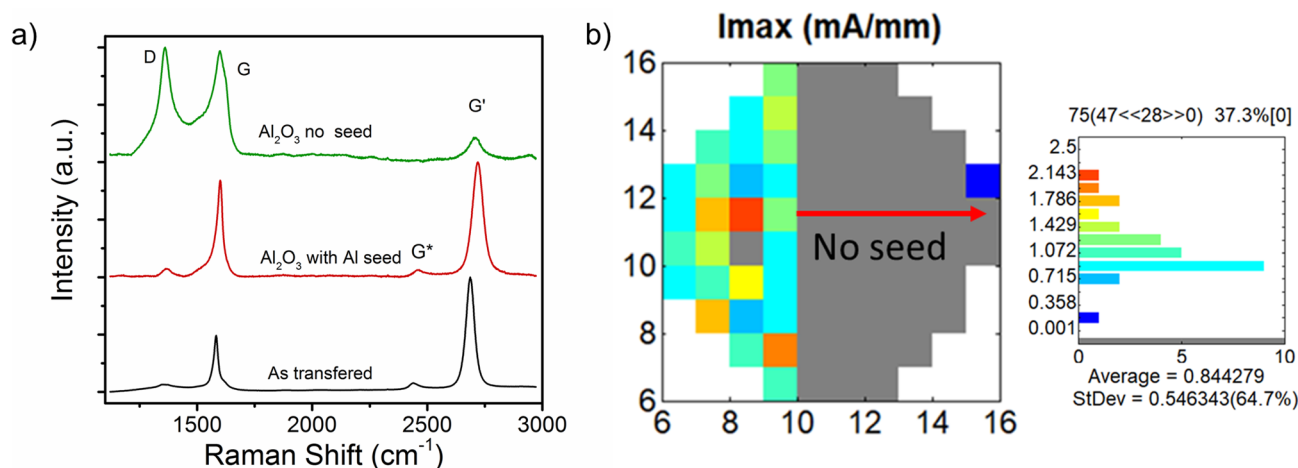
Figure 2. (**a**) Graphene Raman spectra comparing before and after PE-ALD of Al_2O_3 with Al seed and with no seed. (**b**) Map of maximum Ids from graphene FET wafer comparing effect of Al seed layer prior to Al_2O_3 deposition.

Al seed layer, excluded in buffer layer 1 and 2, is deposited followed by 20 nm of Al_2O_3 by PE-ALD and Ti/Au gate contacts.

The advantages of PE-ALDs in-situ auto functionalization comes at the consequence of potentially damaging the graphene layer. Raman spectroscopy was used to investigate the effect of Al_2O_3 deposition on graphene's structural quality. Figure 2a shows Raman spectra from a graphene layer transferred to sapphire before and after Al_2O_3 deposition. To compare the effect of the 2 nm Al layer, the graphene film was masked and Al was deposited on half of the sample. Compared to the as transferred spectra, the half without the Al layer shows a significant increase in defect related D/D' peaks and reduction in the G' indicative of the formation of graphene oxide[37]. The side with the 2 nm Al layer does not have the same increase in D and D' indicating the layer serves to protect the graphene. AFM images (Fig. S1) of Al_2O_3 surface deposited directly on graphene and using an Al seed layers show a similar roughness (~ 1.3 nm RMS) and morphology. Both layers appear to completely cover the graphene layer with no signs of nucleation issues, which is expected due to the in-situ functionalization caused by the O_2 plasma.

To investigate the effect on device operation, a full (2×150 μm) graphene FET wafer was processed, in ~ half of the devices the Al_2O_3 gate dielectrics were deposited with no seed layer and the other half with the Al seed layer. Device characteristics were measured on one device with a 10 μm gate length per reticle. Figure 2b shows a map of the maximum measured current from 95 devices across the wafer. The devices with no seed layer had no measured working devices out of the 57 measured, while the half with the Al seed layer had a yield of 95% working devices with a maximum I_D in the range of 0.7–2.1 mA/mm at V_{ds} of 0.1 V. The oxidation observed in Raman clearly has a significant effect on the electrical conductivity of the graphene layer.

Although use of the Al layer preserves the graphene by protecting it from oxidation, it has been shown to introduce interface charges and traps causing unintentional doping and hysteresis in FETs[28,35]. To mitigate these interface effects we explore inserting a few layer thick sp^2 bonded BN layer between the graphene and Al_2O_3 layer. Figure 3a–c show Raman, AFM and XPS from the as grown BN layer on sapphire before and after PE-ALD of Al_2O_3. BN is well established as an oxidation resistant coating even when thinned to only a few monolayers[38], but how MOCVD/CVD grown films react to O_2 plasma during PE-ALD is not established. AFM shows a uniform surface morphology with a roughness of ~ 0.5 nm (Fig. 3a). Comparison of before and after Raman shows little change in the E_{2g} mode of BN indicating no significant degradation to the BN structure. Investigation of oxidation of these BN films at high temperatures in O_2 and high humidity, by Raman and XPS, show them to be stable above 800 °C (Fig. S2–S3). XPS analysis of the BN layer after PE-ALD of 2 nm Al_2O_3 shows only one photoelectron peak corresponding to the B 1 s (190.5 eV) and N 1 s (397.8 eV) in good agreement with previous reports on sp^2 bonded BN[39] with no oxide related peaks around 193 eV (B–O)[40]. The lack of oxidation signatures in the BN layer indicates the BN layer could be thinned to below four mono-layers. With the established stability of the BN layers under the PE-ALD process, we now investigate its use as a buffer layer for protecting graphene. Figure 3d shows the graphene Raman spectra from before and after PE-ALD Al_2O_3 on bare graphene and graphene covered with the BN buffer. As observed in Fig. 2, direct PE-ALD of Al_2O_3 oxidizes the graphene layer, but by covering the graphene with a thin BN layer the graphene is preserved with little change in the Raman. This can even be observed optically (Fig. S4) where the unprotected portion of graphene becomes completely transparent.

To compare the effect of the 4 buffer types on FET performance, we fabricated a full wafer with top gates fabricated using each type, Fig. 4a. After mesas were defined and ohmic contacts deposited, two films of BN, from the same original wafer, were transferred on each half of the wafer, as denoted by the green rectangles in Fig. 4a. Then the Al layer was deposited on half of the wafer, similar to the wafer in Fig. 2, followed by PE-ALD of Al_2O_3. Wafers were mapped by I_{ds}—V_G transfer curves from one transistor with a 10 μm gate length per reticle. Figure 4b shows the map of maximum measured current for each of these devices at $V_{ds} = 0.1$ V. Just as in Fig. 2 we see a clear delineation in operating devices corresponding to the use of the Al seed layer. However, here we see
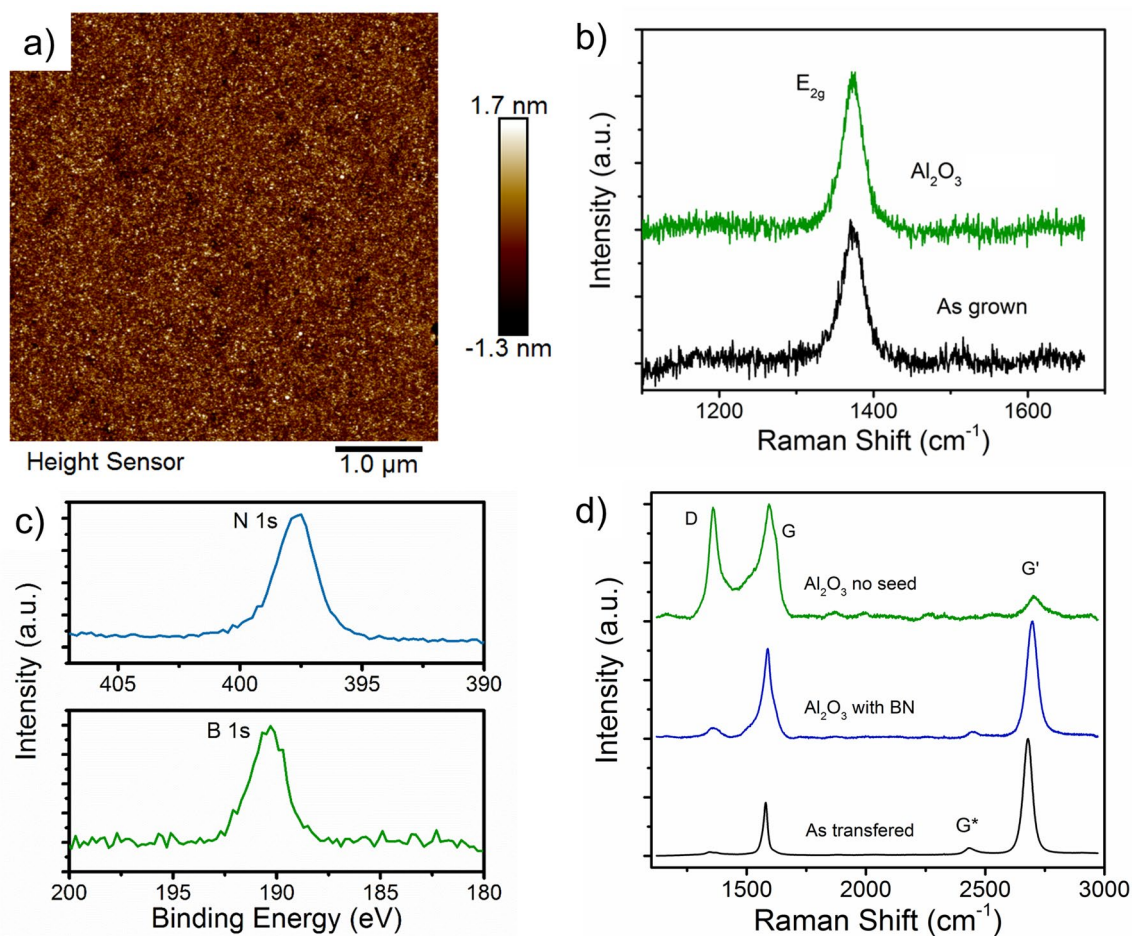
Figure 3. (**a**) AFM image of Al_2O_3 surface on BN/sapphire substrate. (**b**) Raman spectra from BN layer before and after Al_2O_3 deposition. (**c**) XPS spectra of N 1s and B 1s from BN layer under 2 nm of Al_2O_3. (**d**) Raman spectra comparing graphene before and after Al_2O_3 deposition with no seed layer and with the BN layer.

a cluster of functioning devices on the side with no Al layer where the BN film was transferred. Similarly, on the Al seeded side we see multiple functioning devices in regions where the BN was transferred. Figure 4c,d shows representative I_{ds}–V_{ds} output curves from devices fabricated using each of the 4 buffer types. In the devices with the Al seed, a positive increase in I_{ds} with V_G from − 5 to 5 V was measured indicating majority electron carriers. Hall effect measurements from as-transferred graphene on BN/sapphire substrates found all samples were p-type prior to device processing with an average hole concentration of 4×10^{12} cm^{-2} and mobility of 1,860 cm^2/Vs. This shift in carrier type after device fabrication is due to significant n-type doping caused by deposition of the Al_2O_3 gate dielectric[9,35]. Devices with only the BN buffer layer and both the BN and Al layer show a switch in the direction of I_{ds} dependence on V_G. Hall effect measurements taken from van der Pauws (vdP) structures from each region (Fig. 1a top center of the recital) confirm this n-type doping with measured n_s (average of four vdPs) from vdPs with the BN buffer, Al seed layer, and both the BN and Al seed layer of -9×10^{11}, -3×10^{12}, and -7×10^{12} cm^{-2} and Hall mobility of 890, 560, 1,060 cm^2/Vs. To check that the buffer type does not impact the gate leakage current (I_G), we measure I_G as V_G is swept from − 8 to 4 V at V_{ds} of 0.5 V. Figure 4e shows a very low I_G for all gate types, between 12 and 16 pA, demonstrating consistent insulating behavior of the gate dielectric independent of buffer type.

Transfer curves for 10 μm gate length devices for each gate type are shown in Fig. 5. All device types show typical ambipolar behavior with a negative V_{Dirac} due to n-type doping and similar peak transconductance of 30 μS or better. Upon the reverse V_G sweep, hysteresis with a positive shift in V_{Dirac} is observed in I_{ds}–V_G, which is common in graphene FETs. This shift is due to negative charge traps at the graphene interface from defects in the dielectric and/or contamination (H_2O, hydroxides, hydrocarbons)[41–43]. The effect of interface contamination can be reduced by processing under vacuum or inert environments, cleaning processes, annealing, or by inserting a 2D buffer layer, like BN. Indeed, if we compare transfer curves from each buffer type, we observe V_{Dirac} and hysteresis depend strongly on the buffer type with the lowest doping and hysteresis in devices with a BN buffer (Fig. 5d). This shows the inert van der Waals surface of sp^2 BN forms a clean interface and effectively screens charges and doping from Al_2O_3[35]. Furthermore, if we compare devices with only the BN buffer layer and both the BN and Al buffer layers we observe a further reduction in doping and hysteresis by eliminating the Al layer.
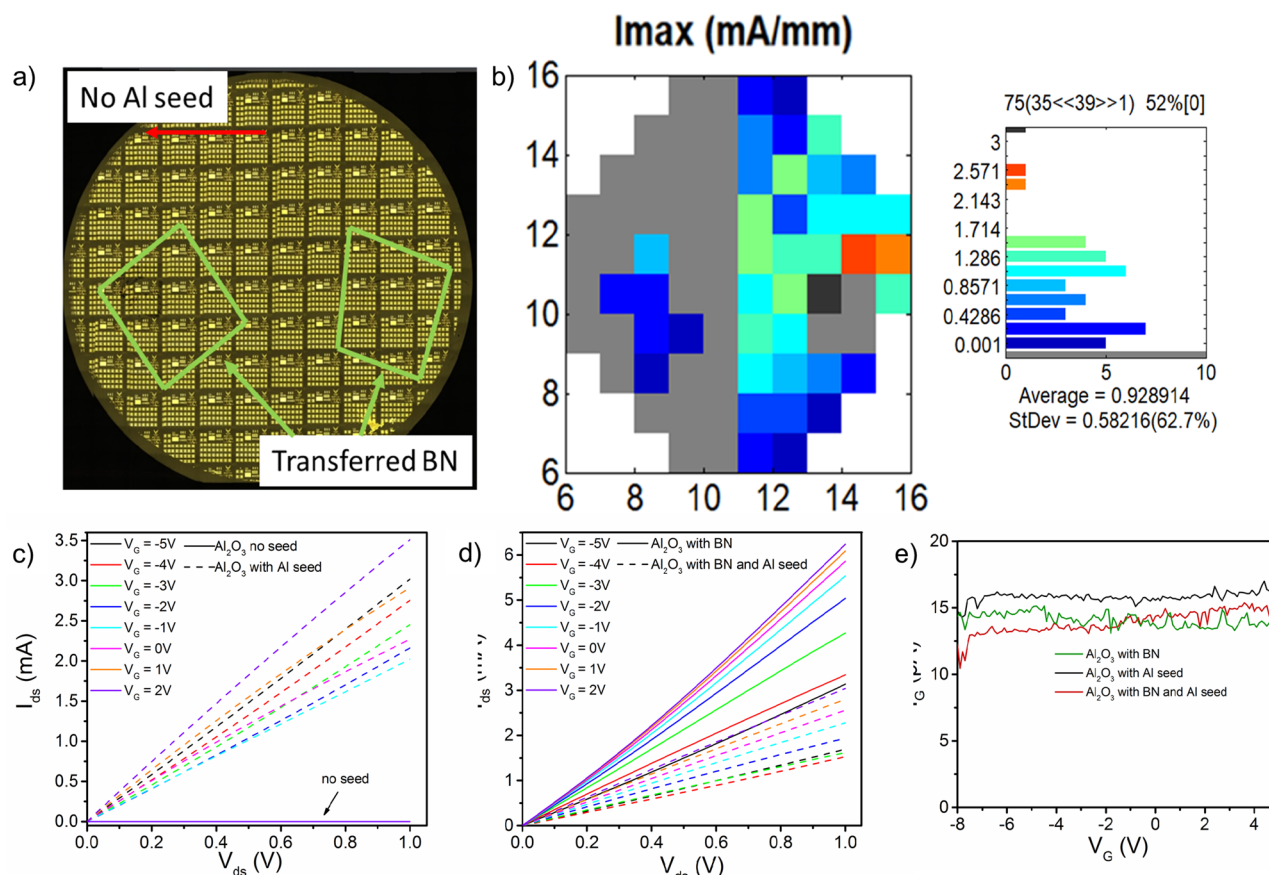
Figure 4. Graphene FETs comparing each of the 4 buffer types. (**a**) Optical image of the 2″ FET wafer indicating regions where BN was transferred (green rectangles) and Al seed deposited. (**b**) Map of maximum I_{ds} from the FET wafer. (**c**) Output curves from 10 μm gate length FETs with no seed and the BN layer and (**d**) with Al seed layer and with BN and Al seed layers. (**e**) Gate leakage current measured for the different buffer layer types at Vds = 0.1 V. The full 2″ wafer in (**a**) is a stitched image from multiple 5× images created using MetaMorph imaging software ver. 7.10 (www.moleculardevices.com).

This Al layer, which oxidizes during exposure to air and O_2 plasma during PE-ALD, is expected to be more highly defective having a higher concentration of traps than the PE-ALD Al_2O_3.

Conclusion

We have reported on the use of few-layer MOCVD grown BN as an oxidation resistant buffer for PE-ALD deposition of Al_2O_3 of graphene FETs. The reactive nature of PE-ALD provides a path for deposition of the continuous Al_2O_3 dielectrics as thin as 2 nm without the need for a nucleation layer but causes oxidation of the graphene channel. Various buffer schemes were investigated to prevent oxidation of the graphene and improve device performance. Both a thin Al layer and transferred BN were shown to protect the graphene from significant oxidation and produce good device performance. The deposition of the Al_2O_3 dielectric contributed to a significant n-type doping causing a negative shift in the V_{Dirac} and hysteresis due to interface contamination and defects in the dielectric. Inserting a thin BN layer enabled reduction of these effects by providing a clean 2D dielectric interface with graphene and eliminating the need for the defective Al buffer layer. This work demonstrates significant improvements in graphene top gated FETs by using MOCVD grown 2D BN as a dielectric buffer, which is broadly applicable to other 2D materials prone to oxidation.

Methods

Boron Nitride on 2″ sapphire substrates and transferred films used in this study were grown by metalorganic chemical vapor deposition (MOCVD) at 1,000 °C, 20 Torr and B/N ratio of 2250 for 30 min[36]. To transfer films, a 300 nm thick layer of PMMA was spun on the BN surface and cured at 180 °C. The BN layer was released by etching in a buffered oxide etch solution (BOE) at 20 °C for up to 2hrs. Released films were wet transferred, dried in air, followed by the PMMA removal with acetone, and finally annealed in 5% H_2:N_2 forming gas at 400 °C for 30 min. Graphene grown on copper by CVD using methane as the carbon source were transferred to the BN/ sapphire substrates using a typical wet transfer with PMMA, similar to the process described in Ref.[44].

The surface morphologies of graphene and BN layers were analyzed by AFM using a Bruker Dimension Icon in tapping mode. Raman measurements of graphene and BN were performed using a Renishaw inVia system under a backscattering geometry. A 488 nm excitation source at 4 mW, 20 μm slits, and a 3,000 l/mm grating was
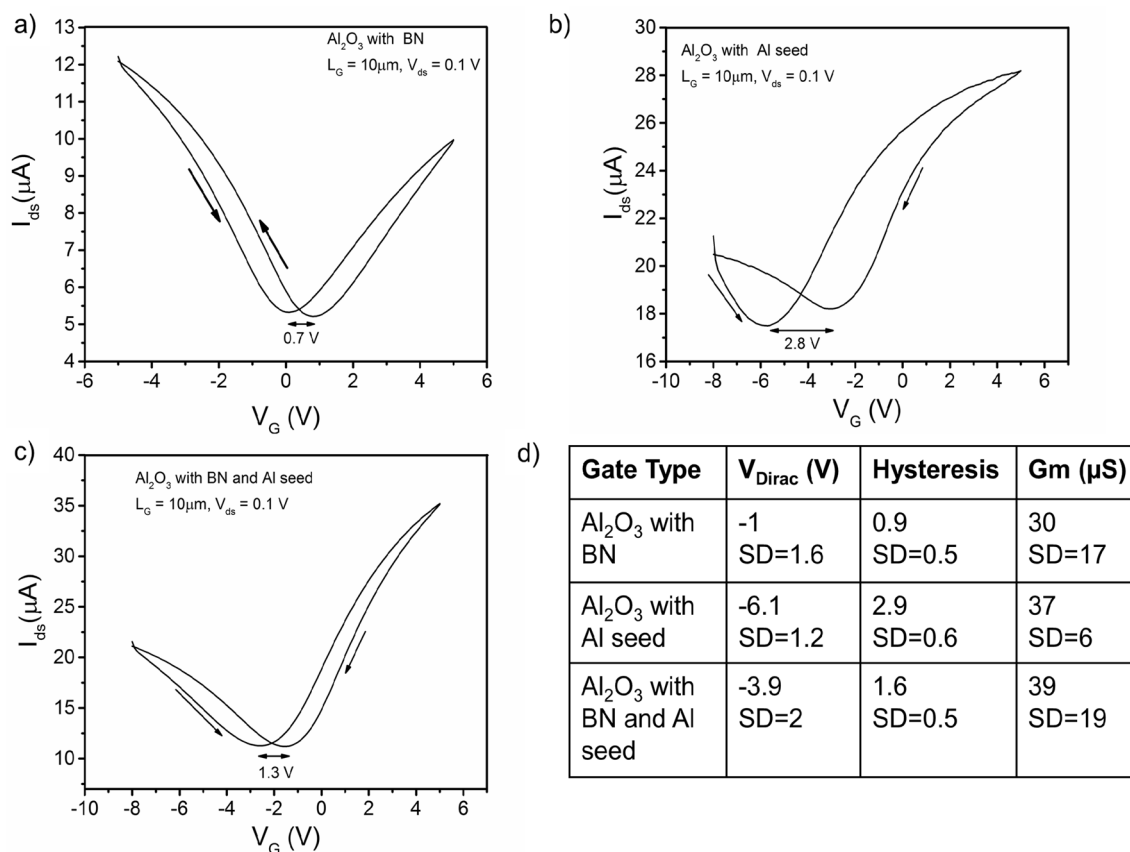
Figure 5. Transfer characteristics of graphene FETs with different buffer types (**a–c**). (**d**) Table summarizing mean V_{Dirac}, hysteresis, and peak transconductance from at least 10 devices with each gate buffer type (std. = standard deviation).

used for these measurements. Chemical analysis of films was performed using X-ray photoelectron spectroscopy (XPS, PerkinElmer Phi 5,500).

Graphene FETs were fabricated using transferred CVD graphene on BN/sapphire. The graphene mesas were etched using an O_2-plasma. Source and drain Ti/Pt/Au contacts were evaporated. A 20-nm thick Al_2O_3 top gate dielectric was deposited by ALD. ALD was performed at 250 °C with half cycles of trimethylaluminum and a remote 300 W oxygen plasma, achieving a growth rate of 0.94 A/cycle. Gate metal (Ti/Au) contacts were defined using a second lift-off process[31]. The automated electronic characterization was performed using a Cascade Summit 12 k probe station with an HP 4142 parameter analyzer and GSG probes.

References

1. Akinwande, D., Petrone, N. & Hone, J. Two-dimensional flexible nanoelectronics. *Nat. Commun.* **5**, 5678. https://doi.org/10.1038/ncomms6678 (2014).
2. Sarkar, D. *et al.* A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **526**, 91–95 (2015).
3. Shim, J. *et al.* Controlled crack propagation for atomic precision handling of wafer-scale two dimensional materials. *Science* **362**, 665–670 (2018).
4. Li, W. *et al.* Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nat. Electron.* **2**, 563–572 (2019).
5. Chen, J. H., Jang, C., Xiao, S., Ishigami, M. & Fuhrer, M. Intrinsic and extrinsic performance limits of graphene devices on SiO_2. *Nat. Nanotechnol.* **3**, 206–209 (2008).
6. Fratini, S. & Guinea, F. Substrate-limited electron dynamics in graphene. *Phys. Rev. B* **77**, 195415 (2008).
7. Chae, W. H., Cain, J. D., Hanson, E. D., Murthy, A. A. & Dravid, V. P. Substrate-induced strain and charge doping in CVD-grown monolayer MoS2. *Appl. Phys. Lett.* **111**, 143106 (2017).
8. Hongtao, L., Liu, Y. & Zhu, D. Chemical doping of graphene. *J. Mater. Chem.* **21**, 3335–3345 (2011).
9. Graces, N. Y. *et al.* Epitaxial graphene surface preparation for atomic layer deposition of Al_2O_3. *J. Appl. Phys.* **109**, 124304 (2011).
10. Giovannetts, G. *et al.* Doping graphene with metal contacts. *Phys. Rev. Lett.* **101**, 026803 (2008).
11. Dean, C. R. *et al.* Boron nitride substrates for high quality graphene electronics. *Nat. Mat.* **5**, 722–726 (2010).
12. Mayorov, A. S. *et al.* Micrometer-scale ballistic transport in encapsulated graphene at room temperature. *Nano Lett.* **11**, 2396–2399 (2011).
13. Wu, Y. *et al.* High-frequency, scaled graphene transistors on diamond-like carbon. *Nature* **472**, 74–78 (2011).
14. Zeng, C. *et al.* Vertical graphene-based hot electron transistor. *Nano Lett.* **13**, 2370–2375 (2013).
15. Mehr, W. *et al.* Vertical graphene base transistor. *IEEE Electron. Dev. Lett.* **33**, 691–693 (2012).

16. Vervuurt, R. H. J., Kessels, W. M. M. & Bol, A. A. Atomic layer deposition for graphene device integration. *Adv. Mater. Interfaces* **4**, 170232 (2017).
17. Lee, B. *et al.* Conformal Al$_2$O$_3$ dielectric layer deposited by atomic layer deposition for graphene-based nanoelectronics. *Appl. Phys. Lett.* **92**, 203102 (2008).
18. Robinson, Z. R. *et al.* Growth and characterization of Al$_2$O$_3$ films on fluorine functionalized epitaxial graphene. *J. Appl. Phys.* **120**, 075302 (2016).
19. Vervuurt, R. H. J. *et al.* Uniform atomic layer deposition of Al$_2$O$_3$ on graphene by reversible hydrogen plasma functionalization. *Chem. Mater.* **29**, 2090–2100 (2017).
20. Nourbakhsh, A. *et al.* Graphene oxide monolayers as atomically thin seeding layers for atomic layer deposition of metal oxides. *Nanoscale* **7**, 10781 (2015).
21. Lim, T., Kim, D. & Ju, S. Direct deposition of aluminum oxide gate dielectric on graphene channel using nitrogen plasma treatment. *Appl. Phys. Lett.* **113**, 013107 (2013).
22. Zheng, L. *et al.* Improvement of Al$_2$O$_3$ films on graphene grown by atomic layer deposition with pre-H$_2$O treatment. *ACS Appl. Mater. Interfaces* **6**, 7014–7019 (2014).
23. Nam, T. *et al.* A composite layer of atomic-layer-deposited Al$_2$O$_3$ and graphene for flexible moisture barrier. *Carbon* **116**, 553–561 (2017).
24. Sangwan, V. K. *et al.* Quantitatively enhanced reliability and uniformity of high-κ dielectrics on graphene enabled by self-assembled seeding layers. *Nano Lett.* **13**, 1162–1167 (2013).
25. Hollander, M. J. *et al.* Enhanced transport and transistor performance with oxide seeded high-k gate dielectrics on wafer-scale epitaxial graphene. *Nano Lett.* **11**, 3601–3607 (2011).
26. Fisichella, G. *et al.* Interface electrical properties of Al$_2$O$_3$ thin films on graphene obtained by atomic layer deposition with an in situ seedlike layer. *ACS Appl. Mater. Interfaces* **9**, 7761–7771 (2017).
27. Fallahazad, B. *et al.* Scaling of Al$_2$O$_3$ dielectric for graphene field-effect transistors. *Appl. Phys. Lett.* **100**, 093112 (2012).
28. Schiliro, E., Nigro, R. L., Roccaforte, F. & Giannazzo, F. Recent advances in seeded and seed-layer-free atomic layer deposition of high-K dielectrics on graphene for electronics. *C* **5**, 53 (2019).
29. Tang, X. *et al.* Damage evaluation in graphene underlying atomic layer deposition dielectrics. *Sci. Rep.* **5**, 15523 (2015).
30. Yang, L. *et al.* How important is the metal-semiconductor contact for schottky barrier transistors: a case study on few-layer black phosphorus?. *ACS Omega* **2**, 4173–4179 (2017).
31. Profijt, H. B., Potts, S. E., van de Sanden, M. C. M. & Kessels, W. M. M. Plasma-assisted atomic layer deposition: basics, opportunities, and challenges. *J. Vac. Sci. Technol. A* **29**, 050801 (2011).
32. Kim, H. & Oh, IK, Review of plasma-enhanced atomic layer deposition: Technical enabler of nanoscale device fabrication. *Jpn. J. Appl. Phys.* **53**, 03DA01 (1014).
33. Oh, I. K. *et al.* Hydrophobicity of rare oxides grown by atomic layer deposition. *Chem. Mater.* **27**, 148–156 (2015).
34. Nayfeh, O. M., Marr, T. & Dubey, M. Impact of plasma-assisted atomic-layer deposited gate dielectric on graphene transistors. *IEEE Electron. Dev. Lett.* **32**, 473–475 (2011).
35. Vangala, S., Siegel, G., Prusnick, T. & Snure, M. Wafer scale BN on sapphire substrates for improved graphene transport. *Sci. Rep.* **8**, 8842 (2018).
36. Paduano, Q. *et al.* Metalorganic chemical vapor deposition of few-layer sp^2 bonded boron nitride films. *J. Crys. Grow.* **449**, 148 (2016).
37. Kaniyoor, A. & Ramaprabhu, S. A Raman spectroscopic investigation of graphite oxide derived graphene. *AIP Adv.* **2**, 032183. https://doi.org/10.1063/1.4756995 (2012).
38. Liu, Z. *et al.* Ultrathin high-temperature oxidation-resistant coatings of hexagonal boron nitride. *Nat. Commun.* **4**, 2541. https://doi.org/10.1038/ncomms3541 (2013).
39. Glavin, N. R. *et al.* Synthesis of few-layer, large area hexagonal-boron nitride by pulsed laser deposition. *Thin Solid Films* **572**, 245–250 (2014).
40. Moon, O. M., Kang, B. C., Lee, S. B. & Boo, J. H. Temperature effect on structural properties of boron oxide thin films deposited by MOCVD method. *Thin Solid Films* **464–465**, 164–169 (2004).
41. Lafkioti, M. *et al.* Graphene on a hydrophobic substrate: Doping reduction and hysteresis suppression under ambient conditions. *Nano Lett.* **10**, 1149–1153 (2010).
42. Wehling, T. O., Katsnelson, M. I. & Lichtenstein, A. I. First-principles studies of water adsorption on graphene: The role of the substrate. *Appl. Phys. Lett.* **93**, 202110 (2008).
43. Lee, Y. G. *et al.* Fast transient charging at the graphene/SiO$_2$ interface causing hysteretic device characteristics. *Appl. Phys. Lett.* **98**, 183508 (2011).
44. Li, X. *et al.* Large-area synthesis of high quality and uniform graphene films on copper foil. *Science* **324**, 1312–1314 (2009).

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Author contributions

S.V. and M.S. prepared the manuscript. S.V. fabricated devices. M.S. planned the research, grew B.N. and analyzed data. A.C. tested devices, K.L. performed ALD, T.P. performed Raman measurements, and G.G. performed XPS. All authors read and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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