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Material Synthesis and Device Aspects of Monolayer Tungsten Diselenide

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In this paper, we investigate the synthesis of WSe_2 by chemical vapor deposition and study the current transport and device scaling of monolayer WSe_2. We found that the device characteristics of the back-gated WSe_2 transistors with thick oxides are very sensitive to the applied drain bias, especially for transistors in the sub-micrometer regime. The threshold voltage, subthreshold swing, and extracted field-effect mobility vary with the applied drain bias. The output characteristics in the long-channel transistors show ohmic-like behavior, while that in the short-channel transistors show Schottky-like behavior. Our investigation reveals that these phenomena are caused by the drain-induced barrier lowering (short-channel effect). For back-gated WSe_2 transistors with 280 nm oxide, the short-channel effect appears when the channel length is shorter than 0.4 µm. This extremely long electrostatic scaling length is due to the thick back-gate oxides. In addition, we also found that the hydrogen flow rate and the amount of WO_3 precursor play an important role in the morphology of the WSe_2. The hole mobility of the monolayer WSe_2 is limited by Columbic scattering below 250 K, while it is limited by phonon scattering above 250 K. These findings are very important for the synthesis of WSe_2 and accurate characterization of the electronic devices based on 2D materials.

WSe_2 is an important member of the transition metal dichalcogenide (TMDC) family due to its smaller effective electron and hole masses compared to most of the other TMDCs[1], and more importantly due to its ambipolar characteristics[2]. The small effective mass implies high carrier mobilities. The hole mobility of WSe_2 is reported to reach 500 cm^2/V-s at room temperature and 2.1×10^3 cm^2/V-s at 5 K[3,4]. The ambipolar conduction is essential for complementary metal-oxide semiconductor (CMOS) circuits such as inverters, since most of the TMDCs (such as MoS_2, $MoSe_2$, and WS_2), are naturally n-type doped. Although $MoTe_2$ and black phosphorus have also been reported to show p-type conduction[5–8], these materials are less stable in ambient conditions. Electrical properties of WSe_2 including quantum oscillations, carrier mobilities, contacts, and polarity controls, have been studied and various electronic devices based on WSe_2, including metal-oxide field-effect transistors (MOSFETs), tunneling devices, bipolar transistors, and integrated circuits, have been demonstrated[2,3,9–22]. However, most of these studies focus on exfoliated WSe_2 flakes. For practical applications, synthesis of large area WSe_2 with controllable layer thickness and quality is essential. There are several recent reports on the growth of thin WSe_2 using chemical vapor deposition (CVD)[23–26], and metal-organic CVD (MOCVD)[27,28]. However, study of the electrical transport of CVD grown WSe_2 is still lacking. In this paper, we systematically investigate the growth of monolayer WSe_2 by CVD and study the current transport of CVD WSe_2, including short-channel effect, temperature dependence of carrier mobility, subthreshold swing, and interface states.

Results and Discussion

Synthesis of CVD WSe_2. Solid precursor WO_3 and Se power were used to synthesize WSe_2 on Si/SiO_2 substrate in a CVD chamber. Various growth conditions have been investigated, including hydrogen flow rate, WO_3 precursor amount, growth temperature, and argon flow rate. We found that these growth parameters can significantly influence the morphology of the WSe_2. Figure 1a–e show the optical images of the synthesized WSe_2 with various hydrogen flow rates and WO_3 precursor amounts. For a given flow rate of argon carrier gas [60 standard cubic centimeters per minute (sccm)], when the hydrogen flow rate increases from 15 sccm to 20 sccm, the grain size of WSe_2 increases dramatically. However, when the hydrogen flow rate further increases to 25 sccm, the grain size decreases and multilayer stacks start to form. This is because selenium has very low chemical reactivity. A

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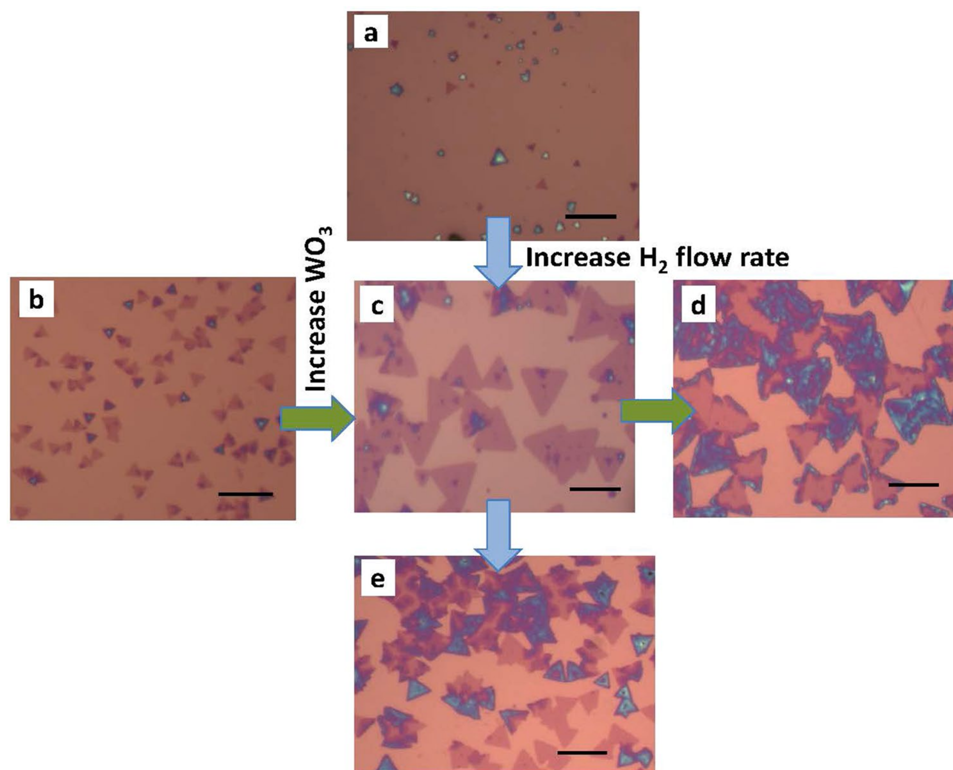

Figure 1. Optical image of CVD WSe_2 grown at various hydrogen flow rates and WO_3 precursor amounts: (**a**) H_2 flow rate 15 sccm, WO_3 quantity 150 mg; (**b**) H_2 flow rate 20 sccm, WO_3 quantity 100 mg; (**c**) H_2 flow rate 20 sccm, WO_3 quantity 150 mg; (**d**) H_2 flow rate 20 sccm, WO_3 quantity 200 mg; (**e**) H_2 flow rate 25 sccm, WO_3 quantity 150 mg. The scale bars in the images are 10 μm.

strong reducer such as hydrogen is needed in the selenization reduction of WO_3. However, if the hydrogen flow rate is too high, the reduction of WO_3 to W happens very quickly and the WO_3 powder only lasts for a very short time, which results in small grains of thick WSe_2. The amount of the precursors loaded in the chamber also plays an important role. For a given amount of Se precursor [(300 milligram (mg)], increasing the quantity of WO_3 precursor from 100 mg to 150 mg can effectively increase the grain size. However, further increase of WO_3 to 200 mg will result in the growth of multi-layer WSe_2.

The optimized growth condition for WSe_2 using this CVD system is 150 mg of WO_3 and 300 mg of Se powder, ambient pressure, 875 °C growth temperature, 70/20 sccm flow of Ar/H_2, and 10~15 minutes growth duration. Perylene-3,4,9,10-tetracarboxylic acid tetra potassium (PTAS) was used as the seeding promoter. With the optimized growth condition, high-quality monolayer WSe_2 was obtained. Figure 2a–d shows the typical optical image, photoluminescence (PL) spectrum, Raman spectrum, and atomic force microscopy (AFM) phase image of the synthesized WSe_2. Bright light emission at ∼1.60 eV and symmetric single PL peak suggest the direct band gap nature of monolayer WSe_2, showing good agreement with other recent reports about PL of monolayer WSe_2[24–26,29–32]. The E_{2g} and A_{1g} modes in the Raman spectrum are at 253.5 cm^{-1} and 264.2 cm^{-1}, respectively. Comparing the peak position with the spectrum obtained from the exfoliated monolayer WSe_2[33], we verify that the WSe_2 film is monolayer. The AFM phase image shows a clear triangle pattern. From the AFM step height profile, the thickness of the WSe_2 is measured as ~0.54 nm, confirming its monolayer character.

Device scaling of the back-gated WSe_2 transistors. WSe_2 transistors with various gate lengths (from 0.1 μm to 5 μm) are fabricated using Pd as metal contacts. Figure 3 illustrated the process flow of the WSe_2 devices. The alignment marks with Ti/Au metals were formed by ebeam lithography, metal deposition and lift-off. Hall-bars and transistors were designed for individual WSe_2 triangles. The source/drain electrodes (40 nm Pd) were formed by ebeam lithography, metal evaporation and lift-off. The WSe_2 channel is defined by ebeam lithography and oxygen plasma etching. The electrical characteristics were measured in vacuum at various temperatures.

Surprisingly, in long-channel transitions (L = 5 μm), the output characteristics (I_D~V_D curves) are linear, indicating ohmic contacts, shown in Fig. 4a, while in short-channel transistors (L = 0.1 μm), the I_D~V_D curves are non-linear, shown in Fig. 4b, resembling Schottky contact characteristics. Since both the long- and short-channel transistors are fabricated on the same wafer with nearly identical WSe_2 and Pd metals. It is very unlikely that they formed different types of contacts. Our further investigation reveals that these non-linear output characteristics in the WSe_2 transistors are not related to the metal contacts, but due to the short-channel effect, which will be discussed below.

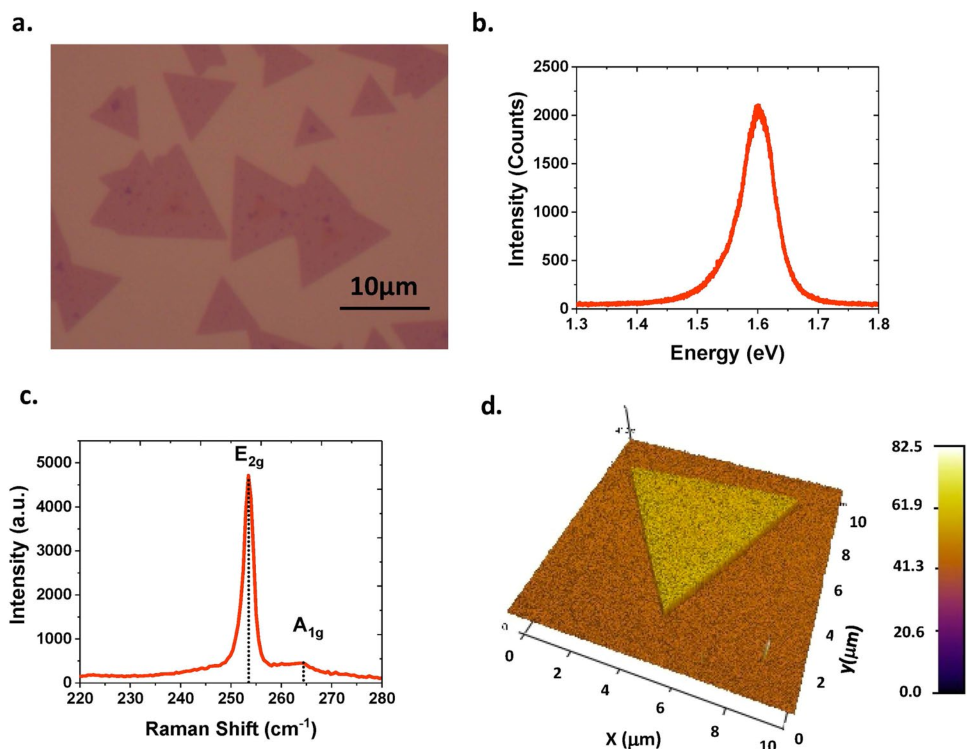

Figure 2. Microscopic characterization of monolayer WSe_2. (**a**) Optical image, (**b**) Photoluminescence spectrum, (3) Raman spectrum, and (4) AFM phase image.

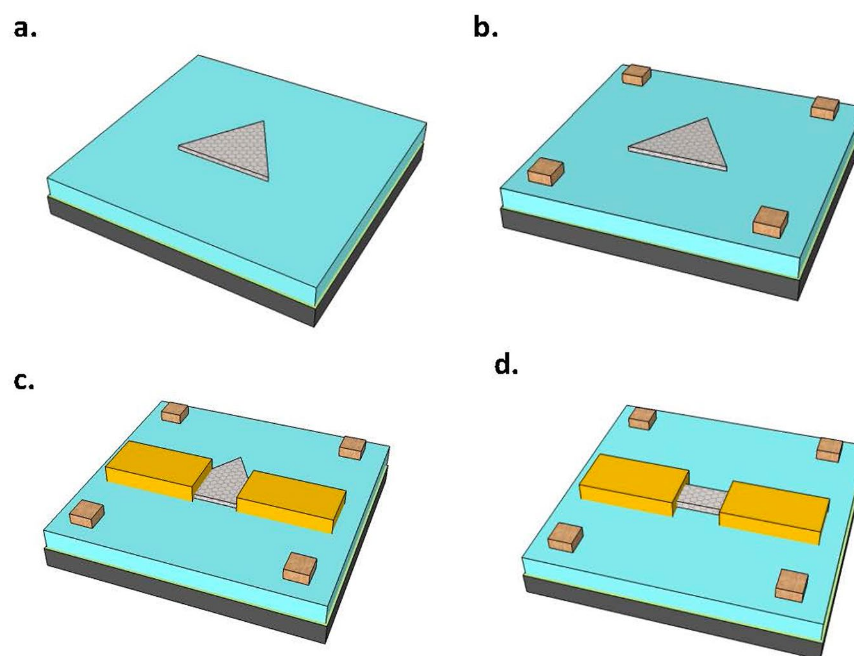

Figure 3. Illustration of the fabrication of the WSe_2 devices. (**a**) Synthesize WSe_2 on SiO_2/Si substrate using CVD. (**b**) Form alignment marks using ebeam lithography, metal deposition and lift-off. (**c**) Form source/drain electrodes using ebeam lithography, metal deposition and lift-off. (**d**) Define channel by ebeam lithography and oxygen plasma etching.

The transfer characteristics (I_D~V_G curves) were measured at various drain voltages for WSe_2 transistors with various gate lengths in a transmission line micro (TLM). A typical SEM image of the TLM structure is shown in Fig. 5a. (Note, in order to avoid the SEM damage on the monolayer WSe_2 in the electronic device, the SEM is taken on a neighboring device with same layout on the same wafer as the device tested electrically). The channel

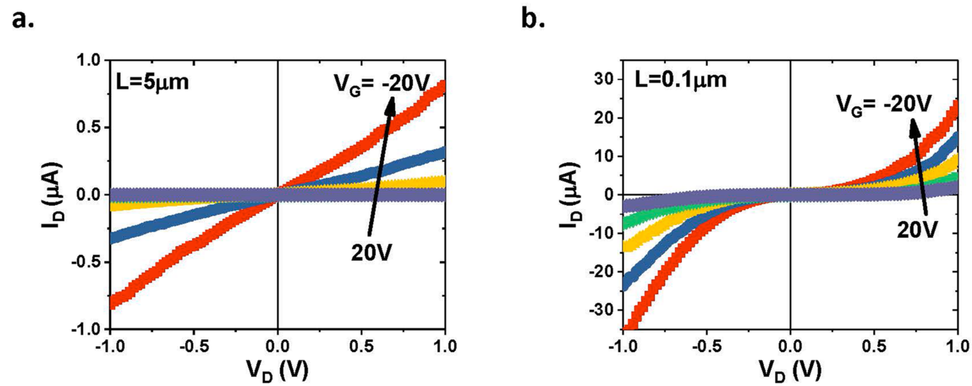

Figure 4. The output characteristics of the CVD WSe_2 transistors with (**a**) channel length L = 5 μm, and (**b**) channel length L=0.1 μm.

conductances at various drain voltages for a long-channel (L = 5 μm) and a short-channel (L = 0.1 μm) transistor, are shown in Fig. 5b and c. For the long-channel transistor, the conductance is nearly independent of the drain voltages. For the short-channel transistor, however, there is a large dispersion of the conductance, especially at the subthreshold regime. Figure 5d plots the threshold voltage as a function of drain voltage for transistors with channel lengths of $L = 0.1\ \mu$m, $0.2\ \mu$m, and $5\ \mu$m. We can see that the threshold voltage increases dramatically as the amplitude of the drain voltage, $|V_D|$, increases for the short channels ($L = 0.1\ \mu$m and $0.2\ \mu$m), while it is nearly constant for the long channel ($L = 5\ \mu$m). This positive shift of the threshold voltage at high drain bias in these short-channel p-type transistors is a result of the fact that the energy barrier between the source and drain is lowered by the high drain voltage and thus the transistors are much easier to turn on. The drain-induced barrier lowering (DIBL) can be estimated using the equation $\mathrm{DIBL} = \frac{V_t^{DD} - V_t^{Low}}{V_{DD} - V_D^{Low}}$, where V_t^{DD} is the threshold voltage measured at a supply voltage (high drain voltage), V_t^{Low} is the threshold voltage measured at a very low drain voltage, V_{DD} is the supply voltage (high drain voltage), V_D^{Low} is the low drain voltage. Here we use drain biases of 0.1 V and 1.1 V to extract the DIBL. Figure 5e shows the DIBL of the back-gated WSe_2 transistor as a function of the channel length. The upturn of the DIBL does not show up until the channel length is shorter than 0.4 μm. Since the back-gate oxide is very thick (280 nm in this case), the electrostatic scaling length is very long. The electrostatic scaling length can be estimated by the equation $\lambda = \sqrt{t_{ox} t_s \varepsilon_s / \varepsilon_{ox}}$, where t_{ox} is the oxide thickness, t_s is the semiconductor thickness, ε_s is the semiconductor dielectric constant, and ε_{ox} is the oxide dielectric constant[34,35]. For the back-gated WSe_2 transistors, assuming $t_{ox} = 280$ nm, $t_s \approx 0.54$ nm, $\epsilon_s \approx 7$, and $\epsilon_{ox} \approx 3.9$, respectively, the electrostatic scaling length is estimated as $\lambda \approx 0.064$ μm. For a planar device, the minimum channel length needed to preserve the long-channel behavior is typically 4–5 times the electrostatic scaling length, which corresponds to $L = 0.26$~0.32 μm in this case. This is consistent with our DIBL results, which reveal that the short-channel effect starts to show up when the channel is shorter than 0.4 μm. As the energy barrier between source and drain reduces, the drain current will increase exponentially. This explains the dramatic increase of the drain current at high drain voltages in the I_D~V_D plots for the short-channel transistors, shown in Fig. 4b.

Carrier mobility in CVD WSe_2. The carrier mobility is an important indicator of the quality of the semiconductor. The carrier mobility of the CVD WSe_2 is studied in the long-channel transistors to eliminate the possible short-channel effects, and the conductances were measured using the four-point method to minimize the impact of the contact resistances. Figure 6a shows the SEM image of a typical Hall-bar device. The four-point conductance as a function of gate voltage measured of a WSe_2 Hall-bar device at various temperatures is shown in Fig. 6b. Note the SEM and conductance are taken on two separate devices with the same layout on the same wafer to avoid the impact of SEM scan on the electrical performance of the device. The field-effect mobility is extracted from the four-point conductance, using the equation $\mu = \frac{1}{(W/L)C_{ox}} \frac{\partial \sigma}{\partial V_G}$, where σ is the four-point conductance, V_G is the gate voltage, W is channel width, L is the channel length, and C_{ox} is the oxide capacitance[36]. The extracted field effect mobility as a function of gate voltage is shown in Fig. 6c. As the transistor is biased further into the inversion, the mobility increases because of the screening effect due to the inversion charge, which reduces the Coulomb scattering. The temperature dependence of the mobility shows a turn-around behavior at 250 K, shown in Fig. 6d. At low temperatures, the mobility increases with increasing temperature, and at temperatures above 250 K, the mobility decreases with increasing temperature. At low temperatures, Coulomb scattering dominates. When the temperature increases, the carrier velocity increases, which can reduce the influence of the Coulomb scattering from the charged impurities. At high temperatures, phonon scattering dominates. Increasing temperature will increase the lattice vibration and reduce the mobility. Seven Hall-bar devices were measured to determine the mobility and carrier density. At $V_G - V_T = -30\ V$, i.e. carrier density of ~$2.3 \times 10^{12}\ \mathrm{cm}^{-2}$, the average mobility is ~$24.8\ \mathrm{cm}^2$/V-s, the maximum mobility is $46.1\ \mathrm{cm}^2$/V-s, and the minimum mobility is $7.9\ \mathrm{cm}^2$/V-s. Note, these electrical characteristics were measured after source/drain formation and before the channel is etched into rectangular shape. After the sample experienced additional process steps, including lithography, oxygen plasma etching and resist strip, and additional characterizations such as SEM, the measured mobilities of the Hall-bar

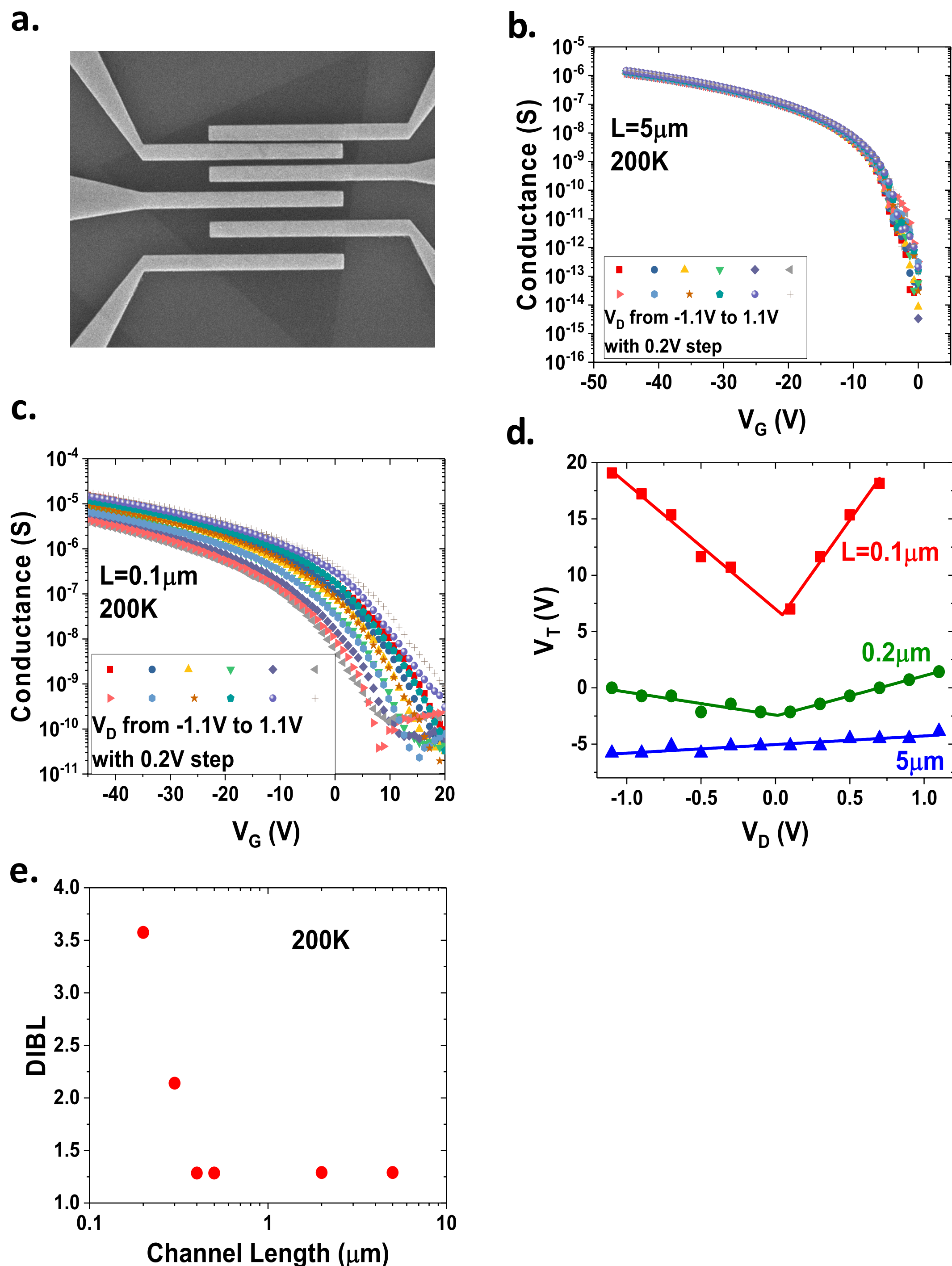

Figure 5. Short-channel effect in WSe_2 transistors. (**a**) SEM image of a WSe_2 TLM structure consisting of five transistors with various channel lengths. (**b**) Conductance as a function of gate voltage in a long-channel transistor (L = 5 μm) measured at various drain voltages. (**c**) Conductance as a function of gate voltage in a short-channel transistor (L = 0.1 μm) measured at various drain voltages. (**d**) Threshold voltage as a function of drain voltage for WSe_2 transistors with various channel lengths from 0.1 μm to 5 μm. (**e**) Drain-induced barrier lowering (DIBL) of the WSe_2 transistors as a function of channel length.

devices are significantly lower, as shown in Fig. S1 in the supplementary information. One possible cause of this mobility degradation is that the additional process steps and the high-energy electron beam in SEM degraded the monolayer WSe_2 channel. The other possible reason for the lower extracted mobility after channel-cut is that there are parasitic current path in the triangular-shaped channel before the channel-cut, which may cause over-estimation of the channel mobility. The gate voltage and temperature dependence of the channel mobilities in a WSe_2 Hall-bar devices after channel-cut and SEM scan are shown in Fig. S2. The mobilities of the WSe_2 device after channel-cut show similar temperature and gate voltage dependence as the one before the channel-cut.

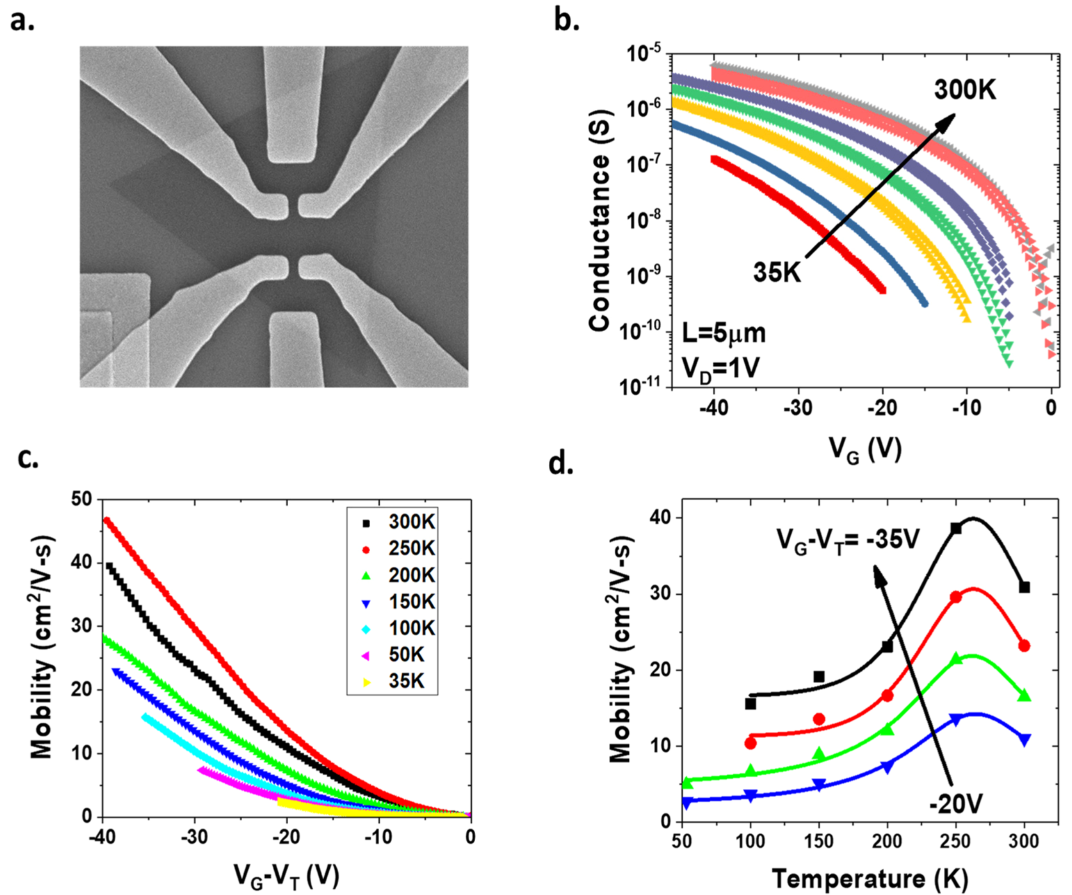

Figure 6. Carrier mobility of CVD WSe_2. (**a**) SEM image of a WSe_2 Hall-bar device. (**b**) Four-point conductance as a function of gate voltage measured at various temperatures. (**c**) Extracted field-effect mobility as a function of gate overdrive, $V_G - V_T$, at various temperatures. (**d**) Temperature dependence of the field-effect mobility at various gate overdrives.

Interface states of the WSe_2 transistors. The interface trap density is another key parameter for semiconductors, which directly impacts the performance of metal-oxide field-effect transistors (MOSFETs), tunneling field-effect transistors (TFETs), and tunneling diodes. The interface trap density of the CVD WSe_2 is evaluated by measuring the subthreshold swing at various temperatures on the long-channel transistors. Figure 7a shows the I_D~V_D curves measured at various temperatures for a transistor with gate length $L = 5\,\mu$m. The subthreshold swing is defined as the gate voltage required to vary the subthreshold current by one decade: $SS = \partial V_G/\partial log(I_D)$, where I_D is the drain current at the subthreshold regime. Figure 7b shows the measured subthreshold swing as a function of gate voltage. The subthreshold swing is typically a function of depletion capacitance, C_D, and temperature. If there are interface states, an interface-state capacitance, C_{it}, will be in parallel with the C_D. Then the subthreshold swing can be modeled as $SS = \frac{kT}{q} ln(10)\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right)$[36]. For transistors with atomically thin channel (monolayer WSe_2), it is assumed that the device is fully depleted and $C_D \approx 0$. Then the interface capacitance, C_{it}, can be extracted. The interface trap density is related to C_{it} by the equation $D_{it} = \frac{C_{it}}{q}$, where q is the elementary charge. Figure 7c shows the extracted interface trap density, D_{it}, as a function of gate overdrive, $V_G - V_T$, at various temperatures. As the gate overdrive, $V_G - V_T$, decreases, i.e. as the Fermi level at the WSe_2/oxide interface approaches the valence band edge, the interface trap density increases, which is similar to the energy distribution of the interface traps in silicon.

The threshold voltages of these back-gated WSe_2 transistors are also strongly dependent on the temperatures. Figure 7d shows the threshold voltage as a function of temperature. The threshold voltage increases monotonically as the temperature increases from 35 K to 300 K. This can be explained by the temperature dependence of the interface trapped charges. The interface state typically has two types: the donor-like and the acceptor-like interface states. The donor-like interface states are neutral when filled with electrons and positive when empty, whereas the acceptor-like interface states are negative when filled and neutral when empty. Assuming that the interface states below the midgap E_i are donor-like, while those above E_i are acceptor-like, similar to silicon, the interface states will be positively charged at threshold voltage in p-type transistors, where the Fermi level is below the midgap. This will result in a negative shift in the threshold voltage as compared to the one without interface states. As the temperature increases, the Fermi level is closer to the mid-gap at the threshold voltage, and the total amount of the positive trapped charges reduces, resulting in positive shift of the threshold voltages. The desorption of the moisture from the WSe_2 surface as the samples warm up could also cause a threshold voltage shift in these back-gated transistors.

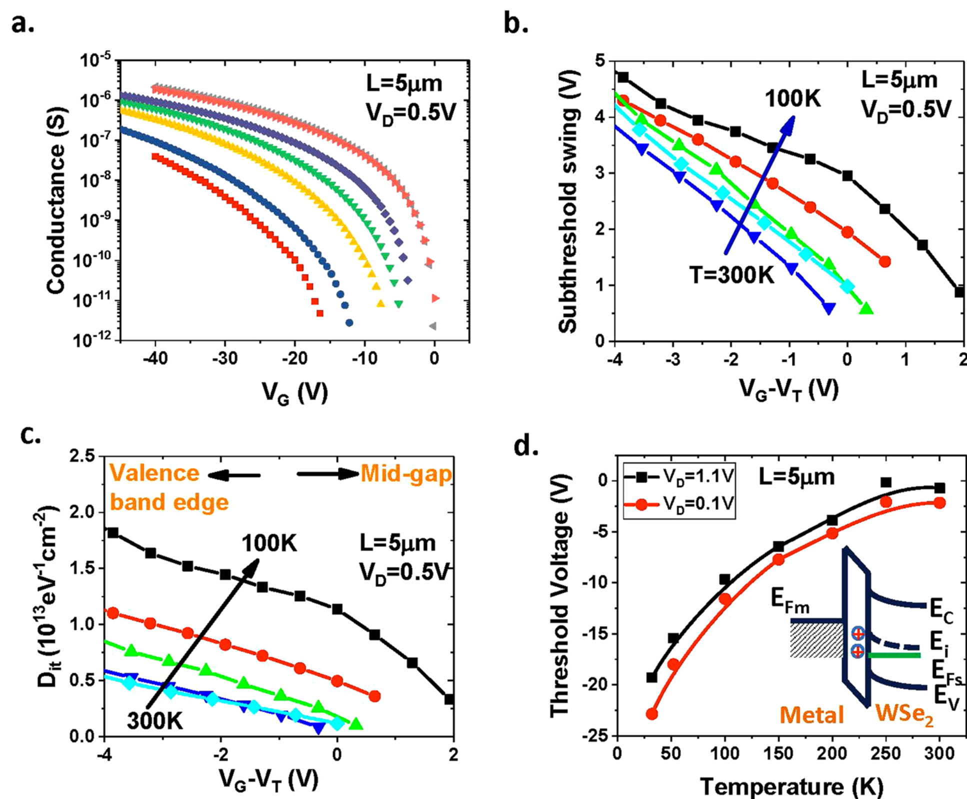

Figure 7. Interface states in back-gated WSe_2 transistors. (**a**) Two-point conductance as a function of gate voltage measured at various temperatures. (**b**) Subthreshold swing as a function of gate overdrive, $V_G - V_T$, at various temperatures. (**c**) Extracted interface trap density as a function of gate overdrive. (**d**) Temperature dependence of the threshold voltage. The inset illustrates the positive interface trapped charges located at the WSe_2/oxide interface when the gate is biased at the threshold voltage.

Conclusion

In summary, we have systematically investigated the synthesis of monolayer WSe_2 using CVD and studied the electric transport of CVD WSe_2. We found that short-channel effect plays an important role in the back-gated WSe_2 transistors when the channel length is in the sub-micrometer regime. The drain-induced barrier lowering can result in variations of the threshold voltages and over- or under-estimation of the carrier mobilities. This short-channel effect can also lead to misjudgment of the metal contacts, as the output characteristics of a transistor with ohmic contacts can show Schottky-like behavior. For back-gated WSe_2 transistors with 280 nm gate oxide, the DIBL starts to show an upturn when the channel length is shorter than 0.4 μm. This extremely long electrostatic scaling length is due to the thick oxide. These findings will be very important for accurate and unified characterization and analysis of 2D electronic devices with back-gate structures. In addition, we also found that the hydrogen flow rate and the amount of WO_3 precursor can significantly influence the morphology of the WSe_2. Large work function metal Pd forms ohmic contact to the monolayer WSe_2. The interface trap density of WSe_2 was extracted from the subthreshold swings. The interface trap density of CVD WSe_2 increases as the energy level approaches the valence band edge. These findings will enrich the knowledge of electric transport in CVD WSe_2 and the scaled electronic devices based on monolayer TMDCs.

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Author Contributions
Z.Y. synthesized the WSe_2 film by CVD, designed, fabricated and measured the devices. J.L. carried out the AFM measurement and participated the device fabrication. K.X. did the metal evaporation, lift-off, SEM and part of electrical characterization. E.C. carried out the ebeam lithography and metal deposition. W.Z. initiated the project, performed electrical characterization and wrote the manuscript with input from Z.Y.

Additional Information
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