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Scaling behavior of InAlN/GaN HEMTs on silicon for RF applications

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Due to the low cost and the scaling capability of Si substrate, InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions. In this paper, a high-performance 50-nm-gate-length InAlN/GaN HEMT on Si with a high on/off current (I_{on}/I_{off}) ratio of 7.28×10^6, an average subthreshold swing (SS) of 72 mV/dec, a low drain-induced barrier lowing (DIBL) of 88 mV, an off-state three-terminal breakdown voltage (BV_{ds}) of 36 V, a current/power gain cutoff frequency (f_T/f_{max}) of 140/215 GHz, and a Johnson's figure-of-merit (JFOM) of 5.04 THz V is simultaneously demonstrated. The device extrinsic and intrinsic parameters are extracted using equivalent circuit model, which is verified by the good agreement between simulated and measured *S*-parameter values. Then the scaling behavior of InAlN/GaN HEMTs on Si is predicted using the extracted extrinsic and intrinsic parameters of devices with different gate lengths (L_g). It presents that a f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study, and an improved f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrown ohmic contact technology and 30% decreased parasitic capacitance. This study confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

Abbreviations

HEMT	High-electron-mobility transistor
I_{on}/I_{off}	On/off current ratio
SS	Subthreshold swing
DIBL	Drain-induced barrier lowing
BV_{ds}	Off-state three-terminal breakdown voltage
f_T/f_{max}	Current/power gain cutoff frequency
JFOM	Johnson's figure-of-merit
g_m	Extrinsic transconductance
MOCVD	Metalorganic chemical vapor deposition
SEM	Scanning electron microscopy
I_d	Drain current
I_g	Gate current
L_g	Gate length
L_{sd}	Source-drain spacing
V_{gs}	Gate-source voltage
V_{ds}	Drain-source voltage
R_{on}	On-resistance
SCEs	Short-channel effects
$\|h_{21}\|^2$	Current gain
U	Unilateral gain
MSG	Maximum stable gain

InAlN/GaN high-electron-mobility transistors (HEMTs) on silicon substrate have attracted more and more attentions due to the low cost and the scaling capability of Si substrate[1–4]. Li et al. demonstrated an InAlN/GaN HEMT on Si with a gate length (L_g) of 55 nm and a source-drain spacing (L_{sd}) of 175 nm[5] using n^{++}-GaN regrowth source/drain contacts. The device presents a maximum drain current ($I_{d,\,max}$) of 2.8 A/mm, a peak extrinsic

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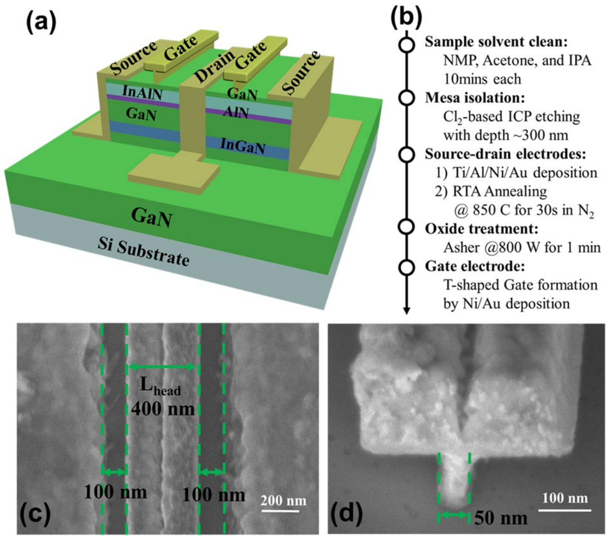

Figure 1. **(a)** Schematic of fabricated InAlN/GaN HEMT; **(b)** Detailed device fabrication steps; **(c)** a plan-view scanning electron microscopy (SEM) image of the InAlN/GaN HEMT with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm; **(d)** A SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

transconductance (g_m) of 0.66 S/mm, and a current/power gain cutoff frequency (f_T/f_{max}) of 250/204 GHz. Xie et al. reported that a record f_T of 310 GHz was achieved on an InAlN/GaN HEMT on Si with a 40-nm gate length[6]. Cui et al. demonstrated an 80-nm-gate-length InAlN/GaN HEMT on Si with a record high on/off current (I_{on}/I_{off}) ratio of 1.58×10^6, a steep subthreshold swing (SS) of 65 mV/dec, and a f_T of 200 GHz, resulting in a record high $f_T \times L_g = 16$ GHz μm[7]. Chowdhury et al. demonstrated a complementary logic circuit (an inverter) on a GaN-on-Si platform with a record maximum voltage gain of 27 V/V at an input voltage of 0.59 V with $V_{DD} = 5$ V[8]. Xie et al. reported an InAlN/GaN HEMT on Si with a f_T of 210 GHz and a three-terminal off-state breakdown voltage (BV_{ds}) of 46 V, leading to a record high Johnson's figure-of-merit (JFOM = $f_T \times BV_{ds}$) of 8.8 THz V[9]. Then et al.reported the high f_T/f_{max} of 190/300 GHz was achieved on the e-mode high-k InAlN/GaN transistor on 300 mm Si substrate[10].

However, to the best of our knowledge, the highest f_T/f_{max} of 454/444 GHz and 348/340 GHz were achieved on 20-nm-gate-length AlN/GaN HEMT[11] and 27-nm-gate-length InAlN/GaN HEMTs on SiC[12], respectively. Although excellent performances have been demonstrated, InAlN/GaN HEMTs on Si still presents much room to be improved compared with GaN HEMTs on SiC substrate. The InAlN barrier can be grown lattice-matched to GaN when the In component is 17%, which makes it easier grow than AlN on GaN[13]. The InAlN/GaN heterostructure also exhibits higher quantum well polarization-induced charge than AlGaN/GaN heterostructure, resulting in higher channel electron density and drain current[14,15]. In addition, compared with AlGaN/GaN, a thinner InAlN barrier in InAlN/GaN HEMTs not only can offer higher frequency performance with an improved device transconductance, but also can suppress the short-channel effect with the reduced gate-to-channel distance[16,17]. Hence, exploring the possible limiting factors of InAlN/GaN HEMTs on Si is significant to further improve the device performance. In this paper, high-performance InAlN/GaN HEMTs on Si are demonstrated. The extrinsic and intrinsic parameters of devices with different gate lengths are extracted and the scale behavior of InAlN/GaN HEMTs on Si is predicted. It presents that a f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study, and an improved f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMTs with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This confirms the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

Experiment

Figure 1a shows the lattice-matched $In_{0.17}Al_{0.83}N$/GaN heterostructure, which is grown on a Si substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial layer structure consists of a 2-nm GaN cap layer, an 8-nm $In_{0.17}Al_{0.83}N$ barrier layer, a 1-nm AlN interlayer, a 15-nm GaN channel layer, a 4-nm $In_{0.12}Ga_{0.88}N$ back-barrier layer, and a 2-μm undoped GaN buffer layer[18]. The electron sheet concentration and electron mobility measured by Hall measurements were 2.28×10^{13} cm^{-2} and 1205 cm^2/V s, respectively.

Figure 1b shows the detailed device fabrication steps. The device fabrication started with mesa isolation using Cl_2/CH_4/He/Ar inductively coupled plasma etching. Then Ti/Al/Ni/Au stack was deposited and annealed at 850 °C for 40 s in N_2 to form the alloyed ohmic contacts. The ohmic contact resistance is 0.3 Ω mm. An oxygen plasma treatment was then applied to form the oxide layer on top of the InAlN layer, which can effectively reduce the gate leakage current and improve RF erformance[19–22]. Finally, a Ni/Au T-shaped gate with a gate width (W_g) of 2×20 μm was fabricated by electron beam lithography. Figure 1c shows a plan-view scanning electron microscopy

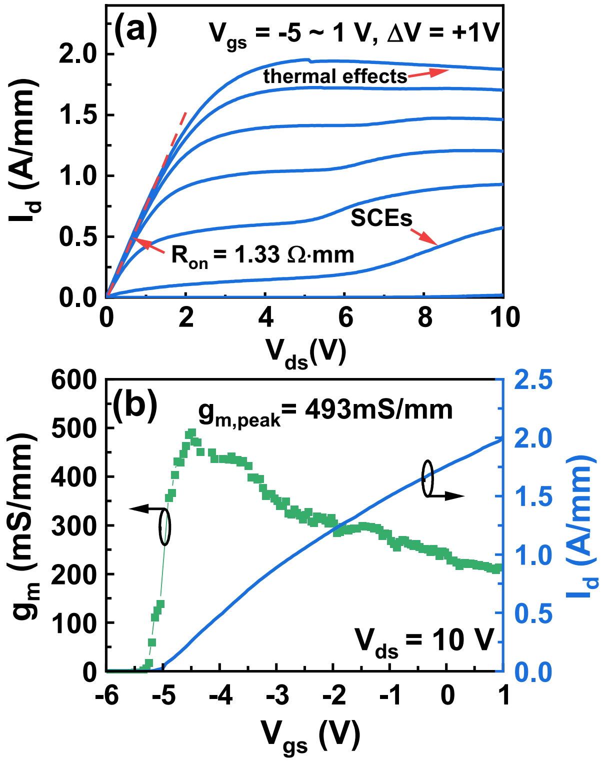

Figure 2. **(a)** Output characteristic, **(b)** the extrinsic transconductance g_m, and the transfer characteristic at $V_{ds} = 10$ V of the InAlN/GaN HEMT with a 50-nm gate length.

(SEM) image of the InAlN/GaN HEMT with a gate head length (L_{head}) of 400 nm and a source-drain spacing (L_{sd}) of 600 nm. Figure 1d shows a SEM image of T-shaped gate structure depicting a gate footprint of 50 nm.

Results and discussion

DC performance. The DC current–voltage (I–V) measurements are carried out by using an Agilent B1500A semiconductor parameter analyzer. Figure 2a shows the output characteristic of the InAlN/GaN HEMT with a 50-nm gate length. The device on-resistance (R_{on}) extracted at gate-source (V_{gs}) of 0 V and drain-source voltage (V_{ds}) between 0 and 0.5 V is 1.33 Ω·mm. The gate-to-channel distance t_{bar} (including a 2-nm GaN, an 8-nm InAlN, and a 1-nm AlN) is 11 nm. Since L_g is 50 nm, the device presents an aspect ratio (L_g/t_{bar}) of 4.5. Due to the low L_g/t_{bar}, the short-channel effects (SCEs) start to appear when V_{ds} is larger than 5 V and V_{gs} is between − 4 to − 1 V. At $V_{gs} = 1$ V, drain current (I_d) in saturation region presents a decrease with increased V_{ds}, an indication of the thermal effect.

Figure 2b shows the transfer characteristic with the extracted extrinsic transconductance (g_m) of the InAlN/GaN HEMT with a 50-nm gate length at $V_{ds} = 10$ V. The maximum saturation drain current ($I_{d,\,max}$) is 2.01 A/mm at $V_{gs} = 1$ V and $V_{ds} = 10$ V. The g_m perk ($g_{m,\,peak}$) is 493 mS/mm. To the best of our knowledge, the record high $I_{d,\,max}$ of 2.8 A/mm and $g_{m,peak}$ of 660 mS/mm were achieved on a 55-nm-gate-length InAlN/GaN HEMT on Si with regrowth technology and L_{sd} of 175 nm[5]. The lower I_d and $g_{m,peak}$ in this study result from the regrowth-free technology and the larger source-drain spacing ($L_{sd} = 600$ nm).

Figure 3a shows the transfer and gate current (I_g) characteristics in semi-log scale of the InAlN/GaN HEMT with a 50-nm gate length at $V_{ds} = 5$ V and 10 V, respectively. At $V_{ds} = 10$ V, the device off-current (I_{off}) is 2.76×10^{-7} A/mm and the I_{on}/I_{off} ratio is 7.28×10^6, which are higher than the record reported values (I_{off} of 7.12×10^{-7} A/mm and I_{on}/I_{off} ratio of 1.58×10^6) achieved from the InAlN/GaN HEMT on Si[7]. An average subthreshold swing (SS) of 72 mV/dec over more than two orders of I_d is extracted from the transfer curve. The drain-induced barrier lowering (DIBL) of 88 mV/V is extracted at $I_d = 10$ mA/mm between $V_{ds} = 10$ V and $V_{ds} = 5$ V, which is the lowest value among the reported GaN HEMTs on Si. The lowest DIBL value suggests a suppressed SCEs for the sub-100 nm gate-length device. Figure 3b shows the off-state three-terminal breakdown characteristic of the 50-nm InAlN/GaN HEMT measured at $V_{gs} = -8$ V. The device features a BV_{ds} of 36 V at a drain leakage current of 1 mA/mm.

RF performance. The device RF performance is measured with a frequency range from 1 to 65 GHz. The network analyzer is calibrated using a two-port short/open/load/through method. On-wafer open and short structures is used to eliminate the effects of parasitic elements. Figure 4a shows the current gain ($|h_{21}|^2$), unilateral gain (U), and the maximum stable gain (MSG) as a function of frequency at $V_{ds} = 10$ V, $V_{gs} = -3$ V after de-embedding. f_T/f_{max} of 140/215 GHz for the InAlN/GaN HEMT with a 50-nm gate length is obtained by

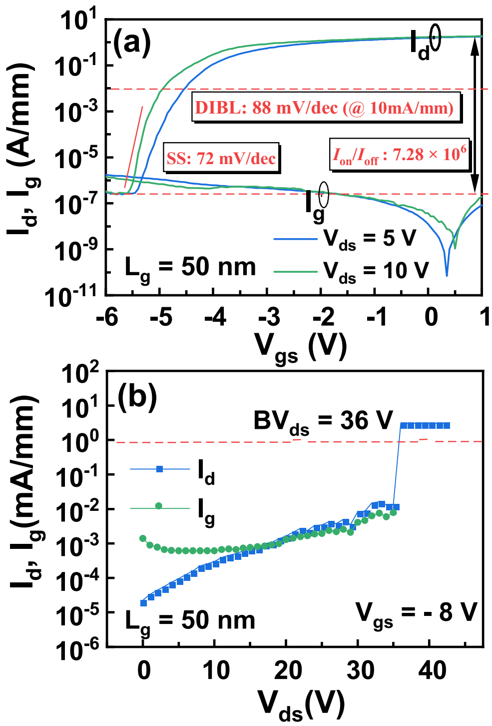

Figure 3. (**a**) The transfer and gate current characteristics in semi-log scale at $V_{ds} = 10$ V and 5 V, (**b**) the I_d and I_g as a function of V_{ds} at $V_{gs} = -8$ V of the InAlN/GaN HEMT with a 50-nm gate length. A BV_{ds} of 36 V was determined.

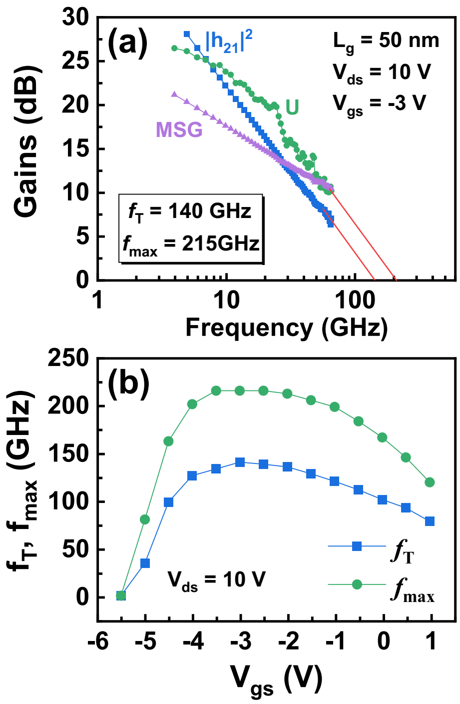

Figure 4. (**a**) RF performance of the InAlN/GaN HEMT with a 50-nm gate length at $V_{gs} = -3$ V and $V_{ds} = 10$ V with $f_T/f_{max} = 140/215$ GHz. (**b**) The f_T and f_{max} as a function of V_{gs}.

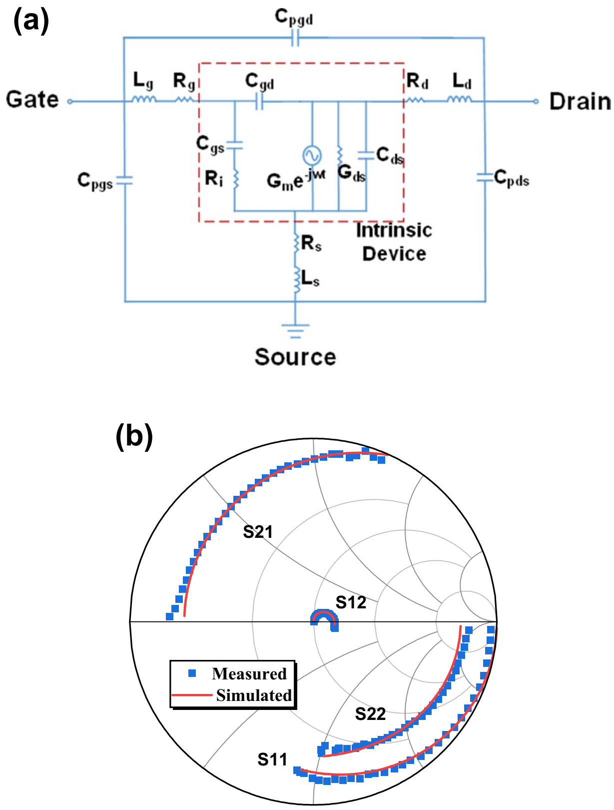

Figure 5. **(a)** Equivalent-circuit model for InAlN/GaN HEMT. The intrinsic elements are shown in the red dashed box. **(b)** Comparison of the simulated and measured S-parameters for the InAlN/GaN HEMT with a 50-nm gate length at V_{ds} = 10 V and V_{gs} = − 3 V.

extrapolation of $|h_{21}|^2$ with a − 20 dB/dec slope. An $(f_T \times f_{max})^{1/2}$ of 173 GHz is obtained, which is the highest record value among the reported InAlN/GaN HEMTs on Si with regrowth-free ohmic contact technology. To the best of our knowledge, a high $(f_T \times f_{max})^{1/2}$ of 226 GHz (f_T/f_{max} = 250/204 GHz) was achieved on a 55-nm InAlN/GaN HEMT on Si[5], and a high $(f_T \times f_{max})^{1/2}$ of 239 GHz (f_T/f_{max} = 190/300 GHz) was demonstrated on the e-mode high-k InAlN/GaN MISHEMTs with L_g of 50 nm[10]. The ohmic contact regrowth technology was used in both reported devices. Here for our device, the alloyed ohmic resistance (R_C: 0.3 Ω mm) is higher than the reported regrowth ohmic contact resistance (R_C: 0.05 Ω mm)[5]. This presents a high potential for the RF performance improvement by further decreasing the ohmic contact resistance. Due to f_T/f_{max} of 140/215 GHz, products of $f_T \times L_g$ and $f_{max} \times L_g$ of 7.0 and 10.75 GHz·µm are achieved, respectively. Although neither passivation nor field plate technology is used, the 140-GHz InAlN/GaN HEMT with an BV_{ds} of 36 V presents a Johnson's figure-of-merit (JFOM = $f_T \times BV_{ds}$) of 5.04 THz·V. Figure 4b shows the measured f_T and f_{max} of the 50-nm InAlN/GaN HEMT as a function of V_{gs}. Both f_T and f_{max} show a gradual decrease compared with their peak values, presenting a good device linearity.

Equivalent circuit model. The classical 16-element equivalent-circuit model is used for the InAlN/GaN HEMT, as shown in Fig. 5a[23,24]. Based on this model, the device extrinsic and intrinsic parameters are extracted in Table 1[23–25]. The slight discrepancy between the simulated and measured *S*-parameter values is observed in Fig. 5b, verifying the accuracy of the extracted extrinsic and intrinsic parameters. The f_T and f_{max} can be calculated using[23,26]

$$f_T = \frac{G_m/G_0}{2\pi((C_{gs}+C_{gd})(1/G_0+(R_s+R_d))+(C_{gd}\cdot G_m/g_0)(R_s+R_d))},$$
$$f_{max} = \frac{f_T}{2\sqrt{(R_s+R_g+R_i)\cdot G_0+2\pi f_T R_g C_{gd}}}. \quad (1)$$

where G_m and G_0 are the intrinsic transconductance and drain-source conductance, respectively; C_{gs} and C_{gd} are the gate-source and gate-drain parasitic capacitance, respectively; R_s, R_d, R_g, and R_i are the parasitic source access resistance, drain access resistance, gate electrode resistance, and input resistance, respectively.

Extrinsic parameters	Intrinsic parameters
$C_{pgd} = 1.16$ fF	$C_{gs} = 444$ fF/mm
$C_{pgs} = 26.35$ fF	$C_{gd} = 104$ fF/mm
$C_{pds} = 26.21$ fF	$C_{ds} = 318$ fF/mm
$L_s = 3.17$ pH	$R_i = 0.90\ \Omega$ mm
$L_g = 44.03$ pH	$G_m = 573$ mS/mm
$L_d = 41.30$ pH	$G_0 = 54$ mS/mm
$R_s = 0.43\ \Omega$ mm	$G_m/G_0 = 10.6$
$R_g = 0.26\ \Omega$ mm	$\tau = 1.09$ ps
$R_d = 0.45\ \Omega$ mm	$f_{T,\ model} = 145$ GHz
	$f_{max,\ model} = 218$ GHz

Table 1. The extracted extrinsic and intrinsic parameters for the 50-nm InAlN/GaN HEMTs.

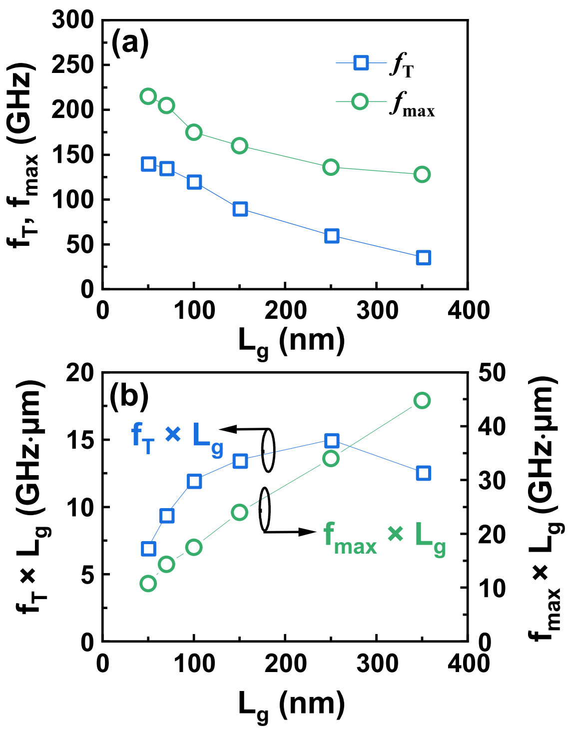

Figure 6. (**a**) Measured f_T and f_{max} as a function of L_g at $V_{gs} = -3$ V and $V_{ds} = 10$ V. (**b**) $f_T \times L_g$ and $f_{max} \times L_g$ as a function of L_g.

The calculated $f_T/f_{max} = 145/218$ GHz is very close to the value ($f_T/f_{max} = 140/215$ GHz) extracted by the extrapolation of $|h_{21}|^2$ with a -20 dB/dec slope, which confirms the excellent RF performance. The high intrinsic transconductance/drain-source conductance (G_m/G_0) ratio of 10.6 contributes to the high f_{max}.

Scaling behavior. The InAlN/GaN HEMTs with L_g between 50 and 350 nm are fabricated. Figure 6a shows the measured f_T/f_{max} of the InAlN/GaN HEMTs with different L_g at $V_{gs} = -3$ V and $V_{ds} = 10$ V. The devices with L_g of 50, 70, 100, 150, 250, and 350 nm present f_T/f_{max} of 140/215, 135/205, 120/170, 90/160, 60/136, 36/128 GHz, respectively. $f_T \times L_g$ and $f_{max} \times L_g$ are obtained in Fig. 6b. A $f_T \times L_g$ peak of 15 GHz μm is achieved on the 250-nm-gate-length InAlN/GaN HEMT with a f_T of 135 GHz. $f_{max} \times L_g$ presents a decrease from 44.8 GHz μm ($L_g = 350$ nm) to 10.75 GHz μm ($L_g = 50$ nm). The decrease of both $f_T \times L_g$ and $f_{max} \times L_g$ as L_g scales down means that the effect of parasitic parameters is more pronounced, thus hindering the improvement of f_T and f_{max}. Due to the large head length of T-shaped gate ($L_{head} = 400$ nm), the transistors features higher f_{max} and $f_{max} \times L_g$.

To shed more light on the scaling behavior, the extrinsic and intrinsic parameters of these devices are further extracted using the equivalent circuit model discussed above. C_{gs} can be separated to two parts: gate-source intrinsic capacitance ($C_{gs,int}$) and gate-source extrinsic capacitance ($C_{gs,\ ext}$). It means $C_{gs} = C_{gs,int} + C_{gs,ext}$[27]. C_{gd} can also be written as $C_{gd} = C_{gd,int} + C_{gd,ext}$. Figure 7 shows the extracted C_{gs} and C_{gd} as a function of L_g. Both C_{gs} and

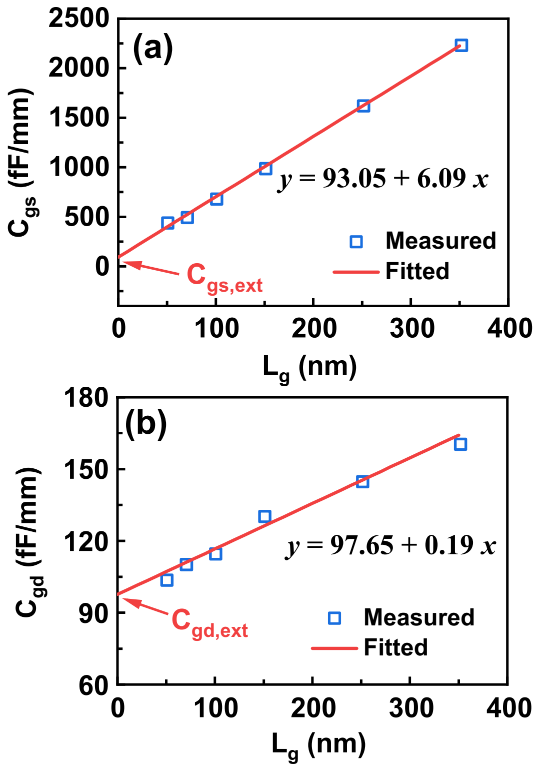

Figure 7. Measured and linear fitted **(a)** gate-source parasitic capacitance C_{gs} and **(b)** gate-drain parasitic capacitance C_{gd} as a function of L_g at $V_{gs} = -3$ V and $V_{ds} = 10$ V.

C_{gd} present a linear dependence upon L_g. By linear fitting, the $C_{gs,ext}$ and $C_{gd,ext}$ are obtained from C_{gs} and C_{gd} at $L_g = 0$ nm[27], as shown in Fig. 7. Here $C_{gs,ext}$ of 93.05 fF/mm and $C_{gd,ext}$ of 97.65 fF/mm are determined, respectively.

The total delay (τ) of transistors can be written as[27,28]

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \tag{2}$$

Here τ is partitioned into three components: transit time (τ_t), parasitic charging delay (τ_{ext}), and parasitic resistance delay (τ_{par}).

τ_t is the transit time under the gate region. It is related to the gate length as well as the electron velocity (v_e) under the gate region, and can be calculated by[27,28]

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{G_m} = \frac{L_g}{v_e} \tag{3}$$

τ_{ext} is parasitic charging delay through $C_{gs,ext}$ as well as $C_{gd,ext}$, and can be written as[27,28]

$$\tau_{ext} = \frac{C_{gs,ext} + C_{gd,ext}}{G_m}. \tag{4}$$

τ_{par} is parasitic resistance delay mainly associated with R_s as well as R_d, and can be written as[27,28]

$$\tau_{par} = C_{gd}(R_s + R_d)\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{G_0}{G_m}\right]. \tag{5}$$

Figure 8 plots τ_t and v_e as a function of L_g calculated from (3). As L_g decreases, τ shows a monotonous drop, which corresponds to the increased f_T. With decreased L_g, v_e increases to a maximum value of 1.08×10^7 cm/s (at $L_g = 150$ nm) and then drop to 0.80×10^7 cm/s (at $L_g = 50$ nm). Figure 9 shows the extracted G_m and G_0 from the equivalent-circuit model as a function of L_g. G_0 shows an increase with decreased L_g. The dependence of G_m and v_e on L_g present the same trend. Based on (3), because C_{gsi} and C_{gdi} linearly depends on L_g, we conclude that the change of G_m is attributed to v_e difference. The same trend of G_m and v_e on L_g is also observed in InAs HEMTs and result from the short channel effect[29–31].

Figure 10 exhibits the calculated τ_t, τ_{ext}, and τ_{par} using (3)–(5). τ_{ext} and τ_{par} is almost unchanged. Conversely, τ_t decreases with decreased L_g and dominates the total delay in all devices. This makes it possible to decrease delay and improve f_T through downscaling of device gate length. However, for the device with L_g below 100 nm,

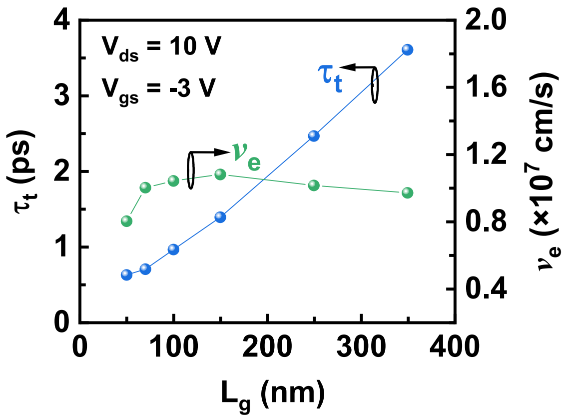

Figure 8. Extracted transit time (τ_t) and electron velocity (v_e) as a function of L_g at $V_{gs} = -3$ V and $V_{ds} = 10$ V.

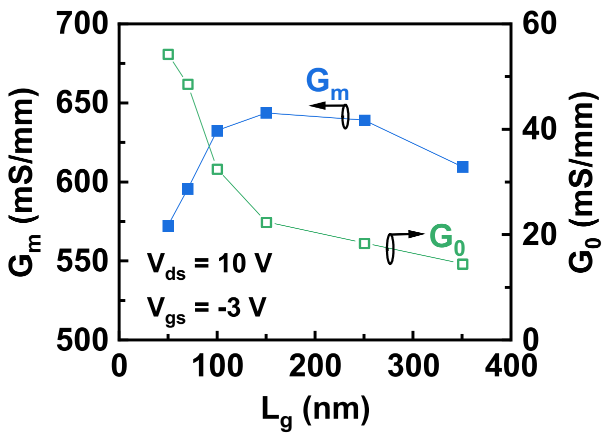

Figure 9. Extracted intrinsic transconductance (G_m) and intrinsic conductance (G_0) as a function of L_g at $V_{gs} = -3$ V and $V_{ds} = 10$ V.

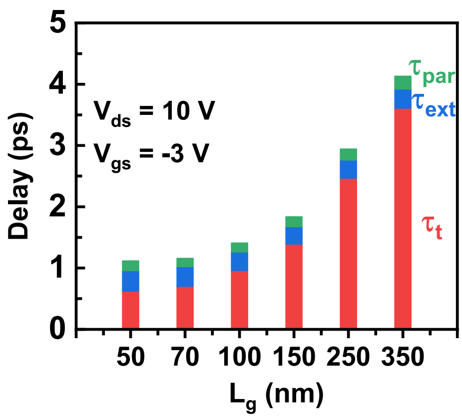

Figure 10. Extracted delay components as a function of L_g. The delay (τ) is partitioned into three components: transit time (τ_t), parasitic charging delay (τ_{ext}), and parasitic resistance delay (τ_{par}).

the effect of τ_{ext} and τ_{par} become non-negligible. The ratios of $(\tau_{ext} + \tau_{par})/\tau_t$ are 39% and 40% for the InAlN/GaN HEMTs with L_g of 70 and 50 nm, respectively. This means the parasitic capacitance and resistance significantly hampers further L_g scaling benefits in RF performance of sub-100 nm InAlN/GaN HEMTs.

Therefore, downscaling and decreasing parasitic resistances as well as capacitances are very important for further improving device performance of InAlN/GaN HEMTs on Si. Figure 11 plots the calculated f_T and f_{max}

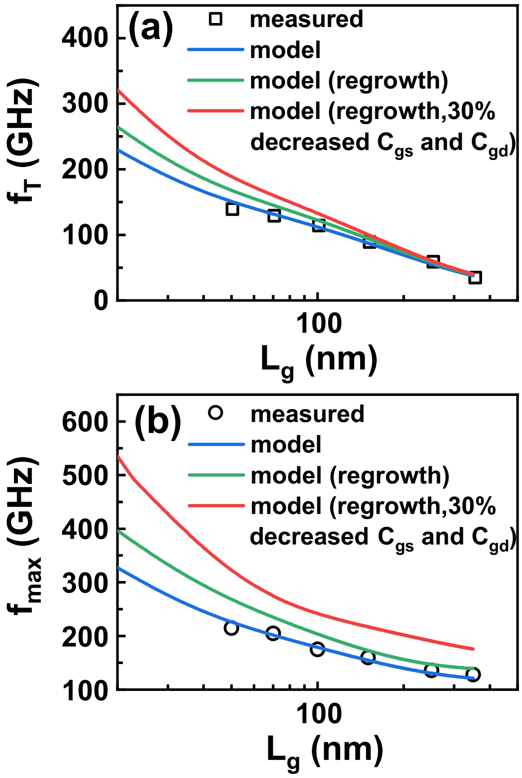

Figure 11. f_T and f_{max} under measured results (Scatters), obtained from model with extracted parameters (Blue-line), model with regrowth ohmic contact(Green-line), and model with regrowth and 30% decreased C_{gs} and C_{gd} (Red-line).

based on the model and the extracted parameters (Blue-line in Fig. 11), which shows a good agreement with the measured results. In terms of the electron velocity saturation, the electron velocity of the InAlN/GaN HEMTs with $L_g < 50$ nm is assumed to be the same as that with $L_g = 50$ nm. With the obtained v_e, τ_t can be obtained using (3), τ_{ext} is parasitic charging delay through $C_{gs,ext}$ and $C_{gd,ext}$, and both are the constant as shown in Fig. 7. τ_{par} is mainly associated with R_s and R_d, which are independent on L_g. As shown in Fig. 10, τ_{ext} and τ_{par} present slight change with L_g. So here τ_{par} of the device with $L_g = 50$ nm is used during the model calculation. Then f_T can be calculated with the obtained τ_t, τ_{ext} and τ_{par} by using (2). When L_g decrases from the 50–20 nm, the T-shaped gate head length of 400 nm is unchanged, so the effect of the small gate length variation on R_g and R_i is miminal. Hence R_g and R_i of device with L_g of 50 nm are used. C_{gd} is extracted from the linear fitting in Fig. 7b and then f_{max} is obtained using (1). The model results present that f_T/f_{max} of 230/327 GHz can be achieved when L_g scales down to 20 nm with the technology developed in the study. To decrease the parasitic resistance, the regrowth ohmic contact can be used. Here R_s (0.30 Ω mm), R_d (0.32 Ω mm), and G_m (573 mS/mm) are changed to 0.10 Ω mm, 0.08 Ω mm, and 620 mS/mm[5]. Then new model results with regrowth technology are plotted (Green-line in Fig. 11) and a f_T/f_{max} of 265/397 GHz is achieved on the device with a 20-nm gate length. Optimizing the detailed structure of T-shaped gate can decrease C_{gs} and C_{gd}. Hence when 30% decreasing of C_{gs} and C_{gd} is added into the model, new results (Red-line in Fig. 11) are plotted and an improved f_T/f_{max} of 320/535 GHz on 20-nm-gate-length InAlN/GaN HEMT is demonstrated. These values are comparable to the 27-nm InAlN/GaN HEMTs on SiC with f_T/f_{max} of 348/340 GHz, suggesting the possibility of further improvement of InAlN/GaN HEMTs on Si.

Conclusions

In summary, high-performance 50-nm InAlN/GaN HEMT on Si with an I_{on}/I_{off} ratio of 7.28×10^6, a SS of 72 mV/dec, a DIBL of 88 mV/V, a BV_{ds} of 36, a f_T/f_{max} of 140/215 GHz, and a JFOM of 5.04 THz V are demonstrated. The extrinsic and intrinsic parameters of transistors with different L_g are extracted and the scaling behavior of InAlN/GaN HEMTs on Si is demonstrated. Based on extracted model, a f_T/f_{max} of 320/535 GHz can be achieved on a 20-nm-gate-length InAlN/GaN HEMT with regrowth ohmic contact technology and 30% decreased parasitic capacitance. This study confirmes the feasibility of further improvement of InAlN/GaN HEMTs on Si for RF applications.

Data availability

The datasets supporting the conclusions of this article are included in the article.

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Author contributions

P.C. and Y.Z. contributed to the research design, experiment measurements, data analysis, and manuscript preparation. All authors reviewed this manuscript.

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Competing interests

The authors declare no competing interests.

Additional information

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