Reconfigurable Boolean Logic Using Magnetic Single-Electron Transistors

M. Fernando Gonzalez-Zalba[1‡]*, **Chiara Ciccarelli**[2‡], **Liviu P. Zarbo**[3], **Andrew C. Irvine**[2], **Richard C. Campion**[4], **Bryan L. Gallagher**[4], **Tomas Jungwirth**[3,4], **Andrew J. Ferguson**[2], **Joerg Wunderlich**[1,3]

1 Hitachi Cambridge Laboratory, Cambridge CB3 0HE, United Kingdom, **2** Cavendsih Laboratory, University of Cambridge, Cambridge, United Kingdom, **3** Institute of Physics, The Academy of Science of the Czech Republic, v.v.i, Cukrovarnick'a 10, 162 53 Praha 6, Czech Republic, **4** School of Physics and Astronomy, University of Nottingham, Nottingham NG7 2RD, United Kingdom

‡ These authors contributed equally to this work.

* mg507@cam.ac.uk

Abstract

We propose a novel hybrid single-electron device for reprogrammable low-power logic operations, the magnetic single-electron transistor (MSET). The device consists of an aluminium single-electron transistor with a GaMnAs magnetic back-gate. Changing between different logic gate functions is realized by reorienting the magnetic moments of the magnetic layer, which induces a voltage shift on the Coulomb blockade oscillations of the MSET. We show that we can arbitrarily reprogram the function of the device from an n-type SET for in-plane magnetization of the GaMnAs layer to p-type SET for out-of-plane magnetization orientation. Moreover, we demonstrate a set of reprogrammable Boolean gates and its logical complement at the single device level. Finally, we propose two sets of reconfigurable binary gates using combinations of two MSETs in a pull-down network.

Introduction

As the downscaling of conventional CMOS technology is bound to reach its fundamental limit new algorithms will be the answer to achieve increasingly higher performance and reduced power consumption. Reconfigurable digital circuits provide a way to extend the functionalities of conventional CMOS by implementing in the same physical space multiple logic operations and therefore increasing the computational complexity. Reconfiguration of the logic functions at each individual device promises even more compact and flexible circuit design [1–5]. However, the implementation of such reconfigurable logic using single-electron transistors (SETs) [6, 7] is appealing because SETs have good scalability, one of the lowest energy-per-switching-event [8] and the possibility to combine their electrical properties with magnetic elements [9–14]. There have been several proposals to implement programmable SET logic by using the charge degree of freedom such as fixed gate voltages [15], non-volatile charge nodes [16, 17] and the spin degree of freedom [18–20].

In this manuscript, we show a proof of principle for reconfigurable Boolean logic based on magnetically-gated circuit elements and we suggest multi-device reconfigurable logic architectures. More particularly, we report the complementary logic operation of a aluminium MSET. The reconfigurable capability of our MSET stems from the magnetization-dependent work function of GaMnAs back gate. When the back-gate is kept at a constant potential the magnetic-field-induced chemical change causes a charge accumulation in the gate electrode which can be readily sensed by the SET as a change in the Coulomb oscillation phase [21, 22]. Although the concept is demonstrated here for MSET devices, the operating principle is general and transferable to any field-effect transistor.

Results

The MSET has two modes of operation: it responds to gate voltage inputs (electric mode) as well as to the orientation of the magnetic moments (magnetic mode). By reorienting the magnetization of the GaMnAs substrate we are able to switch from n-type to p-type MSET. Making use of the magnetic mode we demonstrate two sets of reprogrammable Boolean logic gates implemented at the single device level. Finally, we suggest a strategy to scale the reconfigurable logic operation to the multiple device level.

A schematic cross-section of the proposed aluminium MSET is depicted in Fig 1(a). The key element of this structure is the magnetic gate electrode, an epitaxially grown $Ga_{0.94} Mn_{0.06}$ As layer on GaAs that acts as a back-gate with easy-axis directions [110] and [1–10]. A magnetic field $B = 0.7$ T, larger that the saturation field $B_s \approx 0.3$ T, is applied to rotate the magnetization M with respect to the [001] direction ($\phi = 0°$). The angle θ with respect to the [1–10] direction is kept equal to 90° in all measurements. The results presented here are independent

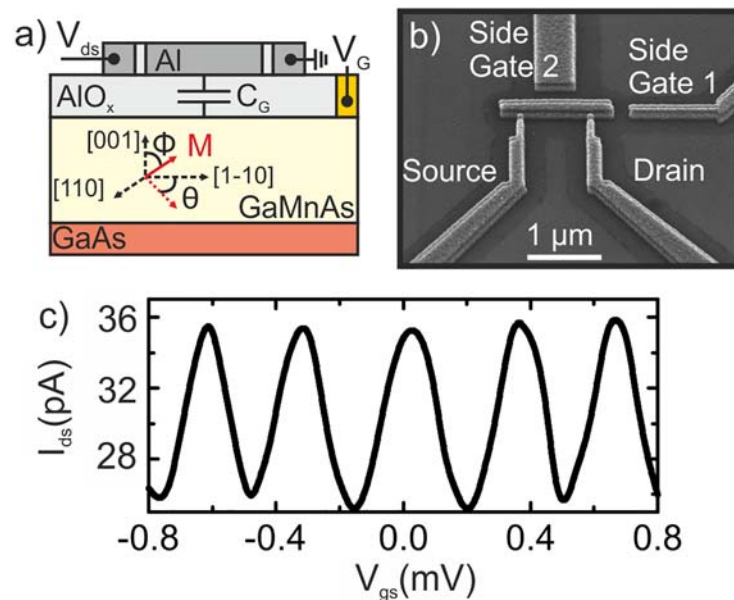Fig 1. **Device structure.** (a) Schematic cross-section of the device sketching the magnetization orientation of the (Ga,Mn)As back-gate layer. (b) SEM image of the device. The aluminium island is separated from the source and drain leads by AlO_x tunnel junctions. Side gates were not used in this experiment. (c) Drain current (I_{ds}) oscillations as a function of the back gate voltage (V_{gs}).

of the magnitude of B for $B > B_s$. A 100 nm alumina layer is used as gate dielectric on top of which the Al-SET is fabricated. The source and drain leads are separated from the micron-sized island by aluminium oxide tunnel junctions, as it can be observed in the SEM image in Fig 1(b). In this letter the side gates were not used but could provide extra-functionality to the structure.

In the electric mode of operation we use the back-gate voltage to control the induced-charge in the island of the MSET. Fig 1(c) shows the drain current (I_{ds}) versus back-gate voltage (V_{gs}) at 300 mK. The plot shows a periodic oscillatory behaviour of the current, namely the Coulomb blockade oscillations. Several devices were studied with typical charging energies $E_C = 100$–300 μeV and gate capacitances $C_G = 0.4$–1.0 fF. We obtain a I_{ON}/I_{OFF} contrast ratio of up to 1.33 and typical tunnel junction resistances of $R_T = 500$ kΩ.

The magnetic mode of operation is based on the dependence of the GaMnAs band structure on the orientation of the magnetization due to spin orbit coupling. The magnetization reorientation yields a shift in the GaMnAs work function $\Delta\mu$ which in itself does not produce a response on the MSET. However, when the back gate is held at constant potential a change in μ causes an inward or outward flow of charge in the gate which in turn offsets the Coulomb oscillations. If the work function shift in the magnetic layer is adequate, the phase shift becomes half a period of the Coulomb blockade oscillations and complementary MSETs are obtained. The equation that defines the necessary work function shift for maximum on-off current ratio can be expressed as,

$$\Delta\mu(B)_{max} = \frac{e^2}{2C_G} \qquad (1)$$

As well, the minimum potential shift for complementary operation at temperature T can be defined as a gate voltage shift equal to the FWHM of the Coulomb peak [23],

$$\Delta\mu(B)_{min} = \frac{4.35 k_B T C_\Sigma}{C_G} \qquad (2)$$

These two equations set the operational parameters in terms of temperature, magnetic field and physical dimensions of the structure.

The complementary operation of the MSET is experimentally demonstrated in Fig 2 for a device with $E_C = 300 \mu$eV and $C_G = 1.0$ fF. To switch between complimentary modes we rotate continuously a saturating magnetic field from $\phi = 90°$, where the magnetization resides M parallel to the plane along the easy-axis [110] (Fig 2(a)) to $\phi = 0°$ where the magnetization is out-of-plane (Fig 2(b)). This can be seen in Fig 2(c) where we plot the source-drain current I_{ds} as a function of the magnetization angle ϕ and gate voltage V_{gs} for $V_{ds} = 15\mu$V and B = 0.7 T. When the magnetization is in-plane, we select $V_{gs} = -61 \mu$V as the logic 0 and $V_{gs} = +86 \mu$V as the logic 1 for the n-type SET (see Fig 2(d)). As the magnetic field is rotated to $\phi = 0°$, the magnetization is re-oriented in the [001] direction and the GaMnAs work function increases producing a gate voltage shift of $\Delta V_{gs} = 150 \mu$V [24]. The combination of work function potential shift in the Ga$_{0.94}$Mn$_{0.06}$As layer with the 300 μV gate voltage period of the device result in that the magnetically-induced gate voltage shift coincides with half a Coulomb oscillation (fulfilling Eq (1)). The MSET behaves effectively as a p-type SET, Fig 2(e). Therefore we can arbitrarily select the function of the SET from an n-SET for in-plane magnetization $\phi = 90°$ to a p-type for out-of-plane magnetization $\phi = 0°$.

We now focus on the logic design that could be implemented at the single device level. It has been shown that any Boolean function of two variables can be implemented on a SET [25]. In this letter, by making use of the magnetic mode of operation, we demonstrate two sets of
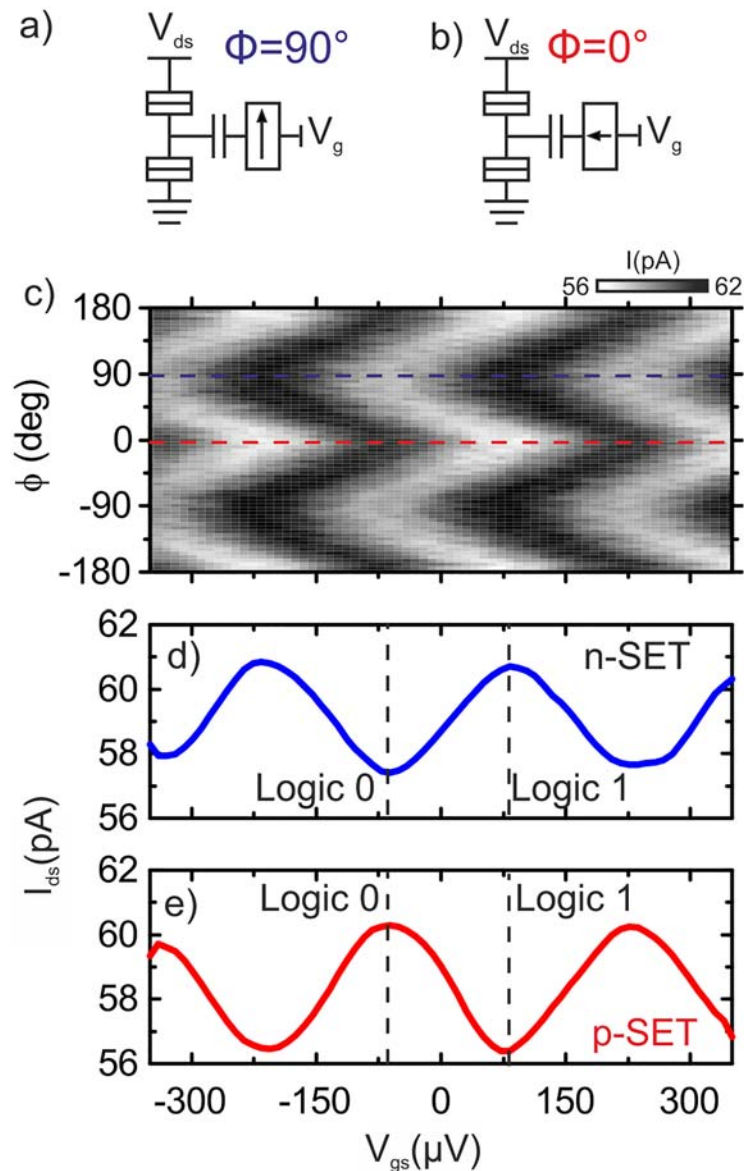
Fig 2. Complementary operation. Schematic diagram of the MSET for different magnetization orientations. (a) $\phi = 0°$ the magnetization is in-plane and (b) $\phi = 90°$ the magnetization is out-of-plane. (c) Coulomb blockade oscillations as a function of the direction of the back-gate voltage V_{gs} and the applied magnetic field orientation ϕ for B = 0.7 T. The-dashed blue and red lines indicate the operating points. (d) MSET Ids-Vgs transfer function at $\phi = 0°$. The logic 0 (1) has been selected at a low (high) current level, n-type SET. (e) MSET Ids-Vgs transfer function at $\phi = 90°$. The logic outputs have been inverted, p-type SET.

reprogrammable logic gates. The inputs in this case are the drain voltage (input A) and the gate voltage (input B) and the output is the drain current. In Fig 3(a) we plot the $V_{ds} - V_{gs}$ diagram of the MSET showing the characteristic Coulomb diamonds at $\phi = 0°$. Overimposed, we schematically show two logic gates framed in red AND and NAND. The output is drawn as en empty dot if the results is 0 (low current level) and a full dot if the results is 1 (high current level). Upon changing the magnetization angle to $\phi = 90°$, the whole diagram is shifted horizontally by $\Delta V_{gs} = -150 \, \mu V$ and, therefore, at the same input voltages the gate output changes
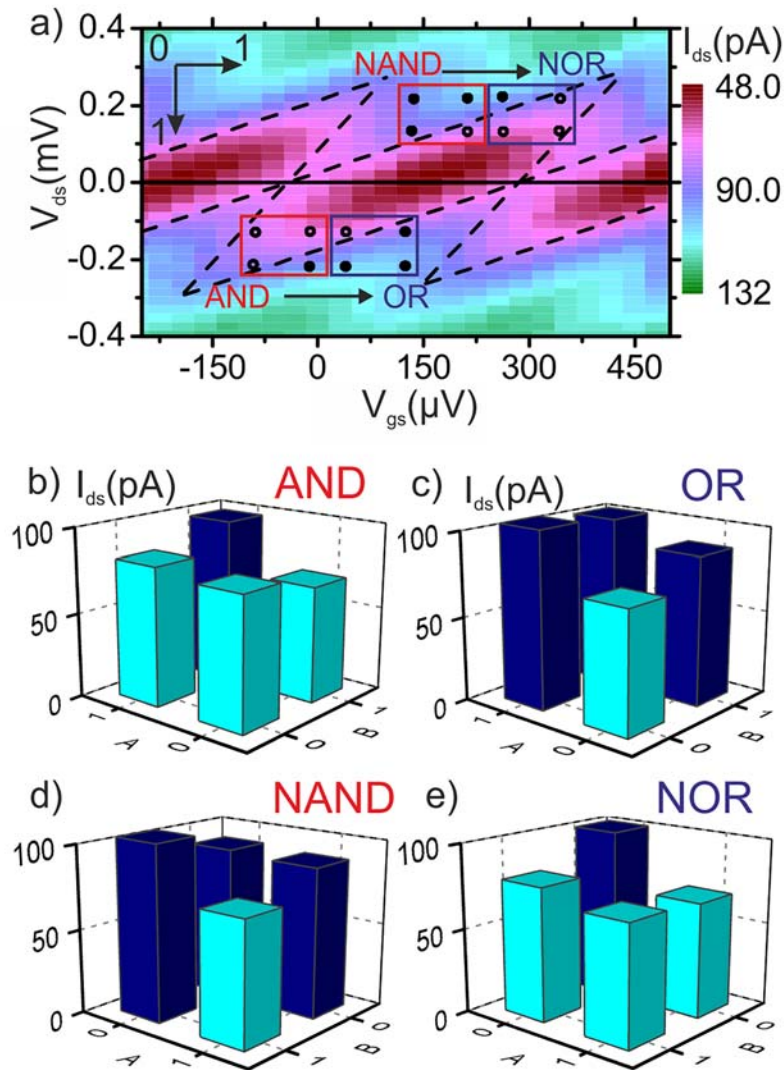
Fig 3. **Single-device logic.** (a) $V_{ds} - V_{gs}$ map of the drain current for $\phi = 0°$ showing the characteristic Coulomb diamonds. Red and blue frames sketch the implemented logic gates for $\phi = 0°$ and $90°$ respectively. (b-c) AND-OR set of reprogrammable logic gates. AND gate implemented at $\phi = 0°$ (b) and OR gate at $\phi = 90°$ (c) with V_{ds} (input A) 0(1) defined as $-132(-220)$ μV and V_{gs} (input B) 0(1) defined as $-96(0)$ μV. (d-e) NAND-NOR set of reprogrammable logic gates. NAND gate implemented at $\phi = 0°$ (d) and NOR gate at $\phi = 90°$ (e) with V_{sd} (input A) 0(1) defined as 220(132) μV and V_{gs} (input B) 0(1) defined as 128(224) μV.

doi:10.1371/journal.pone.0125142.g003

to the two blue-framed logic gates, from (N)AND to (N)OR as depicted by the arrow. The reconfigurable logic gates are demonstrated in the histograms in Fig 3(b)–3(e). In order to discriminate between logic outputs 0 and 1 we select the low(high) current threshold at $I_{ds} = 80$ (90) pA. In Fig 3(b) we represent a histogram of the current output for an AND gate implemented on the edge of the Coulomb diamond. By rotating the magnetization to the in-plane direction ($\phi = 90°$) the Coulomb diamonds shift and the logic gate switches function to OR (Fig 3 (c)). Moreover, in Fig 3(d) and 3(e) we demonstrate the logical complement set of reprogrammable Boolean gates. The set switches between NAND ($\phi = 0°$) and NOR ($\phi = 90°$) logic gates.

Finally, we briefly comment on the possibilities for multi-device reconfigurable logic design. As an example, we focus on pull-down networks formed by two elements with a common
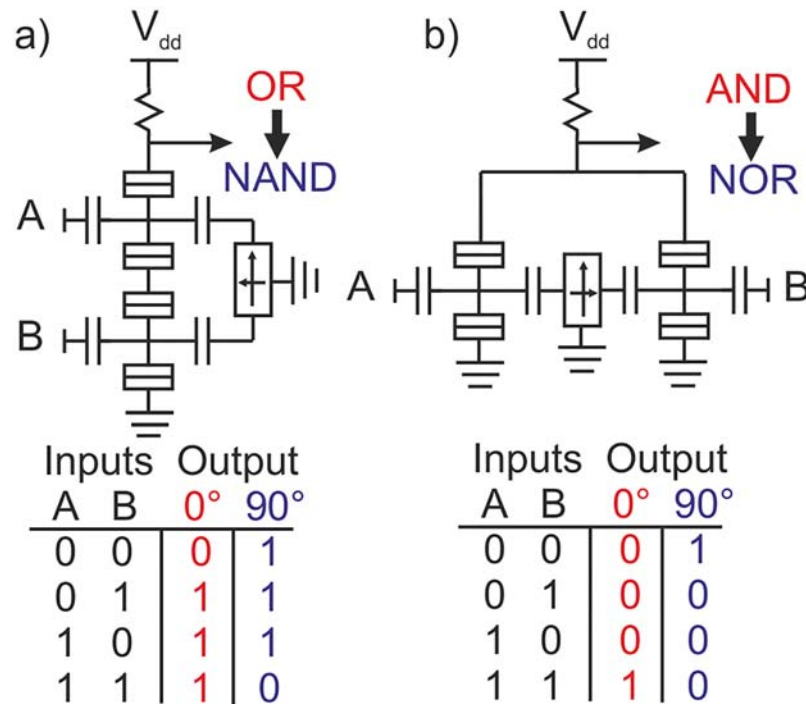
Fig 4. Logic at the multiple device level considering identical SETs and the logic inputs defined in Fig 2. The inputs A and B are defined as taken as the SET gate values. (a) A series pull-down network performs the OR operation at $\phi = 0°$ and NAND at $\phi = 90°$. (b) Parallel pull-down network performs the AND operation at $\phi = 0°$ and NOR at $\phi = 90°$.

doi:10.1371/journal.pone.0125142.g004

magnetic back-gate and independently addressable electrical gates. We concentrate on the case of MSET with identical I_{ds}-V_{gs} transfer functions and logic inputs defined by Fig 2(c) and 2(d). The circuit in Fig 4(a) consists of a resistor load and two MSETs in series. In the state $\phi = 0°$ both MSET are in the p-type state and the network realizes the operation OR. However this gate can be reconfigured by rotating the magnetization, $\phi = 90°$. In this situation both MSET are in the n-type state and the logic operation becomes NAND. Similarly, for a pull-down network consisting of two MSETs in parallel, Fig 4(b) the logic gate can be programmed to switch between AND ($\phi = 0°$) and NOR ($\phi = 90°$) operations.

Discussion

In conclusion, we have demonstrated the complementary logic operation of an aluminium MSET by making use of magnetization-dependent work function of the GaMnAs magnetic back-gate. By using the source-drain voltage and the gate voltage as binary inputs we showed a set of Boolean gates and its logical complement implemented at the single device level, AND-OR and NAND-NOR gates. Finally, we have described a route to integrate multiple MSET in to integrated reconfigurable logic circuits. Although here we present results on MSETs, magnetic gating could be exploited to switch function in more conventional circuit elements such as CMOS field-effect transistors or novel electronic devices such as graphene ambipolar transistors [26] or spin-hot carrier transistors [27]. For reliable room temperature switching, magnetic materials with work function shifts of the order of 60 mV will be required [28]. Materials with large work function anisotropy such as CoPt alloys could provide that

functionality [21]. Moreover, non-volatile logic reconfiguration could be also achieved by making use of the stability of the magnetic moments along non collinear "magnetic easy axes" orientations without applying external magnetic fields or electrical currents.

Acknowledgments

Author Contributions

Conceived and designed the experiments: MFGZ CC TJ AF JW. Performed the experiments: CC. Analyzed the data: MFGZ. Contributed reagents/materials/analysis tools: LZ AI RC BG. Wrote the paper: MFGZ CC JW.

References

1. Strukov DB, Snider GS, Stewart DR, Williams RS. The missing memristor found. Nature. 2008; 453: 80–83. doi: 10.1038/nature06932 PMID: 18451858

2. Joo S, Kim T, Shin SH, Lim JY, Hong J, Song JD, et al. Magnetic-field-controlled reconfigurable semiconductor logic. Nature. 2013; 494: 72–76. doi: 10.1038/nature11817 PMID: 23364687

3. Heinzig A, Slesazeck S, Kreupl F, Mikolajick T, Weber WM. Reconfigurable silicon nanowire transistors. Nano Letters. 2012; 12: 119–124. doi: 10.1021/nl203094h PMID: 22111808

4. Yu WJ, Kim UJ, Kang BR, Lee IH, Lee EH, Hee Y, et al. Adaptive logic circuits with doping-free ambipolar carbon nanotube transistors. Nano Letters. 2009; 9: 1401–1405. doi: 10.1021/nl803066v PMID: 19281215

5. Mol JA, Verduijn J, Levine RD, Remacle F, Rogge S. Integrated logic circuits using single-atom transistors PNAS 2011; 108: 13969–13972.

6. Kastner MA. The single-electron transistor. Rev Mod Phys. 1992; 64: 849–858. doi: 10.1103/RevModPhys.64.849

7. Gonzalez-Zalba MF, Heiss D, Podd G, Ferguon AJ. App Phys Lett. 2012; 101: 103504. doi: 10.1063/1.4750251

8. Zhu C, Gu Z, Shang L, Dick RP, Knobel RG. Towards an ultra-low-power architecture using single-electron tunneling transistors. Proceedings of the 44th annual Design Automation Conference. 2007; 312.

9. Ono K, Shimada H, Ootuka Y. Enhanced magnetic valve effect and magneto-Coulomb oscillations in ferromagnetic single electron transistors. J Phys Soc Japan. 1997; 66: 1261. doi: 10.1143/JPSJ.66.1261

10. Barnas J, Martinek J, Michalek G, Bulka B R, Fert A. Spin effects in ferromagnetic single-electron transistors. Phys Rev B. 2000; 62: 12363. doi: 10.1103/PhysRevB.62.12363

11. Shirakashi J, Takemura Y. Ferromagnetic single-electron transistor with multiple tunnel junctions. J Mag Soc Japan. 2001; 25: 783. doi: 10.3379/jmsjmag.25.783

12. Jalil MBA, Tan SG, Ma MJ. Enhanced magneto-Coulomb effect in asymmetric ferromagnetic single electron transistors. J App Phys. 2009; 105: 07C905 doi: 10.1063/1.3055271

13. Takiguchi M, Shimada H, Mizugaki Y. Correlation between polarity of magnetoresistance ratio and tunnel resistance in ferromagnetic single-electron transistor with superconductive island. J J App Phys. 2014; 53: 043101 doi: 10.7567/JJAP.53.043101

14. Kirchner S, Si Q. Quantum criticality out of equilibrium: Steady state in a magnetic single-electron transistor. Phys Rev Lett. 2009; 103: 206401 doi: 10.1103/PhysRevLett.103.206401 PMID: 20365995

15. Tucker JR. Complementary digital logic based on Coulomb blockade. J App Phys. 1992; 72: 4399–4413. doi: 10.1063/1.352206

16. Ishikuro H, Hiramoto T. Influence of quantum confinement effects on single electron and single hole transistors. In: Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International. 1998; 119–122.

17. Uchida K, Koga J, Ohba R, Toriumi A. Programmable single-electron transistor logic for low-power intelligent Si LSI. In: Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International. 2002;1: 206–460.

18. Wunderlich J, Jungwirth T, Irvine AC, Kaestner B, Shick AB, Campion RP, et al. Coulomb blockade an-isotropic magnetoresistance and voltage controlled magnetic switching in a ferromagnetic GaMnAs sin-gle electron transistor. J Magn Magn Mater. 2007; 310: 1883–1888. doi: 10.1016/j.jmmm.2006.10.676

19. Dery H, Dalal P, Cywinski L, Sham LJ. Spin-based logic in semiconductors for reconfigurable large-scale circuits. Nature. 2007; 447: 573–576. doi: 10.1038/nature05833 PMID: 17538616

20. Hai PN, Sugahara S, Tanaka M. Reconfigurable logic gates using single-electron spin transistors. Japn J Appl Phys. 2007; 46: 6579–6585. doi: 10.1143/JJAP.46.6579

21. Wunderlich J, Jungwirth T, Kaestner B, Irvine AC, Shick AB, Stone N, et al. Coulomb blockade aniso-tropic magnetoresistance effect in a (Ga,Mn)As single-electron transistor. Phys Rev Lett. 2006; 97: 077201. doi: 10.1103/PhysRevLett.97.077201 PMID: 17026268

22. Ciccarelli C, Zarbo LP, Irvine AC, Campion RP, Gallagher BL, Wunderlich J, et al. Spin gating electrical current. App Phys Lett. 2012; 101: 122411–122414. doi: 10.1063/1.4752013

23. Beenakker CWJ. Theory of coulomb-blockade oscillations in the conductance of a quantum dot. Phys Rev B. 1991; 44: 1646–1656. doi: 10.1103/PhysRevB.44.1646

24. In-plane rotations between [110] and [1−10] directions were explored leading to $\Delta\mu = 46$ μeV insufficient for complementary operation.

25. Klein M, Lansbergen GP, Mol JA, Rogge S, Levine RD, Remacle F. Reconfigurable logic devices on a single dopant atom-operation up to a full adder by using electrical spectroscopy. ChemPhysChem 2009; 10: 162–173. doi: 10.1002/cphc.200800568 PMID: 19115322

26. Wang H, Hsu A, Wu J, Kong J, Palacios T. (2010) Graphene-based ambipolar RF mixers. IEEE Elec Dev Lett. 2010; 31: 906 doi: 10.1109/LED.2010.2052017

27. Mizuno Y, Ohya S, Hai PN, Tanaka M. Spin-dependent transport properties in GaMnAs-based spin hot-carrier transistors. Appl Phys Lett. 2007; 90: 62505/1–3 doi: 10.1063/1.2724771

28. Betz AC, Barraud S, Wilmart Q, Placais B, Jehl X, Sanquer M, et al. High frequency characterisation of thermionic charge transport in silicon-on-insulator nanowire transistors. App Phys Lett 2014; 104: 043106. doi: 10.1063/1.4863538