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Performance of thermo-optic components based on dielectric-loaded surface plasmon polariton waveguides

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Theoretical analysis of thermo-optic (TO) modulation with dielectric-loaded surface plasmon polariton waveguide (DLSPPW) components at telecom wavelength of 1.55 μm is presented with simulations performed using the finite-element method (FEM). The investigated DLSPPW configuration consists of a 1 μm-thick and 1 μm-wide polymer ridge placed on a 50 nm-thin gold stripe and supported by a buffer layer material covering a Si wafer. Our analysis covers a broad range of parameters, including the buffer layer thickness, its thermal conductivity, and the metal stripe width, and takes into account the effect of isolation trenches structured along the heated part of waveguide. The results of our simulations agree well with the reported experimental data and provide valuable information for further development of TO plasmonic components with low switching powers, fast responses and small footprints.

The massive growth of telecom and data communication traffic in the last decade can be attributed to using optical fibers as the transmission medium which has already taken over the task of long-distance communications from electrical cables and which refines the connections between different parts of large electronic systems. However, in short-distance communications inside information-processing devices on integrated circuit chips and on circuit boards wires still dominate. It means that the optical signals have to be converted to electrical ones, to be amplified, regenerated, or switched, and then they are reconverted to optical signals. It is well known that optical-to-electronic-to-optical (OEO) conversion is a significant impediment in transmission. Furthermore, a limited capacity of electrical interconnects is a problem for systems even at short on-chip distances and between chips. The replacement of existing electronic network switches with optical ones is thus strongly desired in order to alleviate the need for OEO conversions. Therefore, optical switches can play an important role in applications, including optical inter and cross connection, protection switching and array switching for optical add-drop multiplexing[1].

Among many available switching technologies, TO switches[2] are very attractive due their small size, large scalability, and potentiality for integration with waveguide dense-wavelength division-multiplexing multiplexers. Their optical performances, in terms of cross talk and insertion losses, are acceptable for many applications. In addition, the speed of waveguide devices based on the TO effect is adequate for all routing applications. When designing TO switches, one would naturally aim for low switching power, fast switching time, and high extinction ratio[3,4]. Additionally, the footprint should be as small as possible to meet a requirements for compact waveguide components and easy in fabrication. But in reality, considering a TO switch, a trade-off between the temperature switching time and power dissipation per unit length must be taken into account. In the case of photonic waveguides, if a TO switch is realized using a material with a high thermal conductivity, a short switching time and a high switching power per unit length are obtained. On the contrary, using a material with a small thermal conductivity, a long switching time and a low switching power per unit length is achieved. The reason for it is that metallic stripes, acting as heaters, are deposited on top of or laterally displaced with respect to the waveguides, close to the switching region. It induces, however, high polarization-dependent losses, which affect mostly the TM-polarized modes. To avoid this inconvenience, one should either move away the heating electrodes from the waveguiding region or introduce a thin dielectric layer between the metallic heater and the waveguide, both of which, however, influence thermal properties of a device resulting in deterioration of its characteristics.

The aforementioned problem can be circumvented by using plasmonic waveguides, i.e., waveguides supporting surface plasmon polariton (SPP) modes propagating along metal-dielectric interfaces. Among various SPP-based waveguide configurations, dielectric-loaded SPP waveguides (DLSPPWs)[5,6] represent an attractive alternative by virtue of being naturally compatible with different dielectric and industrial fabrication using large-scale UV

lithography. DLSPPWs satisfy the important requirements of strong mode confinement, relatively low propagation losses, and straightforward integration with control electrodes enabling TO control. The main advantage of this plasmonic technology is that metal stripes can be used both as supports of DLSPPWs and electrodes, allowing thereby efficient heating of DLSPPW ridges and TO control of the DLSPPW mode index, since the mode field reaches its maximum at the metal-dielectric interface[6–8]. At the same time, the main problem in the DLSPPW technology is related to high propagation losses due to the radiation absorption in metal stripes. This impact can be minimized by integration of short DLSPPWs with long dielectric waveguides[9]. In this way, small sizes and low-power switching capabilities of DLSPPW components can be combined with low propagation losses of dielectric waveguides and processing capacity of electronics, resulting in miniaturized and power efficient photonic interconnect routers[10–13]. Additionally, the inevitable propagation losses in DLSPPWs can be turned into a useful functionality by implementing the DLSPPW mode power monitoring realized via measuring variations in the resistance of metal stripes supporting DLSPPW ridges caused by heating due to the mode absorption[14,15].

Here, we conduct a theoretical analysis of TO modulation with DLSPPW components operating at telecom wavelengths by using the finite-element method (FEM), and evaluate the main modulation characteristics for a broad range of system parameters, including the buffer layer thickness, its thermal conductivity, and the metal stripe width. The effect of isolation trenches structured along the heated part of waveguide is also considered. The results of our simulations are compared with the reported experimental data and provide valuable information for further development of TO DLSPPW components with low switching powers, fast responses and small footprints.

Results

Performance characteristics. The TO effect accounts for changes in the refractive index of a dielectric material due to its temperature variation. It is described by the thermo-optic coefficient (TOC) dn/dT, where n is the refractive index of the material at temperature T. By using micro-heaters, temperature gradients can be induced within waveguide structures leading to changes in the refractive index profile, which, in turn, influences the mode effective index and thereby the phase accumulated during the mode propagation. Thus introduced phase modulation can be used to modulate the output mode power and/or switch the mode power between different outputs. In TO components, the heat is generated by transmitting an electrical current through electrodes that are heated by the Joule effect.

The performance of a modulator can be described by several characteristics, such as switching time, extinction ratio (modulation depth), power consumption, insertion loss, and a footprint. The switching time (modulation speed or bandwidth) is one of the most important characteristics of an optical switch. Modulation bandwidth, also known as a 3 dB cutoff frequency for components without cutoff at low frequencies, is defined by the frequency at which the modulated power decreases by half, i.e., by 3 dB. The speed of a modulator is commonly characterized by its ability to perform optical (phase or amplitude) modulation at a certain rate, which is determined by its switching time (and related to its bandwidth). The switching time is proportional to the thermal time constant of the heating or cooling process which is a product of the thermal capacitance and the thermal resistance of the system under measurement

$$\tau = R_{\text{th}} \cdot C_{\text{th}} \tag{1}$$

Here, the thermal resistance of an object, $R_{\text{th}} = L/(\kappa \cdot A)$, describes the temperature difference that will cause the heat power of 1 Watt to flow between the object and its surroundings, and the thermal capacitance of an object, $C_{\text{th}} = c_p \cdot \rho \cdot V$, is the energy required to change its temperature by 1 K, if no heat is exchanged with its surroundings. In our case, L is the thickness of a substrate along the heat transfer direction, A is the cross-section area of the substrate, κ is the thermal conductivity of the material, c_{p} is the specific heat, ρ is the mass density, and V is the heated volume of the material.

The modulation depth characterizes a difference between the maximum and minimum of the modulated mode intensity (power), and, for Mach-Zehnder interferometer (MZI), is expressed by

$$M = \frac{(I_{\max} - I_{\min})}{(I_{\max} + I_{\min})} = 2k/(1+k), \tag{2}$$

where $k = I_1/I_2$ is the ratio between mode powers in two arms of the MZI. In comparison, the extinction ratio is defined as the ratio between $I_{\max}$, the mode (power) intensity at the output when the MZI is tuned to the maximum transmission, and $I_{\min}$, the output intensity when the MZI is adjusted for the minimum transmission

$$ER = 10 \cdot \log\left(\frac{I_{\max}}{I_{\min}}\right) \tag{3}$$

A large extinction ratio, or modulation depth, is needed in order to ensure low bit error rates during the signal detection, in particular, when insertion (coupling and propagation) losses are large.

The power consumption is defined as the power required to switch between the maximum and minimum transmission, and it becomes especially important for densely packed optical components and interconnects. It can also be related to the energy spent (dissipated) when producing each data bit. Insertion loss takes into account the optical power that is lost when modulator is added to a photonic circuit. It is a passive loss that comprises reflection, absorption and mode-coupling losses, and is important because it contributes to the link loss budget and to the overall end-to-end losses in the system. Another important parameter of a device is its footprint, which should be as small as possible to meet requirements for compact waveguide components. In the traditional photonic MZI-based switches, the interaction length for complete switching between the maximum and minimum transmission is usually very long (on the mm-scale), which hinders high-speed performance and results in greater insertion loss, cost and power consumption.

Mach-Zehnder Interferometer. MZI is probably the most extensively studied TO switch because of its simplicity in design and fabrication as well as because of presence of the reference arm, which is useful for compensation of the common-mode effect. There are four main characteristics that allow one to evaluate the MZI performance: switching time, power switching, modulation depth (visibility) and/or extinction ratio. High-performance MZI should feature high-frequency operation (fast switching time), low power swiching, large modulation depth and extinction ratio.

TO MZI operation is based on changing the mode propagation constant in a heated arm resulting in the phase difference of two modes that interfere in the output Y-junction. The length of the heated MZI arm required to ensure complete modulation, i.e., extinguish the mode power at the Y-junction output (in the case of symmetric MZI), is related to the introduction of the phase difference π between the arms

$$\Delta\phi = \pi = \frac{2\pi}{\lambda} \Delta n \bullet L \tag{4}$$

For exactly equal MZI arm lengths, introducing the phase difference π can be realized by heating one of them because the refractive index is temperature dependent:

$$\Delta\phi = \pi = \frac{2\pi}{\lambda} \frac{\partial n}{\partial T} \bullet \Delta T \bullet L \Rightarrow L = \frac{\lambda}{2 \bullet \Delta T} \left(\frac{\partial n}{\partial T}\right)^{-1} \tag{5}$$

Configuration and simulation results. The configuration considered in the simulations consists of a 1 μm-thick and 1 μm-wide

Table 1 | Common materials utilized for the manufacture of TO switches

Material	Refractive index	TOC (1/K)	Thermal conductivity coeff. (W/mK)	Heat capacity (J/gK)	Density (g/cm^3)
PMMA	1.493	$-1.05\cdot10^{-4}$	0.2	1.466	1.2
BCB	1.535	$-2.5\cdot10^{-5}$	0.29	2.18	1.05
SiO_2	1.45	$0.62\cdot10^{-5}$	1.4	1.4	2.19
Si	3.48	$1.86\cdot10^{-4}$	148	0.713	2.32
MgF_2	1.37	$0.09\cdot10^{-5}$	11.6	0.955	3.17
Cytop	1.34	-	0.12	0.861	2.03
Au	0.55 + i·11.5	-	318	0.13	19.32
Cyclomer	1.53	$-2.95\cdot10^{-4}$	-	$5.406\cdot10^{-3}$	-
Air	1	-	0.026	1.005	0.00119

polymer ridge deposited on the 50 nm-thick and 2.0–4.0 μm-wide gold electrodes forming a DLSPPW with the invariable length of 41 μm. The overall resistance of the gold electrode was evaluated at ~5 Ω for 4 μm-wide gold electrodes, and ~10 Ω for 2 μm-wide gold electrodes. The substrate considered is a standard Si wafer covered with materials characterized by different thermal conductivity coefficients (table 1) and with variable thicknesses. Heating of the polymer ridge was realized by applying a square voltage to the electrode pads due to the Ohmic heating of the electrode and heat transfer to the materials in contact with the electrodes[11,13,16,17].

Influence of the buffer layer thermal conductivity coefficient and thickness on the switching performance. The switching characteristics for the considered DLSPPW configuration, such as power consumption and a switching time, have been analysed for different buffer layer thicknesses (t = 0.5 and 1.7 μm) and materials (Cytop, SiO_2 and MgF_2), while keeping at the same time ridge dimensions constant at w = h = 1 μm and the same gold stripe, w = 4 μm and h = 50 nm, (Fig. 1). For such DLSPP waveguide configuration, the real part of the mode effective index and the propagation loss obtained from the imaginary part of the modal effective index were calculated using the two-dimensional electromagnetic finite element method (FEM) (Fig. 1(d)).

The presented configuration can be considered as a parallel connection of thermal resistors and consecutive connection of thermal capacitors. The buffer layer materials with lower thermal conductivity coefficients are characterized by higher thermal resistances, so that lower electrical powers are required to increase a buffer layer temperature, and in consequence, to increase a ridge temperature. On the other hand, a lower thermal conductivity coefficient of a buffer layer results in a larger time constant, which is defined as the time required for the temperature to change by ~63% from its starting value to its final value in a transient situation.

For the same buffer layer thickness to rises a ridge temperature of about 70 K, only 2 mW of a dissipated power is needed for structures with Cytop buffer and more than 11 mW with SiO_2 buffer as a results of higher thermal conductivity of SiO_2 (table 1). The power requirement arises even more for high thermal conductivity MgF_2 buffer where it exceeds of 81 mW (Fig. 2).

At the same time, materials with a higher thermal conductivity ensure faster heat dissipation time. To dissipate a heat from the ridge only 0.55 μs is needed for structure with MgF_2 buffer layer and around 2.2 μs and 7.9 μs for structures with SiO_2 and Cytop, respectively. Based on this it can be concluded there is always tradeoff between power requirements and a response time. One way to reduce a response time is through decreasing a buffer layer thickness. For structure with Cytop buffer layer and for a ridge temperature rise of 70 K, decreasing a Cytop thickness from 1.7 μm to 0.5 μm reduces a response time from 7.9 μs to 3.5 μs at the cost of a power consumption which increases from 2 mW to 3.3 mW. For SiO_2 buffer layer the response time reduces from 2.2 μs to 0.46 μs, and at the same time, power consumption increases from 11 mW to 28 mW for SiO_2 thickness of 1.7 μm and 0.5 μm, respectively.

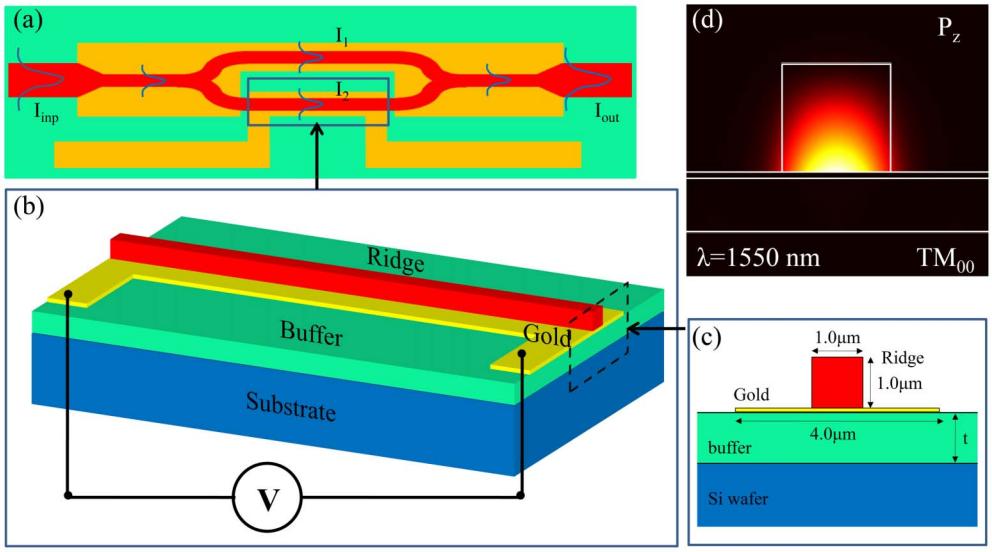

Figure 1 | MZI configuration. (a) Schematic of a DLSPPW-based MZI with (b) considered a heated part of the MZI arm waveguide, where the bias voltage is applied to the gold electrodes. (c) Cross-section of the DLSPPW structure with a PMMA ridge (w = h = 1.0 μm) on top of a gold stripe (w = 4.0 μm, h = 50 nm) deposited on an underlying buffer layer. (d) Field distribution plot of the power flow for structure presented in (c) with the PMMA ridge and Cytop buffer layer below the gold stripe. The fundamental TM_{00} mode is depicted for λ = 1550 nm wavelength where n_{eff} = 1.389 and propagation length L_p = 51 μm.

The performance of each switching element can be compared in terms of power consumption, switching time and footprint. As the waveguide dimensions were kept invariable under all simulations the performance metrics of the switch can be limited to a power consumption and switching time. Considering the heated part of the waveguide being 41 μm-long and high TO polymer as Cyclomer (table 1)[16] to ensure a π-phase shift between MZI arms the ridge temperature increases of 62 K is needed. The power-time metric for a 1.7 μm-thick buffer layer shows ~30.3 mW·μs for structure with Cytop and up to ~48.1 mW·μs and ~85.8 mW·μs for structures with SiO_2 and MgF_2, respectively. Based on this, it can be concluded that for a thick buffer layer the best performances can be achieved with low thermal conductivity buffers. Additionally, a very good fit was achieved with the experimental data where power-time product of ~49.7 mW·μs was achieved for 1.8 μm-thick SiO_2 buffer layer[18,19]. By reducing a buffer layer thickness to 0.5 μm, the power-time metric changes significantly with a change more pronounced for high thermal conductivity materials where ~24.55 mW·μs was evaluated for SiO_2 and ~22.5 mW·μs for structure with Cytop.

Influence of the gold electrode width on the power consumption. One way to reduce the power consumption is to increases the contact area between a metal electrode and ridge. It can be achieved by decreasing the metal electrode width (Fig. 3) and enhancing in this way the efficiency of heat dissipation in the ridge. The results for two different buffer layer materials (Cytop and SiO_2) and two metal widths (w = 2.0 μm and w = 4.0 μm) show significant reduction of a power consumption when metal width decreases from 4.0 μm to 2.0 μm. The contact area between a metal electrode and ridge increases from 25% to 50% and observed power consumption reduces by 21% for structure with the Cytop buffer layer and by 36% for structure with the SiO_2 buffer layer. The power reduction is more significant for materials with high thermal conductivity coefficient.

However, in the case of DLSPPWs there is a cutoff width of the gold stripe below which the propagation length dramatically drops down as narrow gold stripes cause a strong leaking of the guided mode into the substrate (Fig. 3(e) and (f))[20]. It was shown that certain metal width supporting a DLSPP mode is necessary to recover a propagation length similar to that of an infinite thin gold film.

Influence of the trenches on the switching performances of the switch. Another way to reduce the power consumption is by using insulating air trenches on both sides of the metal electrodes, along the heated part of the waveguide (Fig. 4). Those trenches can efficiently suppress lateral thermal diffusion and allows heat flow in only one direction, since the thermal conductivity of air is about 1/58 that of SiO_2. In this way the thermal resistance and thermal capacity of the buffer material reduces which results in small heated volume and it influences on the overall thermal resistance and thermal capacity of the structure. As illustrated by simulation (Fig. 4), a 15% reduction in the power consumption can be achieved for structure with a Cytop buffer layer only by using trenches. This effect is even more pronounced for buffer materials with a higher thermal conductivity coefficient where reduction in power consumption of 39% and 48% was observed for SiO_2 and MgF_2 buffer materials, respectively. At the same time a slight increases of a response time is observed. As previously shown, the main heat dissipation process takes place through the buffer material so incorporation trenches decreases the dissipation area what influences on a slightly longer response time.

Comparison with measurements. To support our calculations, the obtained results were compared with previously fabricated and characterized structures[16,18,19]. In first case (Fig. 5)[16], the modulated MZI arm consist of the Cyclomer ridge (w = 1 μm, h = 0.6 μm) on

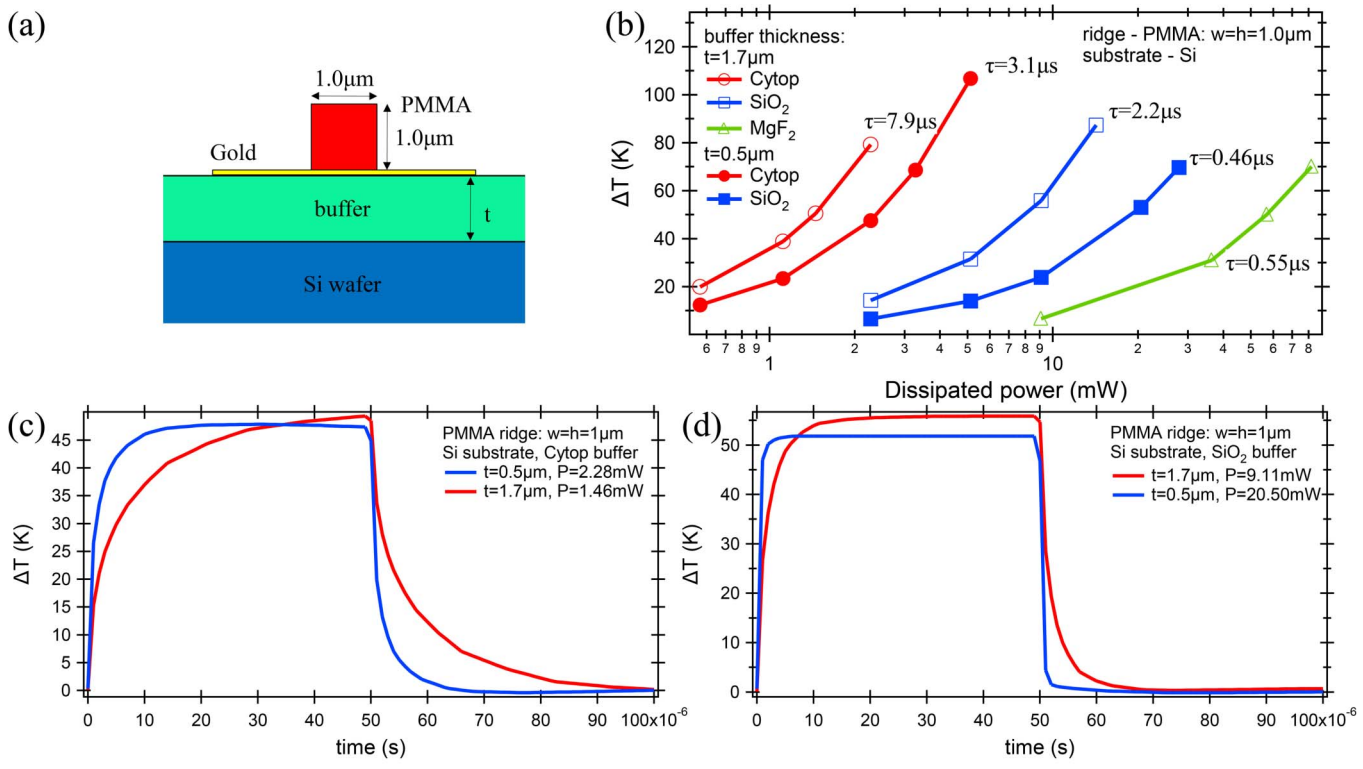

Figure 2 | Influence of the buffer layer on the switching performances. (a) Cross-section of the investigated DLSPPW structures with a PMMA ridge on top of a gold stripe deposited on an underlying buffer layer on the Si wafer. (b) Temperature change in the PMMA ridge versus power dissipated by the gold electrode for different buffer layer materials (Cytop, SiO_2 and MgF_2) and thicknesses (t = 0.5 and 1.7 μm). The temporal temperature changes in the PMMA ridge at the frequency of 10 kHz for (c) Cytop and (d) SiO_2 buffer layers with the thickness of 0.5 and 1.7 μm.

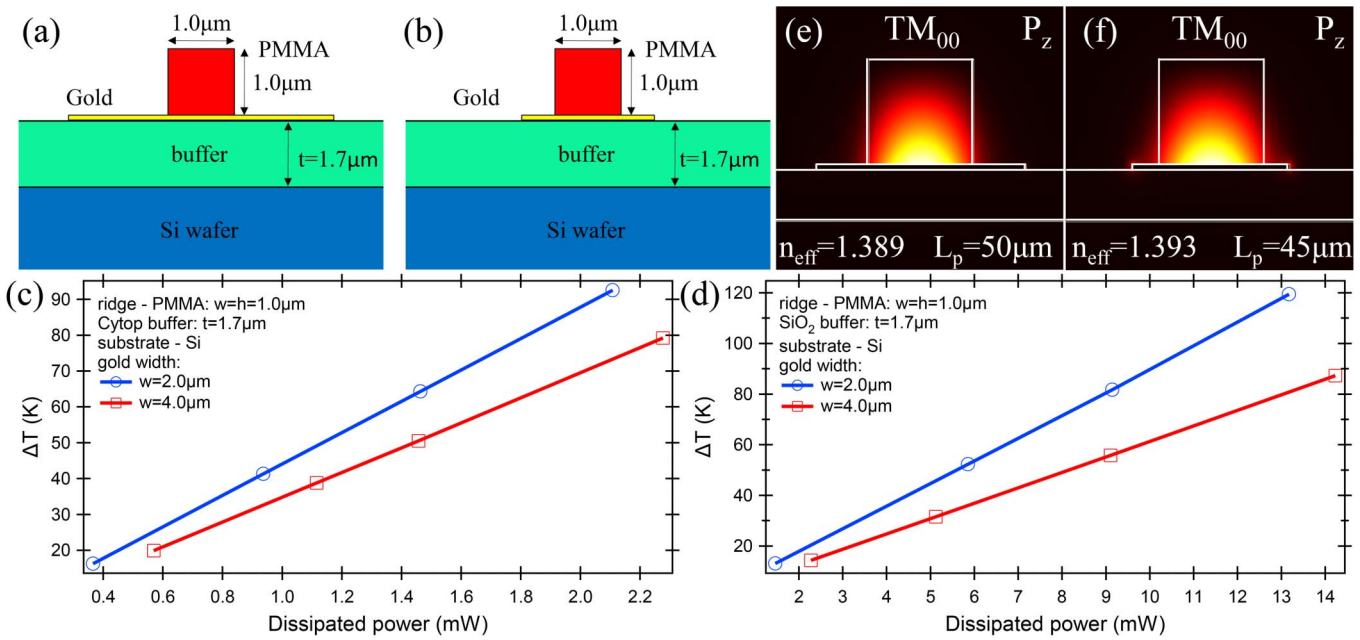

Figure 3 | Influence of the electrode width on the switching performances. (a), (b) Cross-section of the investigated DLSPPW structures with a PMMA ridge on top of a gold stripe of width of w = 4.0 μm (a) and w = 2.0 μm (b) deposited on an underlying 1.7 μm-thick buffer layer on the Si wafer. (c), (d) Temperature change in the ridge versus dissipated power by the metal stripe for metal width of 2.0 μm and 4.0 μm for (c) Cytop and (d) SiO_2 buffer layers. (e), (f) Field distribution plot of the power flow for structure with (e) 2 μm-wide gold stripe and (f) 1.5 μm-wide gold stripe.

the 50 nm-thick gold electrode deposited on a 1.7 μm-thick Cytop on the standard Si wafer. For this configuration, low switching power of 2.35 mW, corresponding to a temperature rise of about 80 K, was obtained with 10–90% rise time of 65 μs and 90–10% fall time of 20 μs. Further improvement was observed in terms of the switching time (20 μs rise time and 15 μs fall time) for overdriven power of ~2.8 mW corresponding to a temperature rise of about 85 K. Our calculations show very good fit with measurements for a structure with 1.7 μm-thick Cytop buffer with time constant of ~8 μs which corresponds to a rise/fall time of ~17.5 μs and dissipated power of ~2.3 mW and ~2.7 mW for a ridge temperature increases of 80 K and 85 K, respectively.

In the second case[18,19], the A-MZI-based switching structure comprised two PMMA-loaded SPP waveguides serving as the active MZI branches and heterointegrated on a SOI rib (h = 1.8 μm) waveguide platform. The DLSPP waveguides consisted of 65 nm-thick and 3 μm-wide gold stripes, on top of which dielectric PMMA ridges (w = 0.5 μm, h = 0.6 μm) were placed. For a 60 μm-long active a-MZI arm length the full switching was possible with the power consumption being 13.1 mW which corresponds to a ridge temperature change of ~61 K with a response time found to be 3.8 μs. Additionally, it was showed that power consumption could be reduced to 10.8 mW (ridge temperature change of ~45 K) with response time found to be 4.6 μs by increasing the active a-MZI arm length to 90 μm. Our calculations showed (Fig. 2) that for this configuration the time constant of ~2.2 μs can be achieved with power consumption ~9 mW and ~11 mW for ridge temperature increases of 45 K and 61 K respectively.

Discussion

In the design of TO switching elements and modulators a transient temperature change in the ridge should be known for fabrication of low-power and fast switching elements. In this paper, the transient temperature change in the ridge was studied for different buffer layer materials and different width of the metal electrodes. Additionally, the influence of the buffer layer thickness on the overall performance of the switch was studied. It was found that buffer layer materials with a high thermal conductivity coefficient ensure fast response time which is, however, at the cost of power consumption. On the other hand, for buffer layer materials with a low thermal conductivity coefficient it is possible to achieve very low power consumption but with slow response time. As the heating part of the electrode is at the same time the part of the DLSPP waveguide supporting a propagating mode and localized below the ridge, the heat dissipates to the ridge as well as to the beneath materials. In terms of the heat, the DLSPP structure can be considered as a parallel connections of thermal resistors and in row connections of thermal capacitors where as the first thermal resistor/capacitor is considered a ridge and as a second one the material below gold electrode. So, the overall performance of the structure is very strongly dependent on the materials below an electrode. It should be mentioned here that Si wafer on which a buffer layer material is deposited can be considered as a heat sink as a thermal conductivity coefficient is much higher compares to buffer layer materials and a ridge. Taking into account the above considerations one way to decrease a response time of the device, while keeping at the same time power consumption on the reasonably level is to use low thermal conductivity buffer material and decreases the buffer layer thickness. Thus, the power-time product decreases from 34.7 mW·μs to 25.7 mW·μs for Cytop buffer layer. It has to be emphasized, that power-time product is very convenient way to characterize the performances of the devices for the same increases of the ridge temperature ΔT. However, to evaluate the performance of different devices where different ridge temperature increase ΔT is assumed it is more proper to use a power-time-length product as a parameter describing a performance of the switches in terms of a switching time, power consumption and footprint. As it can be seen (Fig. 2(b)), for long a heated part of the waveguide the temperature increases as low as 20 K can be sufficient to ensures a full modulation what corresponds to a power consumption of 0.57 mW. However, it is at the cost of a footprint and insertion losses. The insertion losses can be minimalized by incorporation of short active waveguides and heating it to a high temperature. However, it is

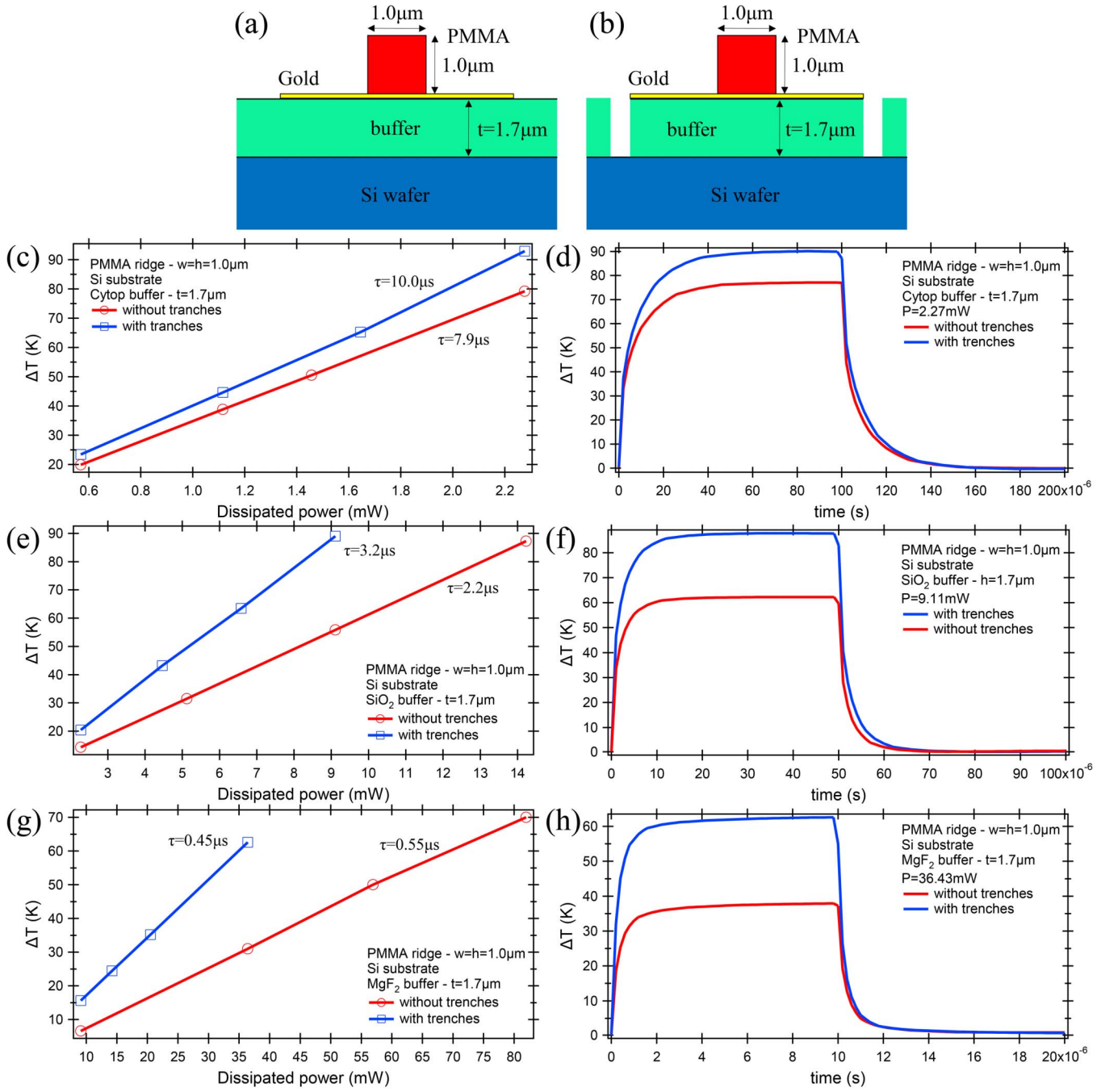

Figure 4 | Influence of the tranches on the switching performances. Cross-section of the investigated DLSPPW structures without trenches (a) and with trenches (b) with PMMA ridge on top of a gold stripe deposited on an underlying buffer layer. (c), (e) and (g) Simulation results of the temperature increase of the ridge versus dissipated power for the structures with or without thermal isolation trenches for Cytop (c), SiO_2 (e) and MgF_2 (g). (d), (f) and (h) transient response of temperature change of the ridge as a function of time for structures from (c), (e) and (g).

at the cost of a power consumption – 2 mW of power is required to increases a ridge temperature to 70 K.

The performed calculations fit very well with the experimental data for Cytop[16] and SiO_2[18,19] buffer layers and confirm the lowest experimentally achieved power-time-length product of ~1790 mW·μs·μm obtained with the Cytop buffer layer[16].

Further improvement in the performance of the switching elements was suggested in this article as well. It can be achieved either by increasing the contact area between metal electrode and ridge or by using an insulating trenches along heated part of the MZI arm. The first one can be realized by decreasing the width of the metal electrode supporting the propagating DLSPP mode. Decreasing the electrode width by factor of two reduces the power consumption about 21% for structure with Cytop buffer layer and about 36% for structure with SiO_2 layer while keeping the response time at the same value. However, it should be in mind, there is a cut off width of the gold electrode below which the propagating mode start to leaks to the beneath substrate exhibiting high losses. Based on this, the insulating trenches seem to be very attractive technology for realization of low power switching devices. Power reduction of 15% was achieved for low thermal conductivity structure (Cytop) at the cost of a response time which arises from 7.9 μs for structure without trenches to 10 μs for structure with trenches. The power-time product in this way arise from 34.7 mW·μs to 38.4 mW·μs.

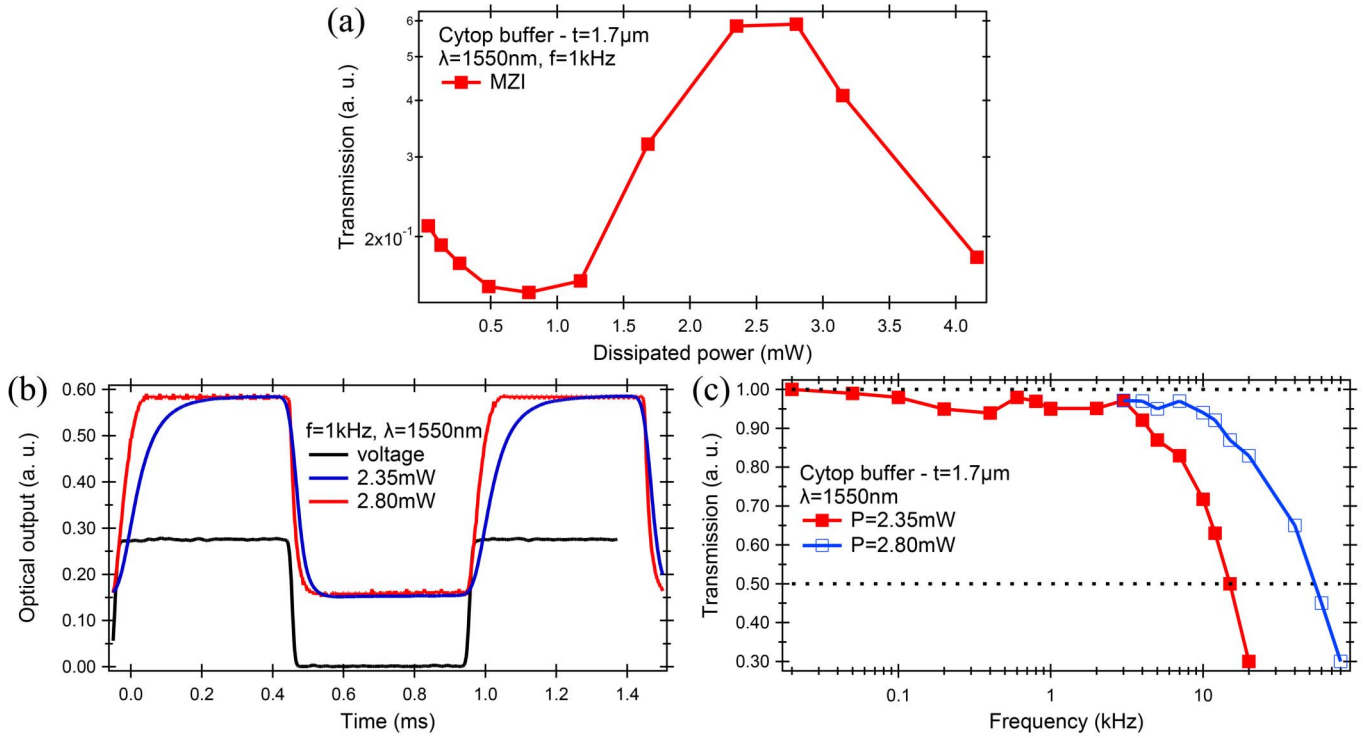

Figure 5 | MZI performances. Dependence of MZI transmission for ON applied voltage (a) on the applied electrical power for structure with Cytop buffer layer and (b) a temporal response measured at the frequency of 1 kHz for two values of applied electrical power. The black curve represents the applied voltage. (c) Dependences of normalized MZI transmission on the modulation frequency for wavelength $\lambda = 1550$ nm.

Methods

The described configuration was investigated using three-dimensional finite element method (3D-FEM) simulations using commercial software COMSOL, with which the transient temperature distribution into the ridge was investigated. The FEM is a well known technique for numerical solution of partial differential or integral equations, where the region of interest is subdivided into small segments and a relevant equation is replaced with a corresponding functional. The boundary condition of constant temperature T = 293 K was assigned to the bottom face of the silicon wafer and all surfaces in contact with air. The conductive heat transfer was assumed within solid and between solid object constituents, while the convective heat transfer was considered between surfaces of the solid materials in contact with air. Furthermore, the heat from any materials being in contact with air is dissipated by convective cooling with the convection coefficient of 10 W/m^2K.

When applying the voltage to the electrode (gold) pads, the passage of the electrical current through a metal stripe causes dissipation of the electrical energy into heat (ohmic heating), which is then transferred to any materials in contact with the gold electrodes through conductive heat transfer. The amount of heat transferred to the area of interest (ridge) depends upon the thermal conductivity coefficients of the ridge and materials below the gold electrode, contact area and thickness of the ridge and material below. As the silicon wafer has much higher thermal conductivity coefficient, it can be treated as a heat sink.

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Author contributions

J.G. and S.B. conceived the idea, design the structures. J.G. performed theoretical calculations, FEM simulations and measurements. J.G. wrote the manuscript and S.B. supervised the project.

Additional information

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