SCIENTIFIC REPORTS

OPEN

SUBJECT AREAS:
ELECTRONIC DEVICES
ELECTRONIC PROPERTIES AND MATERIALS

Received
8 April 2014

Accepted
27 May 2014

Published
19 June 2014

Correspondence and requests for materials should be addressed to X.J.Z. (xjzhang@suda.edu.cn); X.H.Z. (xhzhang@mail.ipc.ac.cn) or J.S.J. (jsjie@suda.edu.cn)

# A High-yield Two-step Transfer Printing Method for Large-scale Fabrication of Organic Single-crystal Devices on Arbitrary Substrates

Wei Deng, Xiujuan Zhang, Huanhuan Pan, Qixun Shang, Jincheng Wang, Xiaohong Zhang, Xiwei Zhang & Jiansheng Jie

Institute of Functional Nano & Soft Materials (FUNSOM) & Collaborative Innovation Center of Suzhou Nano Science and Technology, Jiangsu Key Laboratory for Carbon-Based Functional Materials & Devices, Soochow University, Suzhou Jiangsu, 215123, P. R. China.

**Single-crystal organic nanostructures show promising applications in flexible and stretchable electronics, while their applications are impeded by the large incompatibility with the well-developed photolithography techniques. Here we report a novel two-step transfer printing (TTP) method for the construction of organic nanowires (NWs) based devices onto arbitrary substrates. Copper phthalocyanine (CuPc) NWs are first transfer-printed from the growth substrate to the desired receiver substrate by contact-printing (CP) method, and then electrode arrays are transfer-printed onto the resulting receiver substrate by etching-assisted transfer printing (ETP) method. By utilizing a thin copper (Cu) layer as sacrificial layer, microelectrodes fabricated on it *via* photolithography could be readily transferred to diverse conventional or non-conventional substrates that are not easily accessible before with a high transfer yield of near 100%. The ETP method also exhibits an extremely high flexibility; various electrodes such as Au, Ti, and Al etc. can be transferred, and almost all types of organic devices, such as resistors, Schottky diodes, and field-effect transistors (FETs), can be constructed on planar or complex curvilinear substrates. Significantly, these devices can function properly and exhibit closed or even superior performance than the device counterparts fabricated by conventional approach.**

Compared to their inorganic counterparts, one-dimensional (1D) organic nanostructures offer several unique advantages, such as inherent compatibility with plastic substrates, amenability to roll-to-roll large area producing, flexibility and low-temperature processing requirements[1–3]. Also, the single-crystal 1D organic nanostructures offer the possibility to construct organic electronic devices with unprecedented performance[2]. It is known that the existence of large amount of defects and grain boundaries in the amorphous or polycrystalline organic films is the important reason for the inferior performance of conventional organic devices[4]. However, till now most organic single-crystal devices are fabricated on rigid, flat, and smooth substrates such as $SiO_2$/Si and glass, and the choice of substrates is generally limited by the processing temperature, compatibility with chemicals, and handling requirements etc[5–7]. Fabrication of organic electronic devices on non-conventional substrates, such as paper, poly(dimethylsiloxane) (PDMS), tapes, non-planar or arbitrary substrates will enable the utilization of many desired properties of the substrates, including flexibility, transparency, biocompatibility and low cost, and thus bring about a lots of new applications in flexible organic circuits[8,9], paper electronics[10], solar cells[11], conformal sensors[12], and biointegrated electronics[13].

Unfortunately, traditional microelectronic processing techniques, including photolithography, metallization, and lift-off, are still not applicable for the organic single-crystal devices, although these techniques have been demonstrated to be highly successful for the construction of large-scale integrated electronic devices based on inorganic semiconductors. This is because (i) organic materials are largely incompatible with photolithography process. The inferior chemical/physical stability of organic materials makes them hard to stand the photolithography and plasma involved electrode deposition processes[14], (ii) many flexible/transparent substrates suffer from problems like shrinkage or degradation due to their incompatibility with the harsh solvents usually used in

the photolithography and lift-off processes, and (iii) these techniques are normally restricted to the flat substrates and not applicable to the non-conventional substrates, such as the substrates with curved surfaces[15].

To overcome the difficulty in photolithography, various methods including shadow mask[9,10], inkjet print[16], and in-situ/post-growth integration techniques[17–19], have been developed to fabricate the organic nanostructure based devices. However, the inherent disadvantages of shadow mask and inkjet print methods, such as the poor precision for mask alignment/ink positioning and the limitation in minimum feature size, impede their applications in integrated organic devices. The existing in-situ integration methods usually involve the direct growth of organic nanostructures on pre-fabricated electrode circuits[13], but the solution based or high temperature initiating growth process will inevitably cause the damage to the device substrates. In the post-growth integration method, the as-prepared organic NWs are dispersed on the pre-fabricated electrode circuits, while the bottom-contact device configuration usually offers poor device performance. Recently, various transfer-printing methods have been developed to achieve the transfer of inorganic nanowires (NWs)-based devices onto diverse substrates[20–23]. However, these methods are not applicable to the organic nanostructures because photolithography on the NWs is required in these processes. Also, due to the use of strong acid (for etching the sacrificial layer like $SiO_2$ etc.)[23], these methods show limited applications on the transfer of device with more sophisticated structures, such as Schottky diodes and field-effect transistors (FETs).

Herein, we report an alternative and yet simple, versatile, and high-yield two-step transfer printing (TTP) method that enables fabrication of organic devices onto diverse conventional or non-conventional substrates that are not easily accessible before. The transfer yield for the microelectrode arrays is very high, and the devices eventually formed can function properly with excellent reproducibility. Various organic electronic devices, including resistors, Schottky diodes, and FETs were demonstrated by using the TTP method. Notably, these devices exhibited performance comparable to the device counterparts fabricated by conventional methods, demonstrating the high reliability, robustness, and efficiency of the TTP method. It is expected that the TTP method will have important applications in future flexible organic electronics.

## Results and discussion

The TTP method basically includes two different transfer printing processes: organic NWs are first transfer-printed from the growth substrate to the desired receiver substrate as highly aligned arrays by contact-printing (CP) method, and then electrodes are transfer-printed onto the resulting receiver substrate by etching-assisted transfer printing (ETP) method. We note that CP method is a flexible and convenient way of transferring NWs to nonadhesive or adhesive target substrates with controllable density (Figure S1 in Supporting Information)[24,25]. Figure 1(a) illustrates the ETP process for organic NW based device fabrication, which includes two different approaches. At the beginning of both approaches, a thin copper (Cu) layer (300 nm) was deposited on Si substrate *via* electron-beam evaporation and served as sacrificial layer in subsequent transfer processes. The electrode arrays were then fabricated on the sacrificial layer through routine photolithography and lift-off processes (Figure 1(a), (I)). In first approach, a layer of poly(methylmethacrylate) (PMMA) (solids content 6%, molecular weight 495 kDa) was spin-coated on the electrode arrays, and hardened at 120°C for 120 s

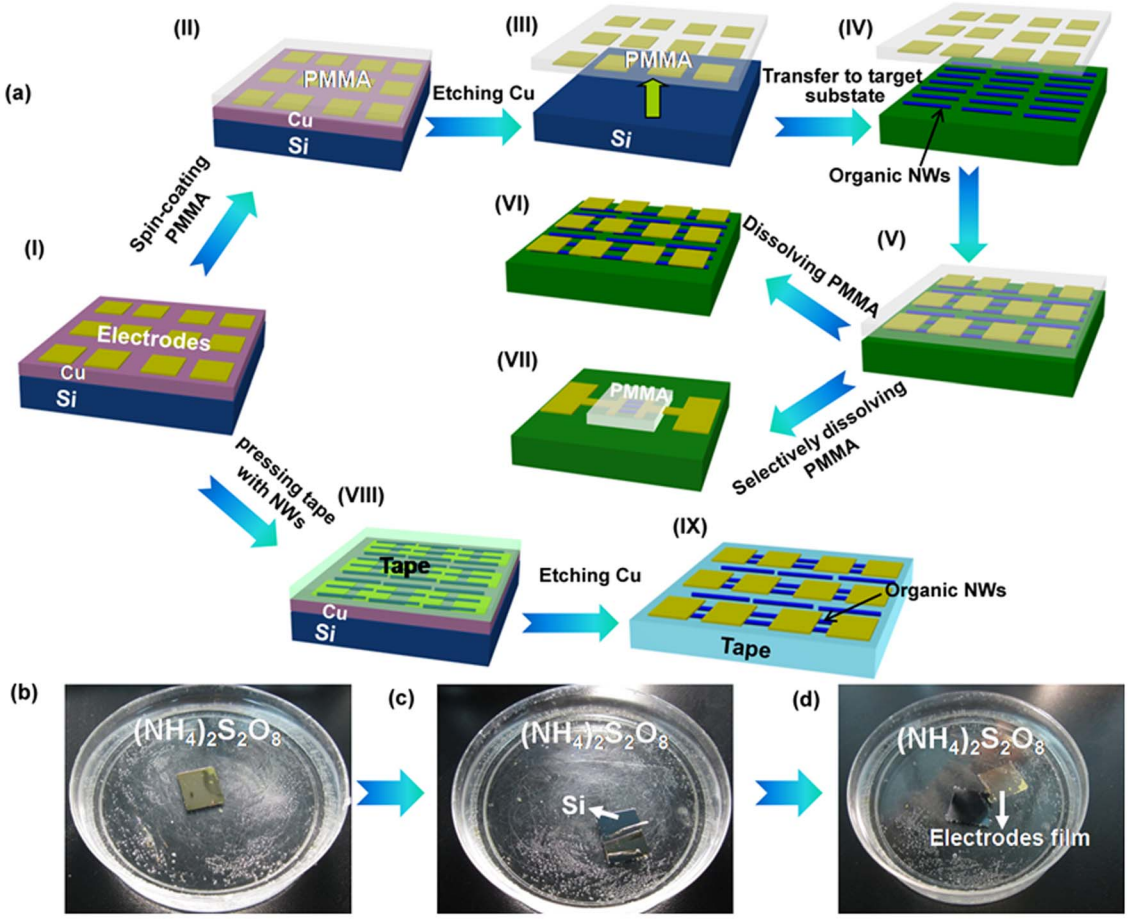


**Figure 1** | (a) Schematic illustration of the TTP method for organic NW based device fabrication. (b), (c) and (d) show the corresponding photographs for the ETP process.

on the hotplate, functioning as a temporary holder (Figure 1(a), (II)). Next, the whole structure was soaked in saturated ammonium persulfate ($(NH_4)_2S_2O_8$) solution at room temperature for 1–3 hours to etch away the sacrificial Cu layer. After that, the PMMA/electrodes film was released and floated freely on the surface of the solution (Figure 1(a), (III)). Photographs in Figure 1b–1d clearly show the ETP process for PMMA/electrodes film releasing from the Cu/Si substrate. The PMMA/electrodes film was then transferred to a deionized (DI) water bath to remove remaining etchant. The target substrate with CP transferred NW arrays was put underneath the floating PMMA-supported electrodes and then lifted up (Figure 1(a), (IV) and (V)). Finally, the PMMA film was dissolved quickly with acetone for ~5 s, leaving behind the top-contacted NW devices on the target substrate (Figure 1(a), (VI)). Also, the PMMA film can be selectively removed at the electrode pad positions to avoid the possible damage of organic solvent to the organic NWs (Figure 1(a), (VII)). In second approach, flexible adhesive tape was used as the receive substrate. After the transfer of organic NWs with CP method, the adhesive tape, along with NWs on it, was pressed against the electrodes patterned Cu/Si substrate (Figure 1(a), (VIII)), then followed by etching away the sacrificial Cu layer to separate the NW devices onto the tape from the donor Si substrate, as shown in Figure 1(a), (IX).

Figure 2(a)–2(f) show the photographs of the microelectrode arrays fabricated by the ETP method on diverse substrates. Notably, this method shows little limitation on the types of target substrates; microelectrode arrays for different kinds of devices, including resistors, diodes, and transistors, could be readily fabricated and transferred onto diverse substrates, such as conventional substrates of $SiO_2$ (300 nm)/Si, glass and non-conventional substrates of paper, PDMS, thermal release tape (TRT), and Kapton tape. It is noteworthy that a high yield of near 100% for the microelectrode arrays can be achieved, as shown in Figure 2(g)–2(i), revealing the high reliability of the proposed ETP method. Local defects and damages are occasionally observed in the ETP fabricated electrode array (Figure 2(f), marked with a red circle), but they normally come from the complicated photolithography, metallization, and lift-off processes for microelectrode fabrication, while have no relation with the subsequent ETP process. It is believed that these defects can be effectively excluded as long as the electrodes fabrication and ETP transfer are well implemented. The ETP process seemingly shares partial common technological features with the previously reported graphene transfer method[26], in which graphene film is released and transferred from the growth substrate of Cu foil, however microelectrode transfer or even the whole device transfer by using this method has never been exploited thus far. In a previous work which is most similar to us process, Au electrodes were pre-patterned on $SiO_2$/Si substrate then released by etching the $SiO_2$ sacrificial layer in a HF solution[23]. However, the use of HF etchant seriously limits the types of metallic electrodes or device structures that can be accessible. Therefore, our work represents an important progress for extending the transfer printing method towards future advanced device applications.

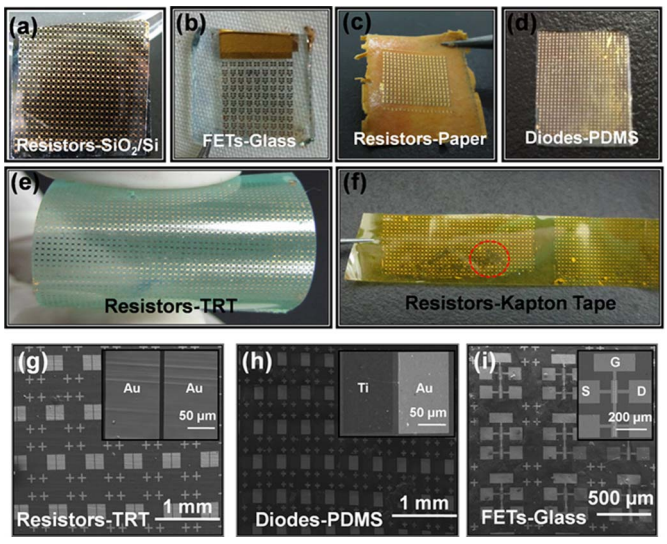


**Figure 2** | Photographs of the transferred microelectrode arrays on various substrates *via* EPT method, including conventional substrates such as (a) $SiO_2$/Si, (b) glass, and non-conventional substrates such as (c) paper, (d) PDMS, (e) thermally release tape, (f) Kapton tape. (g), (h), and (i) show the representative SEM images of the transferred microelectrode arrays, including resistors, diodes, and top-gate FETs, on diverse substrates.

Evidently, the present TTP method offers several important advantages compared to the previous methods[9–10,16]. First, organic NW devices can be constructed on almost any conventional and non-conventional substrates, since the TTP process involves no harsh fabrication process, thermal stress, and vacuum condition. The high transfer yield also guarantees its application in future integrated devices. Second, the TTP method exhibits extremely high flexibility; most of the common electrodes such as Au, Ag, Ti, and Al etc. can be transferred because $(NH_4)_2S_2O_8$ doesn't react with them, and therefore almost all types of organic devices, such as resistors, diodes and transistors, can be constructed. Third, the TTP method can bridge up the gap between traditional photolithography techniques and organic devices. It surpasses conventional shadow mask or inkjet print methods. It is expected that new organic single-crystal devices with more sophisticated structures as well as higher integration level can be realized by using the TTP method. For instance, top-gate FETs, which are not accessible before for organic single-crystal devices, could be readily fabricated through the TTP method (discussed below). Forth, the use of flexible and rollable substrates in the TTP method, such as adhesive tapes, allows the device fabrication implementing in a cost- and time-effective manner, e.g., roll-to-roll (R2R) method can be utilized, thus facilitating the large-scale applications of the organic nanodevices.

By using the TTP method, various devices were successfully constructed from the copper phthalocyanine (CuPc) NWs and their device characteristics were further assessed. Figure 3(a) and 3(b) depict the representative current *versus* voltage (*I-V*) curves of the resistors and Schottky diodes fabricated on $SiO_2$/Si, glass, PDMS, and TRT substrates, respectively, in dark at room temperature. Significantly, it is noted that the devices fabricated by TTP method can function properly on various substrates; I-V curves of the resistors exhibit good linearity, while pronounced rectifying behaviors are observed for the Schottky diodes. To avoid any performance fluctuation caused by the variation of NW number in device channels, the CP process for NW transferring in first step was carefully carried out to ensure nearly the same NW densities on various substrates. In particular, for the adhesive substrates like PDMS and tapes, the NWs were first transferred to a rigid substrate of $SiO_2$/Si or glass, and then the transfer was accomplished by adhering the NW arrays to the adhesive substrates. In this work, the NW densities are controlled to be ~6/100 μm on the receiver substrates. To evaluate the impact of substrate types on device performances, 50 resistor devices on each substrates were measured and the statistical distributions of the dark conductance ($G = I/V$) are depicted in Figure S2. Notably, similar results are obtained on various substrates; the mean conductance is 0.44, 0.46, 0.42, 0.48 pS on $SiO_2$/Si, glass, PDMS, and TRT substrates, respectively, indicating the high reproducibility and reliability of the TTP approach. By taking into account the mean diameter of the NWs of ~550 nm and the device channel length of 10 μm, the conductivities of the CuPc NWs could be estimated to be 0.2 $\mu Scm^{-1}$ in dark. Moreover, investigations on the Schottky diodes on various sub-

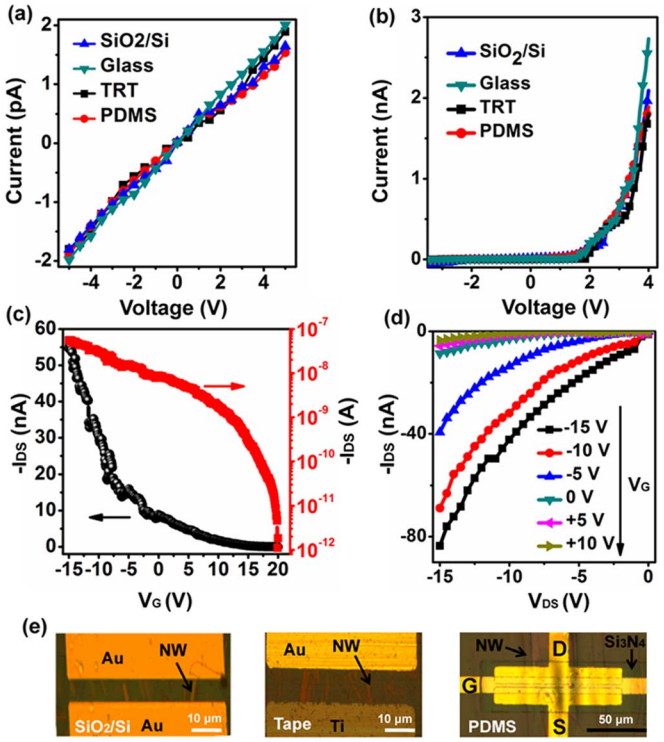


**Figure 3** | Representative I-V curves of CuPc NWs based resistors (a) and Schottky diodes (b) on $SiO_2$/Si, glass, PDMS, and TRT substrates, respectively. (c) The transfer characteristics of CuPc NW based top-gate FETs measured at $V_{DS} = -10$ V on PDMS. (d) Output characteristics of the top-gate FET. $V_G$ varied from −15 to +10 V in a step of +5 V. (e) Optical microscope images of the CuPc NW based devices, including resistor, Schottky diode, and top-gate FET, fabricated on $SiO_2$/Si, tape, and PDMS, respectively.

strates also disclose an excellent reproducibility; the mean rectification ratios are deduced to be 39.5, 40.8, 41.2, and 40.2 on $SiO_2$/Si, glass, PDMS, and TRT substrates, respectively, at a voltage range of ±5 V. Since the Schottky diodes based on organic nanostructures are rarely reported, we can't compare the diode performance with previous results directly. However, in comparison with the conventional organic film based Schottky diodes, which typically have a low rectification ratio less than $10$[27,28], our devices exhibit a large superiority due to the single-crystalline nature of the organic NWs as well as the unique approach for device construction. It is noted that, in above measurements, the residual PMMA on the electrode arrays were fully removed by quickly soaking the devices in acetone for 5 s to facilitate the electrical measurements. However, this may bring the concern that the organic NWs will be damaged during the solvent treatment. To address this issue, an especially designed electrode pads with much longer electrical connections were adopted, as shown in Figure S3(a) and 3(b). PMMA on the electrode pads could be selectively dissolved so as to facilitate the direct comparison of the electrical characteristics of the device before and after removing PMMA (Figure S3(c)). Notably, from Figure S3(d), no visible degradation of device performance is observed, indicating that the CuPc NWs are insensitive to acetone. Certainly, this electrode design can be extended to other organic NWs which are not so stable in organic solvent.

Besides the resistors and diodes, devices with much more sophisticated structure, i.e., top-gate FETs were also fabricated on various substrates, as shown in Figure 3(c) and 3(d), and Figure S4. The top-gate FET consists of a CuPc NWs channel, Au source and drain electrodes, a $Si_3N_4$ (150 nm) dielectric layer, and an Au top gate. From the electrical output characteristics, i.e., source-drain current ($I_{DS}$) versus source-drain voltage ($V_{DS}$) at varied gate voltage ($V_G$) of a typical device on PDMS (Figure 3(d)), it is noted that the device conductance increases monotonously with the decrease of $V_G$, which is the typical feature of a p-channel metal-oxide-semiconductor FET (MOSFET). This result is consistent with the p-type characteristic of the CuPc NWs. Further analysis on the electrical transfer characteristics of the device, in Figure 3(c), discloses a hole mobility ($\mu$) of 0.04 $cm^2V^{-1}s^{-1}$ according to the equation $\mu = g_m L/WC_0V_{DS}$[29], where $g_m = 5.1$ nS at $V_{DS} = -10$ V represents the transconductance of the FET and is deduced from the slope of the $I_{DS}$-$V_G$ curve in the linear part according to the relationship of $g_m = dI_{DS}/dV_G$, $W/L = 3.3 : 10$ is the width-to-length ratio of the NWs channel, $C_0$ is the capacitance per unit area and is given by $C_0 = \varepsilon\varepsilon_0/h$, where $\varepsilon$ is the dielectric constant of $Si_3N_4$ (7.5), $\varepsilon_0$ is vacuum permittivity, and $h$ (150 nm) is the thickness of the $Si_3N_4$ gate dielectric layer. The current on/off ratio of the device can be deduced to be $\sim 10^5$. Interestingly, the device can operate at a relatively small gate voltage range of ±15 V due to the unique top-gate structure. To gain statistical significance, more than 90 devices on PDMS substrate were measured and over 80% of the devices exhibited a mobility above 0.01 $cm^2V^{-1}s^{-1}$. Meanwhile, the mobilities of the devices fabricated on $SiO_2$/Si and glass were also measured and estimated to be 0.01–0.05 $cm^2V^{-1}s^{-1}$ (Figure S4). Although the mobilities of our devices are still lower than the best results obtained for single CuPc NW or nanoribbon (NR) based FETs (0.1–0.4 $cm^2V^{-1}s^{-1}$)[30,31], the values are comparable to the previous reports on CuPc NW or nanotube (NT) based FETs (0.0057–0.064 $cm^2V^{-1}s^{-1}$)[32] and film based FETs (0.0067 $cm^2V^{-1}s^{-1}$)[33]. Moreover, the large current on/off ratio and the low operating voltage presented in this work manifest a high performance of the top-gate CuPc NW FETs. We believe that the device performance can be substantially improved by further optimizing the device structure, reducing the contact resistance, purifying the source material and so on. Close inspection on the optical microscope images of the devices in Figure 3(e) verifies that the TTP process does not produce any visible damage to the CuPc NWs as well as the electrodes; the devices, even the top-gate FET with multilayer structure, are as perfect as that on the original Cu/Si substrate. On the other hand, after carefully examining the electrical characteristics of the TTP fabricated devices, we found that ~30% devices show non-ideal device performance, such as non-linear *I-V* curves (for resistors) and hysteresis (for Schottky diodes and top-gate FETs), indicating that the contact problem somewhat exists in the TTP fabricated devices. However, it is believed that device reproducibility could be significantly improved in the next step work by means of post-annealing and so on. The above results unambiguously demonstrate the great potential of TTP approach for producing high-performance and highly integrated organic NW devices on diverse substrates.

Organic NW based FETs are essential components for future organic electronics. While great progress has been made in the development of organic NW FETs[34,35], almost all the devices are constructed with a bottom-gate configuration. It has been well confirmed that, in inorganic FETs, top-gated devices with high-dielectric-constant (high-*k*) dielectrics can significantly reduce the required switching/operation voltage and allow the fabrication of independently addressable device arrays and functional circuits, and therefore are of significant interests[36,37]. However, due to the inadequate microelectronic techniques, top-gate organic nanostructure based FETs are rarely reported yet. Also, few methods can fabricate organic top-gate FETs on arbitrary conventional or non-conventional substrates at a wafer scale with high yield. Therefore, it appears that the TTP method can overcome the limitations of the existing microelectronic techniques, and offers the possibility to construct high-performance top-gate FETs based on the organic NWs. In order to directly compare the performance of the bottom-gate FETs with the top-gate FETs, CuPc NWs were first transferred to a

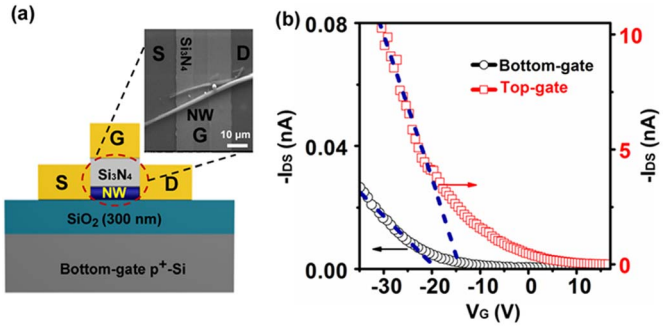


**Figure 4** | (a) Schematic illustration of the top-gate and back-gate NW FETs on a same chip. In top-gate FET, Au electrode and high-$k$ $Si_3N_4$ layer serve as the top gate and gate dielectric, respectively. In bottom-gate FET, the degenerately doped $p^+$-Si substrate and the $SiO_2$ layer serve as the bottom gate and gate dielectric, respectively. Inset shows the top-view SEM image of a top-gate NW FET fabricated on $SiO_2$/Si substrate. (b) $I_{DS}$-$V_G$ curve of the top-gate NW FET at $V_{DS} = -10$ V, along with the $I_{DS}$-$V_G$ curve of bottom-gate NW FET measured at the same conditions for comparison.

conventional $SiO_2$ (300 nm)/$p^+$-Si substrate, constituting the bottom-gate NW FETs. Afterward, the top-gate NW FETs were realized by transferring the electrodes onto the top of NWs *via* ETP method (Figure 4(a)). With this well-designed device architecture, the bottom-gate and top-gate NW FETs can be studied simultaneously, avoiding the fluctuation of NW properties. Inset in Figure 4(a) shows a typical SEM image of the top-gate CuPc NW FET fabricated on the $SiO_2$/$p^+$-Si substrate with two NWs in the conduction channel. Interestingly, it is found that the gate dielectric and gate electrode can wrap on the CuPc NWs, forming a near surrounding top-gate FET structure. As we will discuss later, this device structure will be very beneficial to the device performance improvement. Figure 4(b) depicts the representative transfer characteristics ($I_{DS}$-$V_G$) of the top-gate and bottom-gate NW FET. Notably, the top-gate FET exhibits much enhanced performance compared to the bottom-gate FET, with the current reaching two orders of magnitude higher than that in bottom-gate FET at the same conditions. In addition, for the top-gated NW FET, the $g_m$ at $V_{DS} = -10$ V is about 1.2 nS, corresponding to a hole mobility of $\mu = 0.01$ $cm^2V^{-1}S^{-1}$, which is nearly 34 times larger than that of the bottom-gated FET ($g_m$ = 0.07 nS, $\mu = 0.0003$ $cm^2V^{-1}S^{-1}$). The remarkably superior device performance of the top-gate NW FETs could be attributed to their distinct structures. The high-$k$ $Si_3N_4$ dielectric as well as the unique surrounding gate structure, make for a large gate capacitance and thus a higher gate modulation capability for the top-gate FETs.

The proposed TTP method exhibits extremely high flexibility and is able to fabricate organic NW devices on a large variety of substrates, even on curved or other non-planar surfaces, as demonstrated in Figure 5. The microelectrode arrays can be successfully transferred to various non-planar substrates, including gloved finger tips, cylindrical and spherical PDMS, and leaf. From Figure 5(a)–5(d), it is clear that the metal electrodes are smoothly following the deformation of the curved surfaces. It is noteworthy that these types of device configurations are extremely difficult to be achieved using established electronic technologies, owing to the intrinsically planar nature of the patterning, deposition, etching, materials growth methods that exist for fabricating such systems[15].

The high flexibility of organic NWs also makes it suitable to be used in the flexible electronics. Figure 5(e) shows the photograph of the CuPc NW devices fabricated on the cylindrical PDMS substrate by TTP method. The corresponding optical microscope images (Figure 5(f) and inset in Figure 5(e)) reveal that the NWs can bridge between the two Au electrodes, similar to that on the flat PDMS substrate. Electrical measurements on the devices demonstrate the good ohmic contacts of Au electrodes with the NWs on the cylindrical PDMS (Figure 5(e)), and the conduction current is close to that obtained on the flat PDMS. From the above results, it is believed that the TTP method provides an effective route for integrating well-developed planar device technologies onto the surfaces of complex curvilinear objects, suitable for diverse applications that cannot be achieved by conventional means.

To further exploit the great potential of the TTP method for future low-cost and flexible device applications, a glossy brochure paper was adopted as the device substrate and CuPc NW photodetectors were constructed on it. The as-synthesized CuPc NWs were first transferred onto the glossy brochure paper, and then the microelectrode arrays consisting of Au-Au (50 nm) electrode pairs were transferred on the top of the NWs *via* ETP method, forming the

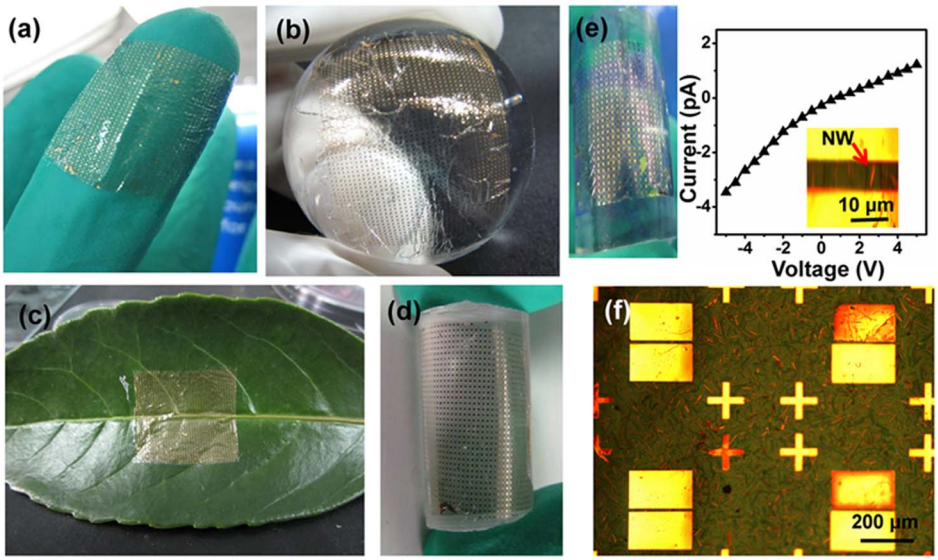


**Figure 5** | Photographs of the transferred microelectrode arrays on curved substrates, such as (a) gloved finger tips, (b) hemispheroidal PDMS, (c) leaf, and (d) cylindrical PDMS. (e) Photograph and representative I-V curve of the CuPc NW resistor devices fabricated on cylindrical PDMS substrate. Inset shows the enlarged optical image of the device on curved PDMS. (f) Optical image of the organic NW resistors on the cylindrical PDMS substrate.

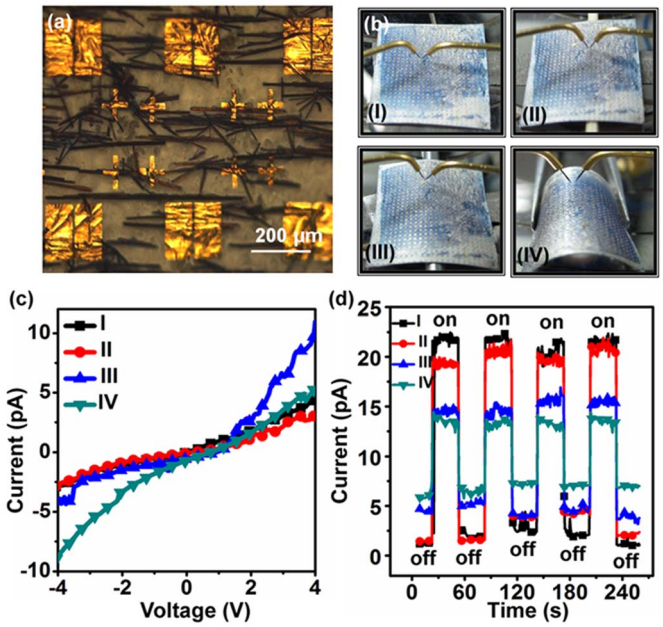


**Figure 6** | (a) Optical microscope image of devices fabricated on the glossy brochure paper *via* TTP method. (b) Photographs of the device with different bending curvature. The corresponding dark *I-V* curves are shown in (c). Curve I, II, III, and IV correspond to the bending curvatures of 0, 0.3, 0.4, and 0.8 $cm^{-1}$, respectively. (d) Photoresponse of the bended device under on-off modulated white light illumination (0.5 $mWcm^{-2}$). The voltage bias was fixed at +10 V.

top-contacted resistor devices, as shown in Figure 6(a). Upon bending, as shown in Figure 6(b), the dark current of the device changes little (Figure 6(c)), indicating that the device is robustness against the tensile stress. The device exhibits pronounced photoresponse when it is illuminated with on-off modulated white light (intensity ~0.5 $mWcm^{-2}$), as shown in Figure 6(d). The impact of bending curvature on the device performance is investigated; the device $I_{light}/I_{dark}$ ratio decreases mildly from 14 at curvature = 0 $cm^{-1}$ to 3.3 at curvature = 0.8 $cm^{-1}$, while the response speed shows little dependence on the bending curvature and is less than 1s within the measurement range.

## Conclusion

In summary, we developed a novel two-step transfer printing method to achieve the fabrication of a host of organic NW based devices, such as resistors, diodes, and top-gate FETs, onto diverse conventional or non-conventional substrates. The TTP method combines two different transfer-printing processes: the organic NWs transfer *via* CP method and the electrodes transfer *via* ETP method. The ETP method has the advantages of simplicity, low cost, and nearly 100% transfer yield regardless of monolayer and multilayer electrodes, and can transfer most of the common metallic electrodes. The devices fabricated by TTP method exhibited closed and even superior performance as compared to the devices fabricated *via* conventional methods. The TTP method can extend photolithography process to organic electronics, and thus surpass the conventional inkjet printing and shadow mask methods in terms of high integration level and low cost. On the other hand, the TTP method will endow the organic single-crystal devices with desirable properties, such as flexibility, stretchability, transparency, and biocompatibility through the use of non-conventional substrates, and thereby impact a range of applications, such as biosensing, flexible displays, robotics, and energy conversion systems. Given the versatility and reproducibility of the TTP method, we believe that it will open up unique opportunities for integrations of organic devices onto various substrates or the surfaces of complex curvilinear objects, and is suitable for diverse applications that cannot be achieved by conventional means.

## Methods

**Growth of CuPc NW arrays and transfer of NWs onto various substrates.** Synthesis of the CuPc NW arrays were conducted in a horizontal quartz tube furnace via physical vapor deposition (PVD). Briefly, a predetermined amount of CuPc powder (J&K, >90%) as the source material was placed at the center of the furnace, while the Si substrate with 6 nm Au on was placed at downstream direction with distance of ~8 cm from the source. The reaction chamber was flushed and filled with 60 sccm Ar carrier gas after it was evacuated to a base pressure of 2 Pa. The pressure in the tube was adjusted to 220 Pa before heating. The temperature of the source material and absorbent were maintained at 415°C during the experiment, while the substrate temperature was ~180°C. After a growth duration of 2 h, large-area aligned CuPc NW array was obtained on the Si substrate (Figure S1). The CuPc NWs were then transferred to the device substrate by the CP method, which involves directional sliding of the CuPc NWs growth substrate against the device substrate, resulting in the well-aligned NWs on the device substrate (Figure S1).

**Device construction.** The microelectrode arrays were fabricated on the Cu (300 nm)/Si substrate via standard photolithography, metallization, and lift-off processes. Cu served as the sacrificial layer in the ETP process. Photolithography was performed in Karl Suss (MJB4) mask aligner with positive photoresist (AR-P 5350). The metallic electrodes were deposited by E-beam evaporation (Kurt J Lesker Company, PVD 75). To fabricate the resistors, symmetric electrode pairs of Au-Au (50 nm) were used, while asymmetric electrode pairs of Au-Ti (50 nm) was adopted for the Schottky diodes. To construct the top-gate FETs, Au (50 nm) source and drain electrodes with channel width of 200 μm and channel length of 10 μm were first defined by photolithography on the Cu layer, and then high-*k* $Si_3N_4$ (150 nm) gate dielectric was deposited by magnetron sputtering (Kurt J Lesker Company, PVD 75) on the source/drain electrodes, followed by the deposition of Au (50 nm) gate electrode on the dielectric layer.

All the electrical measurements were conducted using a semiconductor characterization system (Keithley 4200-SCS) on a probe station (M150, Cascade) in a clean and shielded box at room temperature. To determine the photoconductive characteristics of the CuPc NWs on the paper, the white light from the optical microscope on the probe station was used as the light source (~0.5 $mWcm^{-2}$).


1. Chang, J. F. *et al.* Enhanced mobility of poly(3-hexylthiophene) transistors by spin-coating from high-boiling-point solvents. *Chem. Mater.* **16**, 4772–4776 (2004).
2. Zhang, C. Y. *et al.* Facile one-step fabrication of ordered organic nanowire films. *Adv. Mater.* **21**, 4172–4175 (2009).
3. Moonen, P. F., Yakimets, I. & Huskens, J. Fabrication of transistors on flexible substrates: from mass-printing to high-resolution alternative lithography strategies. *Adv. Mater.* **24**, 5526–5541 (2012).
4. Tang, Q. X., Li, H. X., Liu, Y. L. & Hu, W. P. High-performance air-stable n-type transistors with an asymmetrical device configuration based on organic single-crystalline submicrometer/nanometer ribbons. *J. Am. Chem. Soc.* **128**, 14634–14639 (2006).
5. Wang, X. F. *et al.* High-performance organic-inorganic hybrid photodetectors based on P3HT:CdSe nanowire heterojunctions on rigid and flexible substrates. *Adv. Funct. Mater.* **23**, 1202–1209 (2013).
6. Jiang, H. *et al.* Atomically flat, large-sized, two-dimensional organic nanocrystals. *Small.* **9**, 990–995 (2013).
7. Chang, H. C., Liu, C. L. & Chen, W. C. Flexible nonvolatile transistor memory devices based on one-dimensional electrospun P3HT:Au hybrid nanofibers. *Adv. Funct. Mater.* **23**, 4960–4968 (2013).
8. Mcalpine, M. C., Ahmad, H., Wang, D. & Heath, J. R. Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors. *Nat Materials.* **6**, 379–385 (2007).
9. Sekitani, T., Zschieschang, U., Klauk, H. & Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nat. Materials.* **7**, 1015–1022 (2010).
10. Zschieschang, U. *et al.* Organic electronics on banknotes. *Adv. Mater.* **23**, 654–658 (2011).
11. Yoon, S. M. *et al.* Fluorinated copper phthalocyanine nanowires for enhancing interfacial electron transport in organic solar cells. *Nano Lett.* **12**, 6315–6321 (2012).
12. Litt, B. & Rogers, J. A. Dissolvable films of silk fibroin for ultrathin conformal bio-integrated electronics. *Nat. Materials.* **9**, 511–518 (2010).
13. Khodagholy, D. *et al.* In vivo recordings of brain activity using organic transistors. *Nat. Communications.* **4**, 1575–1582 (2013).
14. Liu, S. H., Wang, W. M., Briseno, A. L., Mannsfeld, S. C. B. & Bao, Z. N. Controlled deposition of crystalline organic semiconductors for field-effect-transistor applications. *Adv. Mater.* **21**, 1217–1232 (2009).
15. Ko, H. C. *et al.* hemispherical electronic eye camera based on compressible silicon optoelectronics. *Nature* **454**, 748–753 (2008).
16. Russo, A. *et al.* Pen-on-paper flexible electronics. *Adv. Mater.* **23**, 3426–3430 (2011).

17. Li, H. Y. *et al.* High-mobility field-effect transistors from large-area solution grown aligned $C_{60}$ single crystals. *J. Am. Chem. Soc.* **134**, 2760–2765 (2012).
18. Minari, T., Liu, C., Kano, M. & Tsukagoshi, K. Controlled self-assembly of organic semiconductors for solution-based fabrication of organic field-effect transistors. *Adv. Mater.* **24**, 299–306 (2012).
19. Briseno, A. L. *et al.* Patterning organic single-crystal transistor arrays. *Nature* **444**, 913–917 (2006).
20. Lee, C. H., Kim, D. R. & Zheng, X. L. Fabricating nanowire devices on diverse substrates by simple transfer-printing methods. *Proc. Natl. Acad. Sci. U.S.A.* **107**, 9950–9955 (2010).
21. Lee, C. H., Kim, D. R. & Zheng, X. L. Fabrication of Nanowire Electronics on Nonconventional Substrates by Water-Assisted Transfer Printing Method. *Nano Lett.* **11**, 3435–3439 (2011).
22. Carlson, A., Bowen, A. M., Huang, Y., Nuzzo, R. G. & Rogers, J. A. Transfer Printing Techniques for Materials Assembly and Micro/Nanodevice Fabrication. *Adv. Mater.* **24**, 5284–5318 (2012).
23. Thanh, Q. N. *et al.* Transfer-printing of as-fabricated carbon nanotube devices onto various substrates. *Adv. Mater.* **24**, 4499–4504 (2012).
24. Takahashi, T. *et al.* A. Monolayer resist for patterned contact printing of aligned nanowire arrays. *J. Am. Chem. Soc.* **131**, 2102–2103 (2009).
25. Fan, Z. Y. *et al.* Toward the development of printable nanowire electronics and sensors. *Adv. Mater.* **21**, 3730–3743 (2009).
26. Huang, X., Zeng, Z. Y., Fan, Z. X., Liu, J. Q. & Zhang, H. Graphene-Based Electrodes. *Adv. Mater.* **27**, 5979–6004 (2012).
27. Rajaputra, S., Vallurupalli, S. & Singh, V. P. Copper phthalocyanine based Schottky diode solar cells. *J. Mater Sci: Mater Electron.* **18**, 1147–1150 (2007).
28. Takshi, A., Dimopoulos, A. & Madden, J. D. Depletion width measurement in an organic Schottky contact using a metal-semiconductor field-effect transistor. *Appl. Phys. Lett.* **91**, 083513 (2007).
29. Wu, D. *et al.* Device structure-dependent field-effect and photoresponse performances of p-type ZnTe:Sb nanoribbons. *J. Mater. Chem.* **22**, 6206–6212 (2012).
30. Tang, Q. X. *et al.* Low Threshold voltage transistors based on individual single-crystalline submicrometer-sized ribbons of copper phthalocyanine. *Adv. Mater.* **18**, 65–68 (2006).
31. Xiao, K. *et al.* Metastable copper-phthalocyanine single-crystal nanowires and their use in fabricating high-performance field-effect transistors. *Adv. Funct. Mater.* **19**, 3776–3780 (2009).
32. Jung, J. S. *et al.* Rectangular nanotubes of copper phthalocyanine: application to a single nanotube transistor. *Chem. Mater.* **22**, 2219–2225 (2010).
33. Bao, Z. N., Lovinger, A. J. & Dodabalapur, A. Highly ordered vacuum-deposited thin films of metallophthalocyanines and their applications in field-effect transistors. *Adv. Mater.* **9**, 42–44 (1997).
34. Tseng, H. R. *et al.* High mobility field effect transistors based on macroscopically oriented regioregular copolymers. *Nano Lett.* **12**, 6353–6357 (2012).
35. Dong, S. H. *et al.* Solution-crystallized organic semiconductors with high carrier mobility and air stability. *Adv. Mater.* **24**, 5576–5580 (2012).
36. Hwang, D. K. *et al.* Top-gate organic field-effect transistors with high environmental and operational stability. *Adv. Mater.* **23**, 1293–1298 (2011).
37. Liao, L. *et al.* High-performance top-gated graphene-nanoribbon transistors using zirconium oxide nanowires as high-dielectric-constant gate dielectrics. *Adv. Mater.* **22**, 1941–1945 (2010).

## Acknowledgments

This work was supported by the National Basic Research Program of China (Nos. 2013CB933500, 2012CB932400, 2011CB808400), the Major Research Plan of the National Natural Science Foundation of China (No. 91233110), the National Natural Science Foundation of China (Nos. 51172151, 51173124), the Natural Science Foundation of Jiangsu Province (BK20131162) and a Project Funded by the Priority Academic Program Development of Jiangsu Higher Education Institutions.

## Author contributions

W.D., J.S.J., X.J.Z. wrote the manuscript. J.S.J., X.H.Z. and X.J.Z. were responsible for the overall experimental design. W.D. and H.H.P. conducted the experiments, J.C.W., Q.X.S., and X.W.Z. measured the devices. All authors reviewed the manuscript.

## Additional information

**Supplementary information** accompanies this paper at http://www.nature.com/scientificreports

**Competing financial interests:** The authors declare no competing financial interests.

**How to cite this article:** Deng, W. *et al.* A High-yield Two-step Transfer Printing Method for Large-scale Fabrication of Organic Single-crystal Devices on Arbitrary Substrates. *Sci. Rep.* **4**, 5358; DOI:10.1038/srep05358 (2014).