Novel Nanotube Multiquantum Dot Devices

R. Tormo-Queralt,[¶] C. B. Møller,[¶] D. A. Czaplewski, G. Gruber, M. Cagetti, S. Forstner, N. Urgell-Ollé, J. A. Sanchez-Naranjo, C. Samanta, C. S. Miller, and A. Bachtold*

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ABSTRACT: Addressable quantum states well isolated from the environment are of considerable interest for quantum information science and technology. Carbon nanotubes are an appealing system, since a perfect crystal can be grown without any missing atoms and its cylindrical structure prevents ill-defined atomic arrangement at the surface. Here, we develop a reliable process to fabricate compact multielectrode circuits that can sustain the harsh conditions of the nanotube growth. Nanotubes are suspended over multiple gate electrodes, which are themselves structured over narrow dielectric ridges to reduce the effect of the charge fluctuators of the substrate. We measure high-quality double- and triple-quantum dot charge stability diagrams. Transport measurements through the triple-quantum dot indicate long-range tunneling of single electrons between the left and right quantum dots. This work paves the way to the realization of a new generation of condensed-matter devices in an ultraclean environment, including spin qubits, mechanical qubits, and quantum simulators.
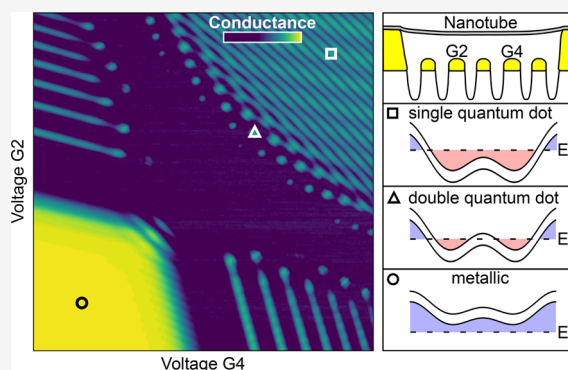
Carbon nanotubes are an excellent platform to study a wide range of quantum phenomena.[1] Many-body and quantum interference effects are observed in two-terminal devices, including Coulomb blockade,[2,3] Kondo physics,[4−9] Wigner states,[10−13] and Fabry-Pérot oscillations.[14−18] More advanced device layouts can be devised to produce double-quantum dot devices[19−23] and spin qubits.[24−27] Nanotubes can be integrated into superconducting impedance-matching circuits.[28] The electronic states of a nanotube can also be coupled to the photons of superconducting resonators[29,30] and the mechanical vibrations of the nanotube itself.[31−40]

The study of these phenomena has been possible thanks to the production of high-quality nanotube devices. These devices are highly sensitive to contamination adsorbed on the nanotube surface as well as charged impurities in the substrate. These are detrimental since they can scatter conducting electrons, modulate the electrostatic potential along the nanotube, and behave as charge fluctuators. One strategy to minimize these issues is to fabricate devices where nanotubes are mechanically transferred onto chips with prepatterned electrodes and trenches,[22,41,42] so that the nanotube surface is not contaminated by etchants and solvents used during the device fabrication. Moreover, nanotubes suspended over trenches are not in contact with the substrate that contains charge impurities. This transfer method also enables integrating nanotubes in circuits containing multiple gate electrodes,[22,26] superconducting cavities,[29,30] and impedance-matching elements.[28] A second strategy consists in directly

growing nanotubes on chips with prepatterned electrodes and trenches.[43] This method can result in lower contact resistances between the nanotube and the electrodes. However, this fabrication method could only produce devices with rudimentary layouts, which contain at best one metallic gate electrode, since more advanced prepatterned structures could not endure the harsh conditions during the nanotube growth at a temperature of about 900 °C.

Here, we report on a reliable method to fabricate carbon nanotube devices with a large number of gate electrodes that withstand the nanotube growth conditions. The gate electrodes consist of Pt nanowires on top of nanoridges made of SiO_2. This structure is obtained by dry etching SiO_2 with the Pt nanowires as a mask. While narrow Pt wires on a planar surface get deformed at high temperature, we found that the SiO_2 nanoridges prevent electrical shorts between neighbor gate electrodes. This layout also enables us to reduce the effect of charge impurities in the SiO_2 layer on the electrons in the nanotube, since the charge impurities are further away from the nanotube and the associated electric field gets screened by
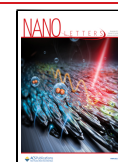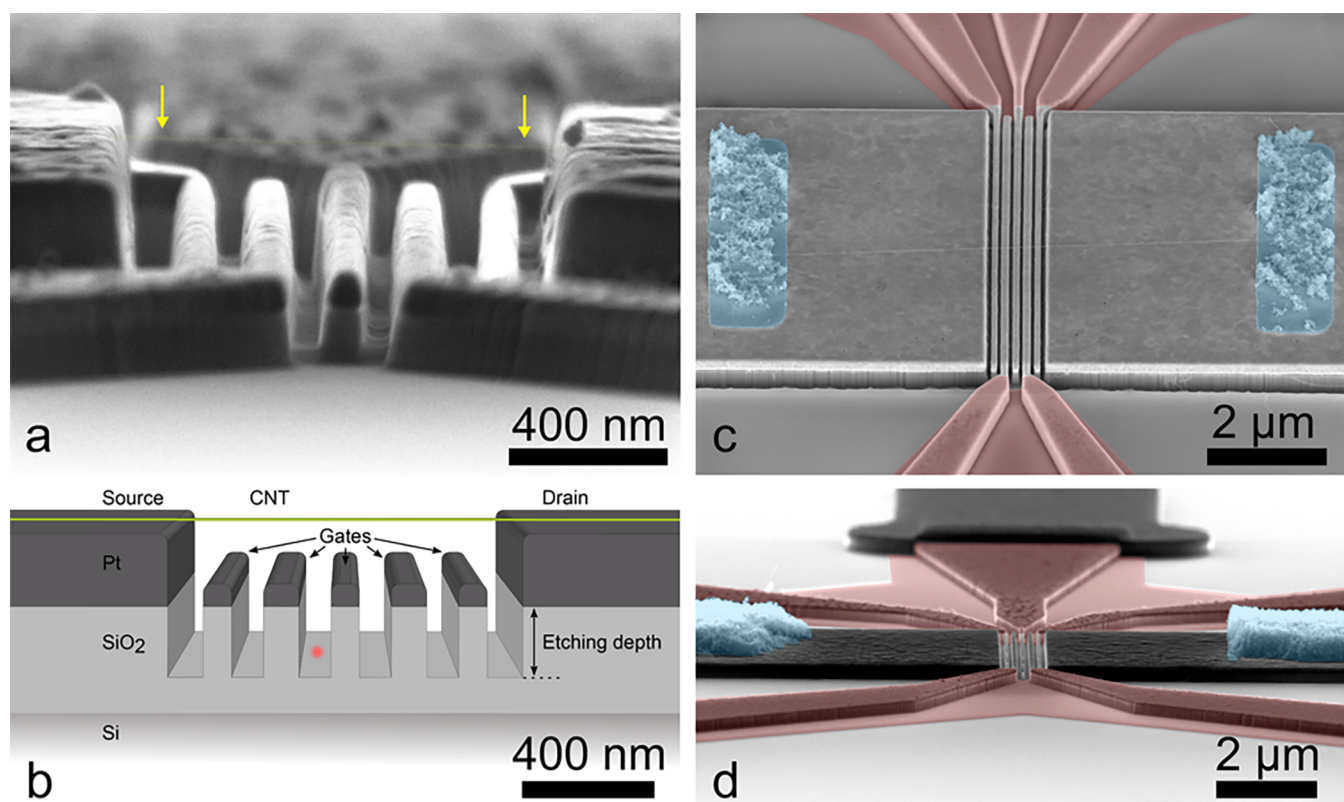
Figure 1. (a) Scanning electron microscope (SEM) image of one of our devices with a carbon nanotube (highlighted by an overlaid yellow line and indicated by two yellow arrows) suspended over five gate electrodes (tilt angle 88° with respect to the chip surface). The nanotube is electrically connected to the source and drain electrodes. (b) 3D schematic representing the device layout. This layout is used to study the impact of a point charge (red dot) on the electrostatic potential along the suspended nanotube (shown in yellow). (c) SEM image of a second device (tilt angle 20°). The rectangular catalyst islands are patterned on both the source and drain electrodes and are highlighted in blue. The SiO_2 layers covering the gates outside the area of interest are painted in red. (d) SEM image of a third device (tilt angle 83°).

the Pt nanowires. We produce nanotube devices with five gate electrodes to electrostatically define multiquantum dots along suspended nanotubes. Charge stability diagram measurements of both double- and triple-quantum dots indicate that the nanotube devices are of high quality.

We fabricate multigate devices with on-chip-grown carbon nanotubes. These devices consist of a nanotube connecting two contact electrodes (source and drain) while being suspended over five gate electrodes (see Figures 1a,b). The nanotubes are grown directly on chips prepatterned with electrodes and trenches using a Fe/Mo catalyst and chemical vapor deposition (CVD) at 900 °C in an $Ar/H_2/CH_4$ atmosphere. The catalyst is patterned into rectangular islands on the source/drain electrodes, see blue shaded regions in Figures 1c,d. The Si substrate is highly resistive (>10 kΩ·cm) and covered by a 300 nm thick thermally grown SiO_2 layer. The electrodes are patterned in multiple electron-beam lithography steps for a better alignment of the gates and a cleaner lift-off process. The gate electrodes are structured using e-beam evaporation with 5 nm of Ti and 60 nm of Pt, while the source and drain electrodes are thicker as they consist of 5 nm of Ti and 150 nm of Pt. Pt is chosen because it can withstand the high temperature CVD step without melting. The detailed fabrication process is described in Section 1 of the Supporting Information.

A crucial step in the fabrication is the dry-etching of the SiO_2 between the gate electrodes. Once all the Pt electrodes are defined, they are used as a hardmask for the reactive ion

etching of the SiO_2 layer by ca. 150 nm. As a result, the gate electrodes are defined on top of abrupt SiO_2 ridges (see Figures 1a and 2a,b). This increases the device fabrication yield
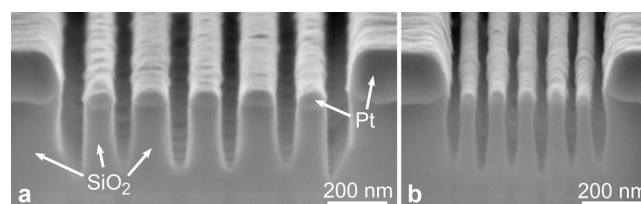

Figure 2. Cross section image of two devices after the nanotube growth with a standard-width trench in (a) and an ultranarrow trench in (b). The devices are prepared using Ga focused-ion beam etching for the imaging with a scanning electron microscope using a 85° tilt angle.

by a large amount by preventing electrical shorts between neighboring electrodes during the harsh conditions of the CVD growth as well as keeping the narrow gate electrodes continuous. In addition, etching the SiO_2 away from the nanotube is expected to diminish the effects of the charge fluctuators in the SiO_2 on the electron state in the nanotube (see the discussion below).

When growing carbon nanotubes on chips with prepatterned structures, care has to be taken to increase the probability of having one nanotube between the source and drain electrodes while minimizing unwanted nanotubes that create electrical
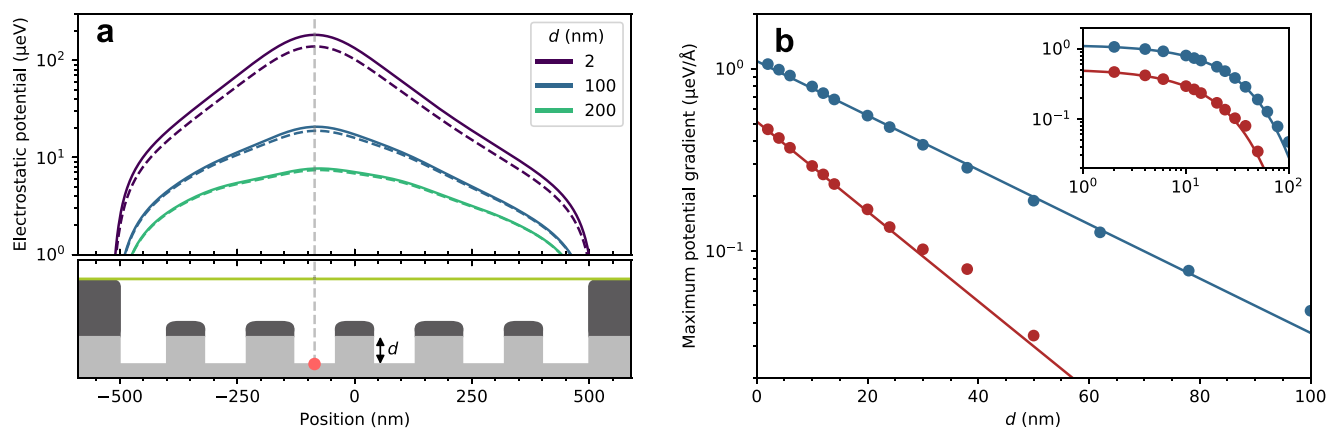
Figure 3. (a) The simulated electrostatic potential along the nanotube created by one electron in the oxide. Solid lines are the potential with the charge on the surface of the SiO$_2$ for various etching depths. Dashed lines show the potential when the charge is moved 10 nm into the SiO$_2$. The schematic of the device cross-section includes the nanotube in yellow, the electron as a red dot, the metal electrodes in dark gray, the SiO$_2$ in gray, and the SiO$_2$ etching depth d. (b) The largest value of the electrostatic potential gradient along the nanotube as a function of the etching depth d. Blue is for the device shown in (a) and red for a device with smaller separation between the gates (see text). The solid lines are fits to exponential decay. Inset shows the data displayed on a log−log scale.

shorts to the gate electrodes. For this, we use two complementary strategies. The first strategy consists in evaporating a SiO$_2$ layer onto the chip covered with an electron beam lithography resist used to pattern the catalyst structures. After the drop casting of the catalyst, we found out that the catalyst remains attached to the SiO$_2$ layer during the lift-off of the lithography resist, which significantly reduces the amount of nanotubes grown from the catalyst deposited in unwanted regions. As for the second strategy, we encapsulate the electrical connections between the gate electrodes and the wire-bonding pads with a SiO$_2$ layer (see red shaded area in Figure 1c,d) to minimize electrical shorts by undesired nanotubes between electrodes.

The fabrication process allows for an extreme miniaturization of the gate electrodes. We have been able to reduce both the gate widths and the gate separations down to 40 and 60 nm, respectively. This allows us to fabricate devices with a source-drain separation as low as 560 nm (see Figure 2b) and a nominal nanotube-to-gate separation of 100 nm. These ultranarrow electrodes survive the extreme conditions of the CVD process without failure. This is verified with a chip, which is exposed to the CVD process at 900 °C with the usual gas flow conditions but without catalyst such that nanotubes are not grown. With a probe station, we measure the electrical resistance between all the 6 neighboring electrode pairs of the 49 devices patterned on the chip. We do not measure any electrical shorts out of the 294 electrode pairs, which is remarkable, especially when considering that the gate electrodes are 7 um long and the gap between them is only 60 nm wide. Scanning electron microscopy inspection of the chip indicates only one discontinuous gate structure, likely due to an electrostatic discharge unrelated to the growth. Therefore, we conclude that electrode failure during CVD is a negligible factor in the device yield, even for the smallest gate separation.

We are able to get on average one high-quality nanotube device in about 1 day of work starting from a diced wafer containing 49 chips with prepatterned electrodes. We define a high-quality nanotube device when the resistance is low and the nanotube is suspended and behaves as a narrow-gap semiconductor. After catalyst deposition and CVD, we select

devices using electrical measurements at room temperature. First, we use a probe station in air to identify devices with a source-drain resistance <200 kΩ and no parasitic shorts to the gates measured with an applied voltage of 100 μV. This corresponds to ca. 2% of the 49 devices per chip. We then use a probe station in vacuum at room temperature to select devices that feature the gate voltage-dependent conductance characteristics of a narrow-gap semiconductor, reach a resistance <150 kΩ at negative gate voltage, and have no measurable shorts to the gates up to an applied voltage ±3 V. All of the above is the case for ca. 16% of the devices previously selected with the probe station in air, which corresponds to about 1 device every 6 chips. These devices are usually suspended, and it is possible to measure their mechanical vibrations in the large majority of the cases. In total, we have characterized 74 chips. The first two devices measured at low temperature are discussed below.

The device layout enables us to reduce the effect of charge fluctuators, which are known to influence and limit device performance.[44−46] Typically, charge fluctuators are associated with defect states in the substrate in the vicinity of the active device area. In our case, the SiO$_2$ between and below the gate electrodes may host a sizable amount of trapping centers.[47,48] These defects are tightly linked to noise and charge trapping phenomena,[49,50] which can limit the performance of double-quantum dot devices.[23,45,46] To assess the impact of charge fluctuators when etching away the SiO$_2$ beneath the nanotube, we carry out finite-element method simulations using COMSOL (see also Supporting Information, Section 2). Using the geometry of the device in Figure 2a, the position-dependent electrostatic potential along the nanotube for an electron at the surface of the SiO$_2$ layer with different etching depths (plain lines) is shown in Figure 3a. The electron is positioned in between two gates as shown by a red dot in the schematic. As the etching depth of the SiO$_2$ is increased, the effect of the electron on the electrostatic potential is reduced primarily due to the increased screening of the electric field by the metallic gate electrodes between the electron and the nanotube. Since charge fluctuators are often associated with electrons moving between two positions, we quantify the
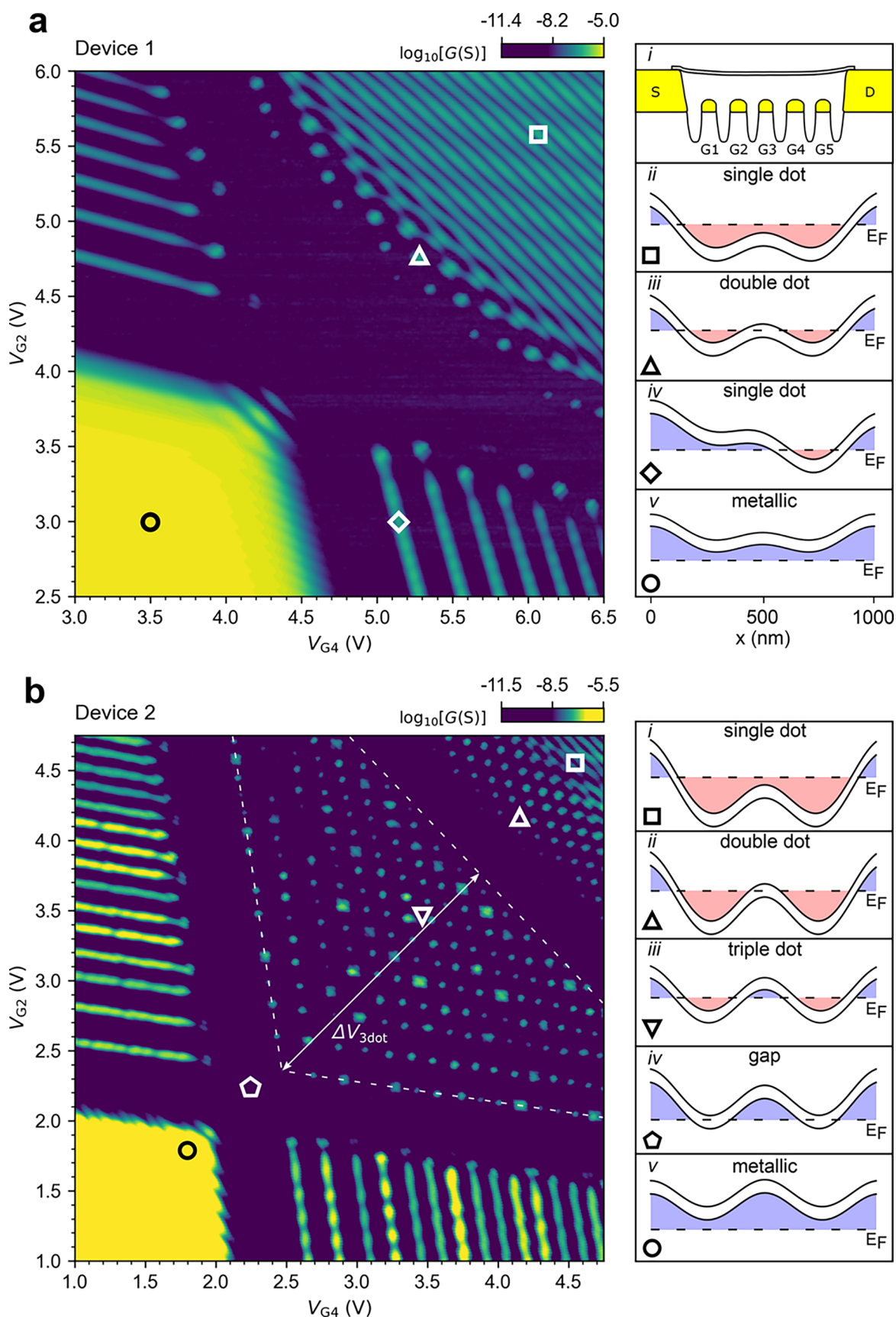
Figure 4. (a,b) Charge stability diagrams measured at 14 K displaying the conductance of two different devices recorded as a function of the gate voltages V_{G2} and V_{G4} applied to gates G2 and G4. The voltages applied to gates G1, G3 and G5 are $V_{G1} = -7$ V (-4 V), $V_{G3} = -3.5$ V (-4 V) and $V_{G5} = -7$ V (-4 V) in panels a and b, respectively. Transport regions of interest are marked by the symbols ◯,□,◇,⬠,△ and ▽. The inset i in panel a shows the schematic of the cross-section of the device. The other insets in panels a and b show the electrostatic potential along the

Figure 4. continued

nanotube at different locations marked in the charge stability diagrams. The dashed white lines in panel b bound the triple-quantum dot region with characteristic size ΔV_{3dot}. The conductance is measured with an applied voltage smaller than $k_B T/e$.

change of the electrostatic potential along the nanotube when a single electron moves by a small amount into the SiO_2 layer (dashed lines in Figure 3a). We compute the largest value of the resulting electrostatic potential gradient along the nanotube and show its value as a function of the SiO_2 etching depth in Figure 3b. The potential gradient is exponentially suppressed as the SiO_2 etching depth is increased. The suppression is larger when the gate electrode separation is shorter; the red curve corresponds to the ultranarrow trench layout in Figure 2b. These simulations indicate that the effect of the charge fluctuators is significantly reduced when etching away the SiO_2 underneath the nanotube. Additional simulations indicate that the effect of charges located elsewhere, and moving in other directions, are also diminished by increasing the etching depth.

We now turn our attention to charge stability diagram measurements revealing the high quality of the nanotube devices. Figure 4a shows the zero-bias conductance of the nanotube as a function of the voltage V_{G2} and V_{G4} applied to the two nominally symmetric gates G2 and G4 sketched in the top inset i. The data presents a high level of symmetry with respect to the diagonal axis going from the bottom left to the top right of the figure. This indicates that the left and right regions of the suspended nanotube have similar electron transport properties. A hypothetical difference in chemical doping along the nanotube or the presence of a strong impurity center would break the symmetry of the measured charge stability diagram. The absence of the 4-fold degeneracy pattern in the modulation of the conductance in electron-doped regions is also observed in devices with single gates[17] when only a few electrons are added in the conduction band. These high-quality measurements have been achieved without any current annealing of the nanotube,[17] since the relatively high contact resistance $R_c \sim 4h/e^2$ prevents the use of this method in an optimal way.

The number of quantum dots along the nanotube can be controlled by V_{G2} and V_{G4}. In the region marked by ◯ in Figure 4a, the conductance remains large around $e^2/4h$ without any sizable modulation, indicating that there is no quantum dot formed along the nanotube. When tuning V_{G4} by a large amount from ◯ to ◇, the nanotube enters a region with the characteristic conduction modulation of a single quantum dot. This indicates that a quantum dot has been formed by two p−n junctions in the suspended nanotube region above the electrode where V_{G4} is applied; the corresponding electrostatic potential modulation along the nanotube is shown in inset iv. When setting V_{G2} and V_{G4} to △ along the symmetric diagonal of the charge stability diagram, the array of conductance peaks observed in this region is consistent with the formation of a double-quantum dot. The electrostatic profile along the nanotube at △ is symmetric with respect to the nanotube center (inset iii); the tunnel barrier between the two quantum dots is created when the Fermi energy lies in the energy gap of the nanotube. In the region indicated by ▢, the regular modulation of the conductance suggests the formation of a single quantum dot that is extended almost over the entire suspended region of the nanotube (inset ii). The electrostatic potential profiles in insets ii-v are obtained from finite-element

method simulations[22] taking into account the device layout imaged by scanning electron microscopy after the measurements. The simulations can qualitatively account for the variation of the number of quantum dots along the nanotube, although the simulations do not consider the shift of the electrochemical potential induced by the Coulomb repulsion when one electron is added in the quantum dot. The simulations can also account for the ≃0.5 V offset between the V_{G2} and V_{G4} ranges in Figure 4a; the offset originates from the angle between the nanotube and the electrodes, so that the nanotube has different capacitive couplings to gates G2 and G4 due to the asymmetric electric field between the nanotube and the two wide electrodes that connect the gates and the contact pads (see Supporting Information Sec. 3). Standard electron transport measurements[51] in the double-quantum dot region point to a large lever arm ($\alpha \simeq 0.25$) as a result of the short separation between the nanotube and the gate electrodes. This is crucial for strong coupling between the double-quantum dot and a superconducting resonator in future measurements.[52−54]

A triple-quantum dot is realized in a second device by applying large negative voltages to gates G1, G3, and G5. The region indicated by the white dashed lines in Figure 4b is assigned to a triple-quantum dot region (inset iii), since it is bounded by two low-conductance transport gaps (⬠ and △) along the symmetry diagonal axis of the charge stability diagram. The transport gap indicated by ⬠ corresponds to the intersection of the quasi-vertical and the quasi-horizontal transport gap strips. At this point the Fermi energy is in the band gap in both nanotube segments above gates G2 and G4, where there are minima of the electrostatic potential (inset iv). The transport gap near △ corresponds to the situation where the Fermi energy is in the band gap at the center of the nanotube, where there is a local maximum of the electrostatic potential (inset ii). Here, the transport gap strip is perpendicular to the symmetry diagonal of the charge stability diagram, since the center of the nanotube hosting the local band gap maximum is capacitively coupled to gates G2 and G4 by the same amount. Furthermore, we observe that the triple-quantum dot region can be eliminated when reducing the electrostatic potential at the center of the nanotube by sweeping the central gate voltage V_{G3}. Figure 5a shows how the size of the triple-quantum dot region quantified by ΔV_{3dot} in Figure 4b gradually decreases to zero when varying V_{G3}. The triple-quantum dot region disappears when the difference ΔE_{3dot} between the valence band along the nanotube segment above gate G3 and the conduction band along the segments above gates G2 and G4 approaches zero; see the inset of Figure 5a. All these experimental facts point to a well-defined triple-quantum dot formed by electrostatic means.

In the triple-quantum dot region, we find a regular array of conductance peaks (▽ in Figure 4b). The conductance peaks are situated at the intersection between the conductance lines of the single-quantum dot formed on the right side of the nanotube at low V_{G2} and that of the single-quantum dot formed on the left side at low V_{G4}. This indicates that the conductance peak array in ▽ emerges when the potential of the right dot is aligned with the potential of the left dot. Electron transport in a triple-quantum dot is usually observed
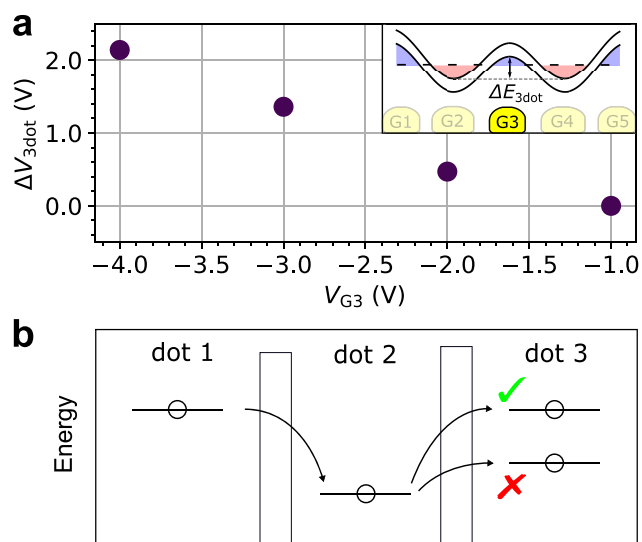
Figure 5. (a) Size of the triple-quantum dot region quantified by ΔV_{3dot} as a function of the voltage V_{G3} applied to the central gate. We extract ΔV_{3dot} from plots similar to the one shown in Figure 4b. The triple-quantum dot region gets fully suppressed for $V_{G3} > -1$ V. The voltages applied to gates G1 and G5 are $V_{G1} = V_{G5} = -4$ V. Inset: the electrostatic potential along the nanotube. To a first approximation ΔV_{3dot} is linearly proportional to the electrostatic potential difference ΔE_{3dot}. (b) Sketch of the cotunneling process through a triple quantum dot showing an allowed (green tick) and a forbidden (red cross) electron transition.

when the potential of the three dots are aligned,[55,56] but this is unlikely to occur for the majority of the observed peaks in the array, since sweeping V_{G2} and V_{G4} also shifts the potential of the central dot due to cross-capacitance. A possible explanation for the observation of the conductance peak array might be related to an exceptionally large broadening of the energy level of the central dot reaching values close to the charging energy. The broadening could, for instance, arise from strong charge fluctuators, large electrical fluctuations on the gate electrodes, or the coupling to the mechanical vibrations of the suspended nanotube. However, the same broadening would then be expected when one single-quantum dot is formed in the nanotube. This is not the case, indicating that the transport through the triple-quantum dot does not originate from the broadening. We attribute the measured conductance array to a virtual process leading to a long-range tunneling of single electrons between the left and the right quantum dots, while the center dot is not necessarily in resonance with the two other dots.[57] It is an elastic cotunneling mechanism in which an electron in the left dot tunnels into the right dot via virtual events (see Figure 5b). This process only takes place when the potential levels of the left and right quantum dots are aligned as observed in our measurements.

Looking ahead, our fabrication process offers the prospect to produce a new generation of nanotube devices in an ultraclean environment. Growing nanotubes directly over prepatterned electrodes enables lowering the two-terminal resistance at helium temperature below $\sim 2h/e^2$, which we will achieve by measuring more devices in a dilution cryostat. This will be key to produce nanotubes with essentially no surface contamination as recently demonstrated in ref 17., where the contamination molecules adsorbed during the manipulation

of the device in air are removed with the current annealing method. This method[58−60] consists of applying a large current through the nanotube in a dilution cryostat at base temperature. The removal of the contamination can be revealed by regular quantum electron interference measurements, which are particularly sensitive to disorder;[17] the contamination-free surface is also supported by the fact that it is possible to deposit single layers of helium atoms with the expected density.[61] Our fabrication process also enables suspending nanotubes away from the charge fluctuators in the substrate. In such an ultraclean environment, nanotube double-quantum dots may produce charge qubits[23] and spin qubits[24−27] endowed with long coherence times.[62−64] By coupling the double-quantum dot to the mechanical vibrations of the nanotube, it might be possible to build a completely new qubit where the information is stored in the mechanical vibrations. Such a mechanical qubit might feature a sub-kHz decoherence rate, since it inherits the long coherence time of the mechanical vibrations.[65] More advanced devices that contain four quantum dots might be used as analogue quantum simulators that can emulate the electron−phonon interaction in small-size quantum materials.[66,67] Several states are expected to emerge from the competition between the electron−phonon interaction and the electron−electron repulsion. These include charge density waves, Mott insulators, and states with electron−electron pairing induced by vibrations.

■ ASSOCIATED CONTENT

ⓢ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c03034.

Further information regarding the fabrication process, the COMSOL simulations, Device 1, and the electrode dimensions of all devices discussed (PDF)

■ AUTHOR INFORMATION

Corresponding Author

A. Bachtold − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain;* ⓞ orcid.org/0000-0002-6145-2479; Email: adrian.bachtold@icfo.eu

Authors

R. Tormo-Queralt − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

C. B. Møller − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

D. A. Czaplewski − *Center for Nanoscale Materials, Argonne National Laboratory, Argonne, Illinois 60439, United States;* ⓞ orcid.org/0000-0003-2262-0908

G. Gruber − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

M. Cagetti − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

S. Forstner − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

N. Urgell-Ollé − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

J. A. Sanchez-Naranjo − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

C. Samanta − *ICFO - Institut De Ciencies Fotoniques, The Barcelona Institute of Science and Technology, 08860 Castelldefels, Barcelona, Spain*

C. S. Miller − *Center for Nanoscale Materials, Argonne National Laboratory, Argonne, Illinois 60439, United States*

Complete contact information is available at:
https://pubs.acs.org/10.1021/acs.nanolett.2c03034

Author Contributions

[¶](R.T.-Q., C.B.M.) These authors contributed equally to the work.

Notes

The authors declare no competing financial interest.

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