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Hysteresis in Lanthanide Zirconium Oxides Observed Using a Pulse CV Technique and including the Effect of High Temperature Annealing

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Abstract: A powerful characterization technique, pulse capacitance-voltage (CV) technique, was used to investigate oxide traps before and after annealing for lanthanide zirconium oxide thin films deposited on n-type Si (111) substrates at 300 °C by liquid injection Atomic Layer Deposition (ALD). The results indicated that: (1) more traps were observed compared to the conventional capacitance-voltage characterization method in $LaZrO_x$; (2) the time-dependent trapping/de-trapping was influenced by the edge time, width and peak-to-peak voltage of a gate voltage pulse. Post deposition annealing was performed at 700 °C, 800 °C and 900 °C in N_2 ambient for 15 s to the samples with 200 ALD cycles. The effect of the high temperature annealing on oxide traps and leakage current were subsequently explored. It showed that more traps were generated after annealing with the trap density increasing from 1.41×10^{12} cm^{-2} for as-deposited sample to 4.55×10^{12} cm^{-2} for the 800 °C annealed one. In addition, the leakage current density increase from about 10^{-6} A/cm^2 at $V_g = +0.5$ V for the as-deposited sample to 10^{-3} A/cm^2 at $V_g = +0.5$ V for the 900 °C annealed one.

1. Introduction

With the continuous scaling down Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), SiO_2 based devices have reached their physical limitations. When the thickness of the SiO_2 gate dielectric is below 1.4 nm, the electron tunneling effects and leakage current become serious obstacles for the device reliability [1]. To further decrease the size of devices, high-*k* materials (dielectric constant larger than that of SiO_2, 3.9) have been employed to replace the SiO_2 gate dielectrics. For example, In MOSFET technology, SiO_2 was replaced by a hafnium-based high-*k* material in 2007 [2]. With the introduction of high-*k,* the equivalent oxide thickness (EOT) becomes smaller with thick physical thickness compared to SiO_2 gate dielectric [3]. The small EOT is desired to scale down the size of devices and the large physical thickness ensures the small leakage current. As Nadimi reported, the leakage current density for hafnium oxide and silicon oxide decreased 0.31 decade/Å and 0.49 decade/Å, respectively, with the increase of oxide thickness [4]. The gate dielectrics with small EOT can be obtained without the expense of an increase of the device leakage current by the employment of high-*k* material. The leakage current is one of the most significant issues related to device reliability [5–9]. Therefore, a number of high-*k* materials, HfO_2, ZrO_2, Y_2O_3 and their silicates, have been widely studied due to their high dielectric constants [10,11]. However, for zirconia, it exhibits a wide range of phases with various dielectric constants in theory ranging from 16 for the monoclinic phase to 47 for the metastable tetragonal phase [12]. Other research showed that the metastable tetragonal and cubic phases of ZrO_2, with higher *k*-values, were stabilized by addition of small amounts of rare earth elements (such as La, Gd, Dy, Er, *etc.*) [13–17]. Therefore, lightly lanthanum doped zirconium oxide is considered to be a potential candidate to further reduce the EOT to scale the transistor size and has attracted a great amount of attention from both industrial and academic researchers [18–20].

With regard to the electrical characterization of the material, a number of methods have been proposed to investigate the reliability, degradation, device lifetime, defect loss, electron trapping and de-trapping, interface states *etc.* [21–25]. One of the more recent methods, termed the pulse capacitance-voltage (CV) technique, is able to complete the film characterization in several hundreds of micro-s. The detailed working principles and mechanism have already been discussed in our previous research outputs [3]. Using this powerful method, more traps were extracted compared with conventional methods, e.g., measured by Agilent 4284A LCR meter. This was attributed to the fast characterization of the pulse CV technique and less de-trapping process occurred before accomplishment of the measurement. As a result, more traps were measured. For the time-dependent trapping/de-trapping, the traps were traced by changing the edge time, width and peak-to-peak voltage of a gate voltage pulse [3].

In this work, MOS capacitors with $LaZrO_x$ deposited by Atomic Layer Deposition (ALD) as gate dielectric were fabricated and rapid thermal annealing (RTA) at different temperatures was performed. X-Ray diffraction (XRD) was used to investigate the physical properties of each sample. The pulse CV technique was employed to investigate the oxide traps and trace the time-dependent trapping/de-trapping,

and the results of the pulse CV technique and the conventional test method were compared. The focus of the present work is, therefore, on exploring the CV hysteresis of the oxides and the effect of high temperature annealing. An interesting correlation between annealing temperature and oxide traps, which provides a reference for the properties of the high-*k* thin films, will be discussed in the paper.

2. Results and Discussion

Figure 1a shows the input signal and the output signal of the pulse CV technique [3]. The CV characteristics shown in Figure 1b are extracted from the results in Figure 1a and delta V_g is denoted in Figure 1b as well. The structure of the tested sample was shown in the inset of Figure 1a. From the observation of Figure 1b, there was a shoulder between −0.8 and −0.4 V. The shoulder was attributed to interface states that respond at lower frequencies and may originate from the La and Zr diffusion and mixing with the SiO_2 interlayer during deposition [13,26].
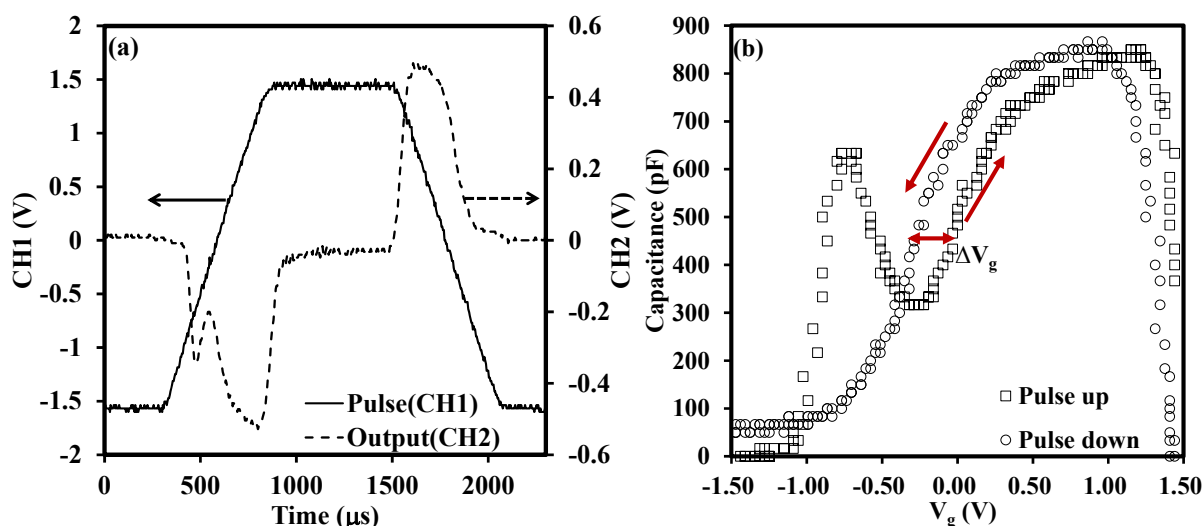

Figure 1. (**a**) Input, Channel 1 (CH1), and output, Channel 2 (CH2), signal for the pulse CV technique [3]; (**b**) CV characteristics of pulse up and pulse down extracted from (**a**). In Figure 1a, we used a functional/arbitrary waveform generator to input a pulse voltage waveform (CH1) on the gate of the sample. The related current through the sample (i_{total}) was fed into a current amplifier and then was amplified as an output voltage signal (CH2). Both channels of an oscilloscope were used to track the input and output voltages. Delta V_g denoted in Figure 1b represent the gate voltage shift between pulse up and pulse down. The thickness of the sample under test was about 22 nm.

Figure 2 illustrates the conventional CV characteristics measured by the Agilent 4284A (Agilent, Santa Clara, CA, USA). From the comparison of Figure 1b and Figure 2, it is clear that there is an obvious hysteresis between the CV curves (ramp up and ramp down) measured by the pulse technique while there is almost no hysteresis in the conventional test. The large hysteresis is revealed by rapid characterization provided by the pulse CV technique, (in the order of several hundred micros), and the traps are not recovered completely before the end of the measurement. The pulse CV technique tracks the trap density in the oxide more accurately, or in other words, the conventional test underestimates the

trap density in the oxide. The verification of the influence of test time on change of delta V_g will be fully discussed later. We firstly give a possible explanation for the horizontal shift of the CV curves measured by the pulse technique. The shift of the curves is attributed to charge trapping/detrapping in oxide [25,27]. In our case, the charges existing in the oxide probably belong to as-grown fixed positive charges (oxygen vacancies) with high energy levels or probably are trapped in as-grow electron traps in the high-*k* oxide. When the gate is applied with a positive bias voltage ($V_g > 0$), electrons are de-trapped from the as-grown electron traps to the metal gate through tunneling and the net positive charges in the oxide lead to the CV curves shifting negatively. Similarly, if a negative voltage ($V_g < 0$) is applied on the metal side, the as-grown positive charges will be compensated by electrons from the metal gate and trapped in the as-grown electron traps. Thus, the negative charges shift the measured CV curves in the positive direction [28–31].
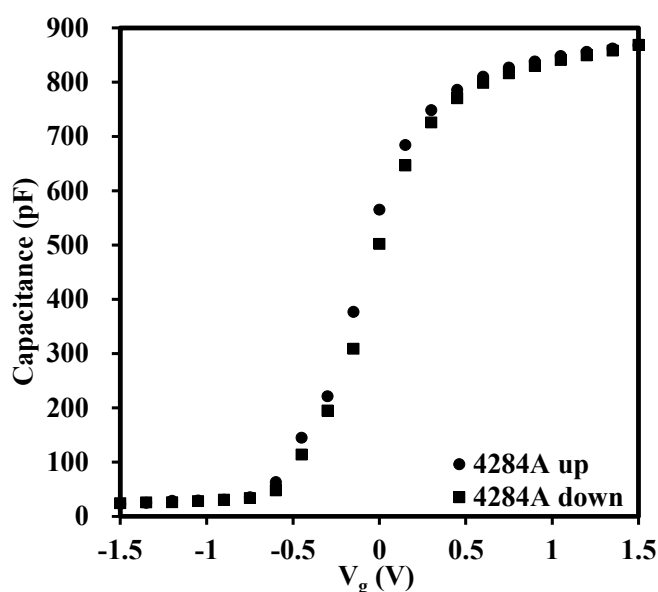

Figure 2. Conventional CV characteristics measured by Agilent 4284A for the sample with the thickness of about 22 nm. It is clear that there is an obvious hysteresis between the CV curves measured by the pulse technique while there is almost no hysteresis for the conventional test.

With regard to the test time, the edge time indicated in the inset of Figure 3a, it is critical for the characterization of traps in the oxide and we will discuss it in detail in conjunction with the experiment results shown in Figure 3a,b in this section. During the measurement, the rising edge gave an initial measurement before any stress was applied. Then, the falling slope of the pulse applied to the gate provided another measurement post stress. The stress was provided and determined by the width of the pulse. If the width of a pulse induced charge trapping in oxides, there would be a hysteresis between the ramp up and ramp down of the CV curves as described in Figure 1b. In addition, the change of the edge time leads to the change of the test time. Longer edge time means more test time at each voltage bias. When the edge time was increased to a relatively large value, or relative long test time (several s), the pulse CV technique may be considered to be the same as the conventional CV test technique carried out using a LCR meter, (the Agilent 4284A in our case). This hypothesis was consistent with the results shown in Figure 3a,b. In Figure 3a, it is obvious that the extracted trap density, N_{ot}, was reduced from 2.48×10^{12} cm^{-2} with edge time of 300 μs to 0.7×10^{12} cm^{-2} with edge time of 900 μs.

The N_{ot} was calculated from the formula, $N_{ot} = \Delta V_g \times C_{ox}/q$, assuming these traps were located at the silicon and oxide interface.
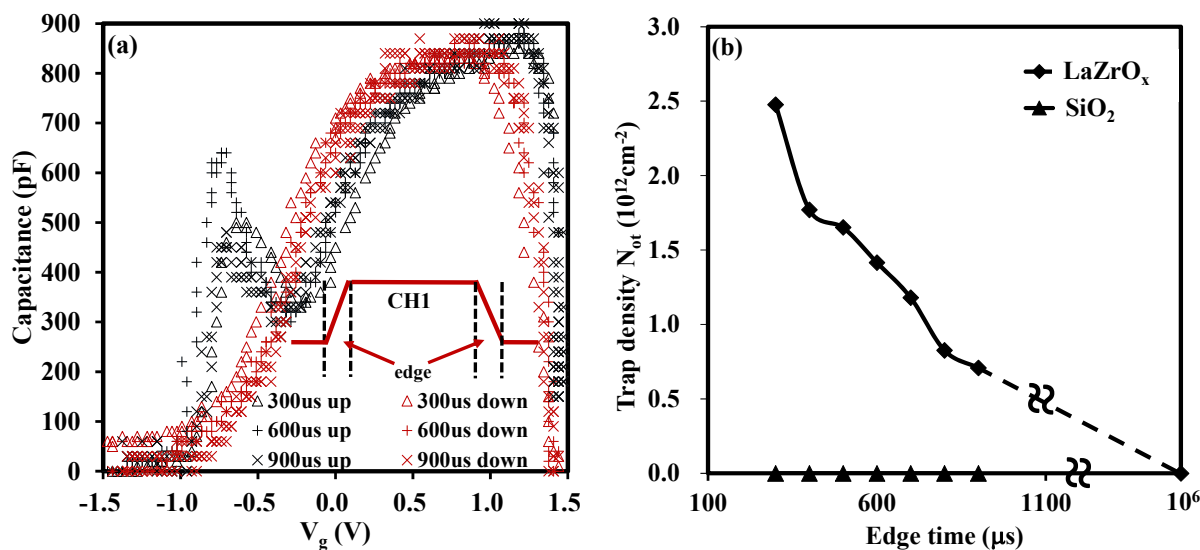

Figure 3. (**a**) Capacitance *versus* gate voltage with various edge time for LaZrO$_x$ (thickness of the stack about 22 nm); (**b**) Variation of N_{ot} *versus* edge time for LaZrO$_x$ and SiO$_2$. The large edge time means long test time in the measurement and the N_{ot} observed will decrease with the increase of test time.

The above analysis implies that the trapped electrons/holes were recovered with an increase of the measurement time, in turn, leading to the partial reduction of trapped charges. Figure 3b graphically summarizes the relationship between trap density and edge time of a high-*k* material (LaZrO$_x$) and a silicon dioxide. For the silicon dioxide gate dielectric, it has been shown that there are no as-grown electron traps in the oxide and no hysteresis is observed whatever the edge time is [3]. Thus, the silicon dioxide sample was used as a reference in this experiment. By adjusting the edge time, the time-dependent trapping/de-trapping was tracked correspondingly. For the high-*k* material in this research, N_{ot} was reduced with an increase of the edge time as shown in Figure 3b. Due to the limitations of the function generator (RIGOL DG2041A), the longest edge time used was 900 micro s. However, from the trend of N_{ot}, it can be estimated that if the edge time was long enough, say, one second, the trap density measured by pulse CV technique would be equal to that of the conventional CV test as shown in Figure 2. The dashed line in Figure 3b indicates the behaviour of N_{ot} with edge time. It can also be concluded that the recovery of trapped electrons/holes are sensitive to the measurement time from the change of N_{ot} with variation of test time. To be precise, the short test will give the large N_{ot}. Therefore, the time-dependent trapping/de-trapping should be probed by short edge time in the pulse CV measurement, which is able to access shallower traps (traps at a high energy levels within oxide), at least for the timescale considered here. While for the longer values of edge time, the transient shift of the N_{ot} is attributed to slow electron trapping/de-trapping [3].

After the examination of the edge time, the research focused on the influence of the stress time, or the width of a pulse, on trap density. The stress time (pulse width) is indicated in the inset of Figure 4. Figure 4 shows that charges trapped in the oxide were highly dependent on the stress time with N_{ot} of

4.14×10^{12} cm^{-2}, 3.17×10^{12} cm^{-2}, 2.48×10^{12} cm^{-2} for stress time of 4500 μs, 2500 μs and 800 μs, respectively, at an initial state (edge time of 300 μs). It may be that the longer width, or stress time, the larger the electron fluency supplying the charge into traps in the oxide, this in turn, leads to more trapped charges. Also, the figure indicates that the recovery of N_{ot} with the edge time for the three curves shares similar trends regardless of the initial charges trapped in the oxide. This result also indicates that the de-trapping process is highly dependent on the test time.
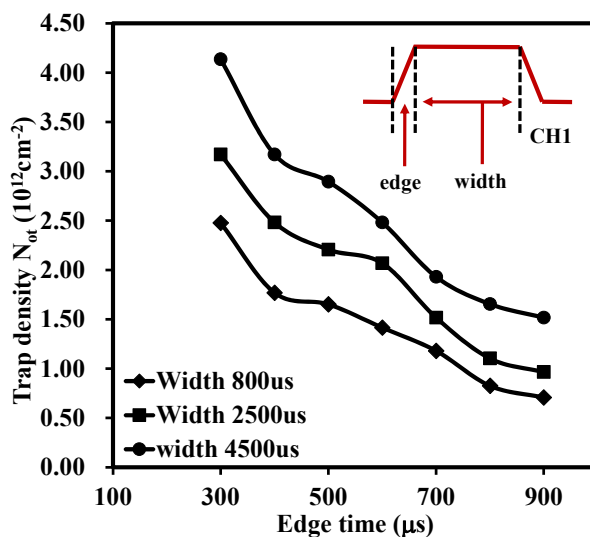

Figure 4. Variation of N_{ot} *versus* edge time with different stress time (the pulse width) for LaZrO$_x$. The length of stress time is controlled by the width of the pulse. The longer stress time can induce more traps in the oxide, in turn, the increase of N_{ot}. The thickness of the device under test was about 22 nm.

Finally, the pulses with various V_{PP} were applied to the gate of the MOS capacitors to investigate the effect of V_{PP} on charge trapping. The pulses used in the experiment did not have any voltage offset. In other words, if V_{PP} was 4 V, then the pulse started from −2 V and ended with 2 V. Figure 5 concludes the relationship between extracted trap density and edge time under different V_{PP}. It shows that for larger V_{PP} stress (4 V), the larger N_{ot} (3.58×10^{12} cm^{-2}) was observed because the traps in the deeper/higher energy level in the oxide were also tracked by the higher voltage [3]. Interestingly, for $V_{PP} = 4$ V, the extracted trap density was saturated with small edge time, 400 μs in this case, which meant that all the traps at the corresponding energy level were fully tracked provided that the edge time was below 400 μs at this voltage level.

The traps in the oxide characterized by the pulse technique were discussed above, and it was found that more traps were tracked by the pulse CV characterization method compared with the conventional one (e.g., using an LCR meter with an analogue ramp). Also, the time-dependent trapping/de-trapping was traced by adjusting the edge time, width and peak-to-peak voltage of a voltage pulse. If the edge time (test time) was long enough, the result obtained by the pulse CV technique was the same as the conventional method, which provided a calibration of the new technique. Before the discussion of high temperature annealing effect on the oxides, the dielectric constant of the as-deposited sample was calculated. Firstly, the stack thickness of about 22 nm was measured by ellipsometer. Then, based on the thickness and the size of the electrode contacts, diameter of 0.3 mm, the dielectric constant of the stack

was estimated to be 27 approximately. From our previous work on ALD deposition and other research outputs using water as the oxidizing agent, a thin SiO_x film was formed at the film/Si substrate interface [3,19,32]. It is likely that the overall dielectric constant of the stack was limited by the presence of such an interfacial layer.
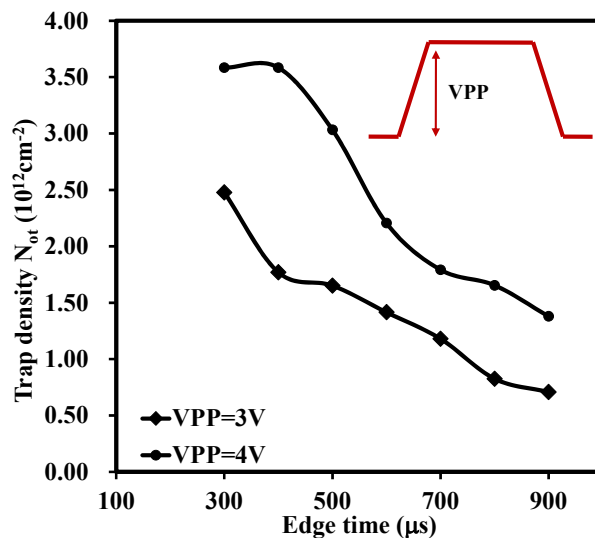

Figure 5. Variation of N_{ot} *versus* edge time with V_{PP} for the sample with thickness of 22 nm. The large voltage applied can track the traps at deeper energy level. When V_{PP} was 4V, the extracted trap density, N_{ot}, was about 3.58×10^{12} cm^{-2}.

The above analysis was based on the as-deposited sample and the annealed ones will be discussed in the following sections. In order to examine the effect of the high-temperature annealing on the oxides, post-deposition annealing was performed at 700 °C, 800 °C and 900 °C in N_2 ambient for 15 s. The CV characteristics for the annealed samples are presented in Figures 6 and 7 in order to illustrate the horizontal shift and vertical change of the CV curves, respectively. Due to the unacceptable distortion of the CV curves caused by the large leakage current for the sample annealed at 900 °C, only CV curves from the as-deposited, 700 °C annealed and 800 °C annealed samples are presented in Figure 6. The delta V_g is indicated in each curve as well. From the delta V_g of the curves in Figure 6a–c, it was obvious that the RTA led to the increase of trap density, from 1.41×10^{12} to 4.55×10^{12} cm^{-2}. The increase of trap density was probably caused by the increase of oxide trap, interface state and border trap density. Other researchers also found similar results, which suggested that as the oxide-trap charge increased after the high temperature annealing, a concomitant increase was also observed in the interface and border-trap densities [33]. From Figure 7, it was discovered that the accumulation capacitance, or CET, of the high-k/IL stacks decreased with the increase of annealing temperature, which was mainly due to the thickness increase of the SiO_x interfacial layer after RTA. This phenomenon also occurred in our previous work which showed that the interfacial layer, SiO_x, was increased after 900 °C annealing attributed to either internal or external oxidation mechanism [34]. In addition, the CV curve was stretched out with annealing temperatures, which indicated the increase of interface states by either silicate formation or diffusion [33,35]. The two figures (Figures 6 and 7) indicated that annealing conditions should be controlled carefully, otherwise some disadvantages, such as the increase of the oxide traps, interface state and of the IL thickness, can be caused after annealing.
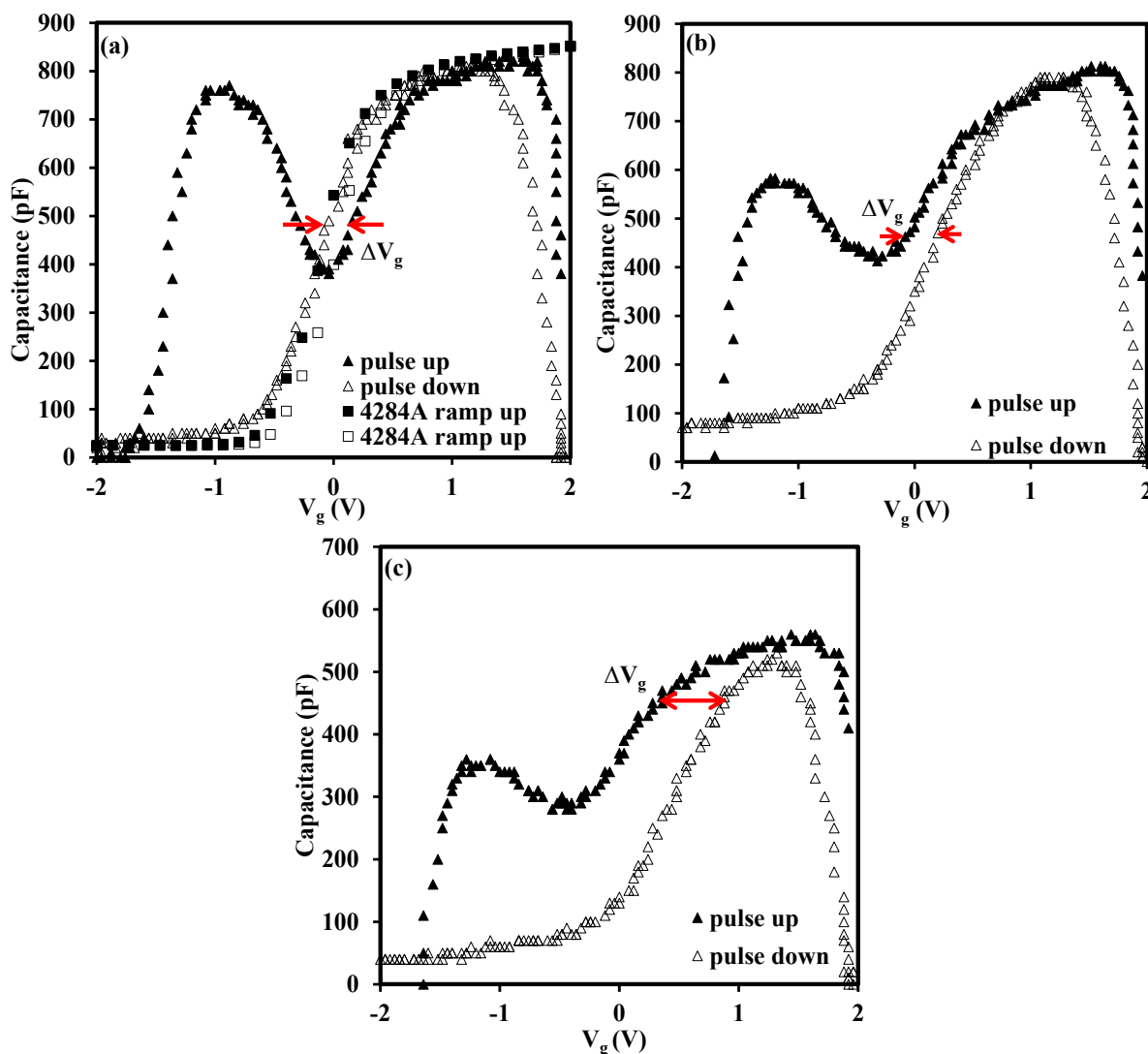
Figure 6. The influence of RTA on trap density (extracted from V_g indicated in each figure) for the CV characteristics measured by pulse CV technique with the annealing condition for (**a**) as-deposited (**b**) 700 °C (**c**) 800 °C. The thickness of the sample under test before annealing was about 22 nm. The conventional CV curves measured by the Agilent 4284A LCR meter are also shown in Figure 6a (square symbols) as comparison. The result implies that the delta V_g (or trap density) will increase with the RTA temperature.

Figure 8 provides the XRD diffraction patterns (with normal angle) for the as-deposited, 700 °C annealed, 800 °C annealed and 900 °C annealed samples to determine the morphology of the films. From the observation of the pattern for the as-deposited one, the thin films was poly-crystalized with weak reflections. The planes for diffraction peaks were indexed in the figure. With the increase of the RTA temperature, the diffraction peaks became stronger and shaper. In addition, more noticeable diffraction peaks appeared when the RTA temperature reached 900 °C. Noticeably, for the RTA temperature of 900 °C, a diffraction pattern for $ZrSiO_4$ was observed, implying the diffusion of the elements occurred at the interface and zirconium silicide was formed [36,37]. The behaviour would deteriorate the interface and enhance the increase of leakage current, which was consistent with the result in Figure 9.
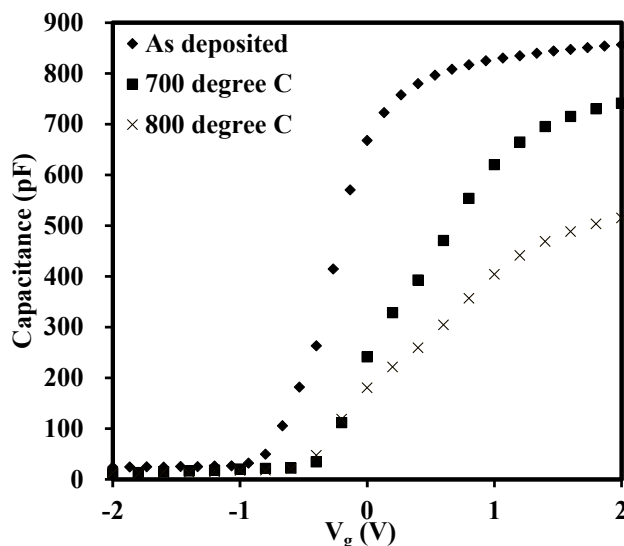
Figure 7. Capacitance *versus* gate voltage for as-deposited sample with thickness of 22 nm and the ones after RTA. The capacitances (dielectric constants) decrease, mainly due to increase of the thickness of the interfacial layer silicon oxide between the high-*k* material and substrate after annealing, with the increase of the annealing temperature.
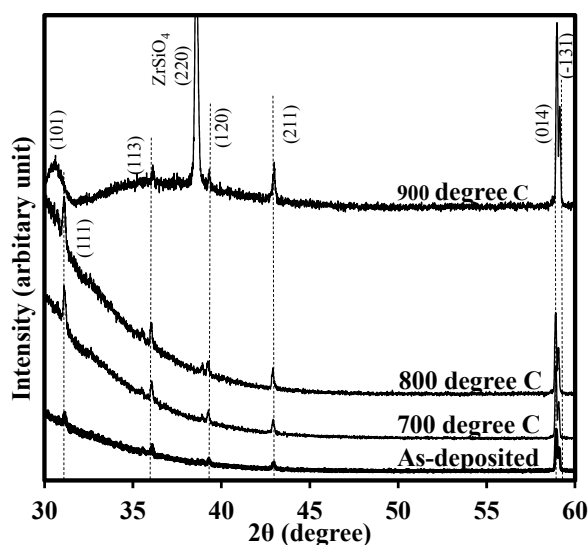

Figure 8. XRD patterns (with normal angle) for the as-deposited, 700 °C, 800 °C and 900 °C annealed samples. The thickness of the device under test was about 22 nm. For the as-deposited one, the thin films was poly-crystalized with weak reflections. When the RTA temperature reached 900 °C, more noticeable diffraction peaks appeared.

Figure 9 illustrates the gate leakage current densities of the samples. The leakage current densities increase dramatically with the annealing temperature as shown in the figure. The leakage current was compared at the point with the bias voltage of 1 V beyond flatband voltage (V_{FB} + 1 V), at the bias voltage of 0.5 V in this experiment. For the 900 °C annealed sample, the leakage current density, with around 10^{-3} A/cm^2 at V_g = +0.5 V, is 1000 times larger than that of the as-deposited one, with about 10^{-6} A/cm^2 at the same bias voltage. This result is consistent with the crystallization of the samples and deterioration of the interface indicated by the XRD patterns.
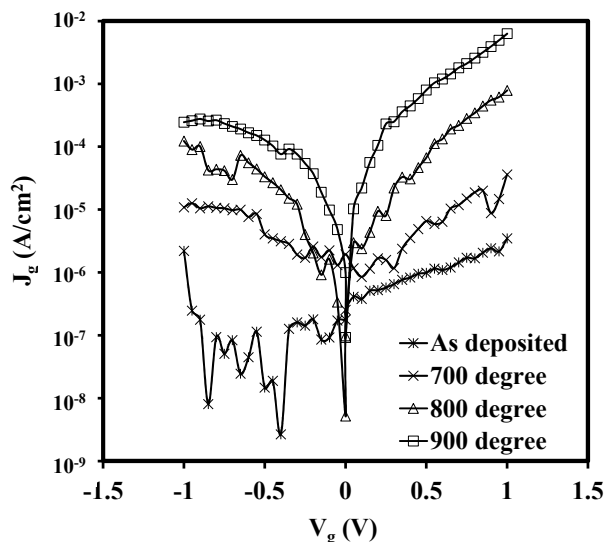
Figure 9. Gate leakage current *versus* gate voltage for the four samples. The thickness of the sample was about 22 nm for the as-deposited one. It is obvious that the leakage current will increase dramatically with the annealing time. The 900 °C annealing one, with 10^{-3} A/cm^2 at V_g = +0.5 V, is 1000 times than that of the as-deposited one.

3. Experimental Section

The n-type Si (111) wafers with resistivity of 1–10 Ω·cm were used as the substrates of MOS capacitors in this experiment. The wafer was cleaned following the standard Radio Corporation of America (RCA) cleaning procedures and dried by N_2 gun. After cleaning, the lanthanide zirconium oxide thin films were deposited by ALD at the substrate temperature of 300 °C using $(C_2H_6N)_4Zr$ and $(C_{11}H_{19}O_2)_3La$ as precursors. The temperatures for zirconium and lanthanum precursors were 130°C and 100 °C, respectively. The 50 °C deionized water (DI water) was served as the oxygen source. For deposition, nine cycles of water (30 ms)/purge (20 s)/$(C_2H_6N)_4Zr$ (1000 ms)/purge (25 s) were followed by one cycle of water (30 ms)/purge (20 s)/$(C_{11}H_{19}O_2)_3La$ (300 ms)/purge (25 s). In other words, the cycle ratio of zirconium oxide to lanthanum oxide was 9:1. The whole sequence was repeated 20 times and the total number of cycles was 200. Pure N_2 was used as both carrier gas and purge gas. After the deposition of gate dielectric, the wafer was sliced into four pieces. For three of them, the rapid thermal annealing (RTA) at 700 °C, 800 °C and 900 °C, respectively, for 15 s was performed in N_2 ambient before the deposition of contact gates. Then, XRD (with normal angle) analysis was carried out using Rigaku miniflex diffractometer (Rigaku, Tokyo, Japan) with Cu$_{K\alpha}$ radiation (0.154051 nm, 40 kV, 50 mA), spanning a 2θ range from 30° to 60° at a scan rate of 1°/min for all samples. The thickness of each thin film was measured by ELLIP-SR-1 ellipsometer with the incident angle of 65°and wavelength from 300 to 850 nm with the step of 10 nm. The aluminum electrode contacts with a diameter of 0.3 mm and thickness of 500 nm were deposited by an E-beam evaporation. The backside was deposited with aluminum as well after the treatment of a diluted HF solution to form ohmic back contact. The fabricated structure of the sample was shown in Figure 10. Aglient 4284A precision LCR meter, Keithley 487 picoammeter and a useful developed pulse CV system [3] were employed to investigate the electrical properties of the samples. All of the electrical measurements were performed in the dark at room temperature with the Faraday Cage surrounding the wafer prober.
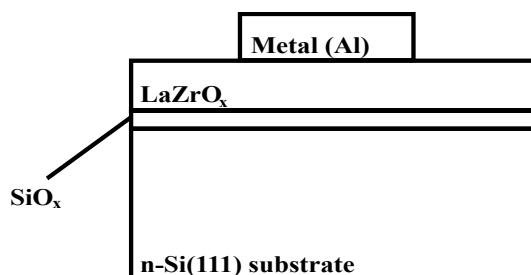
Figure 10. The fabricated structure of the sample tested in the experiment. SiO_x was the native oxide of silicon grown during deposition. The aluminum contacts with a diameter of 0.3 mm and thickness of 500 nm were used as electrode contacts.

4. Conclusions

Lanthanide zirconium oxide thin films were deposited on the n-type Si (111) substrates by Atomic Layer Deposition. Overall, dielectric constants of the stack of 27 were estimated. In order to explore the influence of rapid thermal annealing, post deposition annealing was performed at 700 °C, 800 °C and 900 °C, respectively, in N_2 ambient for 15 s. A useful characterization technique, pulse capacitance-voltage technique, was employed to be a powerful tool to track the traps in the oxides. It was found that the traps in the stack was highly dependent on the edge time, width and peak-to-peak voltage of a gate voltage pulse. The recovery of trapped electrons/holes were sensitive to the measurement time and the short test would give the large trap density. For the width time, the longer width, or stress time, the larger the electron fluency supplying the charge into traps in the oxide, this, in turn, led to more trapped charges. With the higher voltage level, more traps were detected since the traps in the deeper/higher energy level in the oxide were tracked. The influence of the high temperature annealing on the thin films as studied as well. It showed that more traps were generated after annealing with the trap density increasing from 1.41×10^{12} cm^{-2} for as-deposited one to 4.55×10^{12} cm^{-2} for 800 °C annealed one. In addition, the leakage current was also increased. The leakage current density of the 900 °C annealed sample (about 10^{-3} A/cm^2 at $V_g = +0.5$ V was 1000 times larger than that of the as-deposited film (around 10^{-6} A/cm^2 at $V_g = +0.5$ V. The X-ray diffraction was carried to give the comprehensive analysis. The XRD patterns showed that with the increase of the RTA temperature, the diffraction peaks became stronger and shaper. More noticeable diffraction peaks appeared when the RTA temperature reached 900 °C. This behaviour supported the results of the increase of leakage current density.

Acknowledgments

Author Contributions

Qifeng Lu extracted the data and drafted the manuscript. Qifeng Lu and Yifei Mu prepared the samples. Ce Zhou Zhao monitored and led the whole research project. Chun Zhao, Steve Taylor and Paul R. Chalker participated in the discussions. All of the authors read and approved the final manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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