ACS MEASUREMENT SCIENCE Au
AN OPEN ACCESS JOURNAL OF THE AMERICAN CHEMICAL SOCIETY

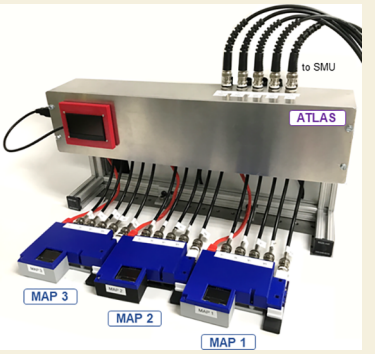
pubs.acs.org/measureau
Article

ATLAS-MAP: An Automated Test Station for Gated Electronic Transport Measurements

Amber Walton, Michael Manno, Paul J. Dauenhauer, C. Daniel Frisbie,* and Daniel McDonald*

Cite This: ACS Meas. Sci. Au 2024, 4, 659–667
Read Online

ABSTRACT: The diversification of electronic materials in devices provides a strong incentive for methods to rapidly correlate device performance with fabrication decisions. In this work, we present a low-cost automated test station for gated electronic transport measurements of field-effect transistors. Utilizing open-source PyMeasure libraries for transparent instrument control, the "ATLAS-MAP" system serves as a customizable interface between sourcemeters and samples under test and is programmed to conduct transfer curve and van der Pauw methods with static and sweeping gate voltages. Zinc oxide transistors of variable thickness (5, 10, and 20 nm) and channel size (50 μm to 3 mm, of equal length and width) were fabricated to validate the design. Standardization of testing procedures and raw data formatting enabled automated data analysis. A detailed list of parts and code files for the system are provided.



KEYWORDS: *automation, PCB, microcontroller, transistor, transfer curve, van der Pauw*

INTRODUCTION

The proliferation of electronics in daily life has created unprecedented motivation for semiconductor fabrication and research. With a global revenue of $599.6 billion in 2022,[1] the semiconductor industry has incentivized the development of new fabrication methods to achieve targeted device architectures and performance, leading to a large and complex set of design variables.[2,3] The ability to tune the fabrication of electronic materials has grown with the diversification of deposition techniques, such as atomic layer deposition, chemical vapor deposition, molecular beam epitaxy, magnetron sputtering, electron-beam deposition, spin coating, and solution casting, with each method possessing its own subdiscipline for optimizing results.[4] The breadth and intricacy of thin film growth methods, the increasing number of potential predeposition and postdeposition treatments, and the complexity of multilayer architectures have significantly increased the number of experimental options per device application. As a result, a system for the rapid correlation of design decisions to device performance is needed to reduce the iterative exploration of process conditions to achieve the optimal devices.

The device performance of a field-effect transistor depends on the sensitivity of the semiconducting channel's conductivity on an applied electric field. A variety of electrical techniques, such as the transfer curve and van der Pauw methods, are employed to assess the power required for device operation, the efficiency of charge transport within the semiconductor, and the maximum change of channel conductivity.[5−7] Industrially, these tests can be performed using in-line metrology equipment[8,9] or automated machinery installed with probe cards matching the fabricated integrated circuit.[10] In an academic environment, electronically evaluating samples is often performed manually due to (i) the novelty and frequent evolution of device designs in exploratory research, necessitating an easily customizable testing platform, and (ii) funding constraints compared to industrial laboratories. To perform these measurements manually often requires time-intensive handling of individual samples and the application of retractable probes or soldered wires over a sample's contact points. Through programs such as the National Nanotechnology Initiative,[11] academic and start-up organizations have increased access to nanotechnology facilities to conduct exploratory electronic device research, thus incentivizing the design of an easily adaptable, low-cost system for employing electrical measurements.

Alongside the increasing need for economical, automated metrology setups has been the maturation of the printed circuit board (PCB) industry. PCBs are now readily customizable, low-cost, and fabricated commercially with quick turnaround. When interfaced with programmable microcontrollers, PCB-based equipment can be utilized for numerous research applications, such as ion-guided mass spectrometry devices,[12]

Received: July 2, 2024
Revised: August 29, 2024
Accepted: August 30, 2024
Published: September 27, 2024

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

melting curves,[13] open-source potentiostats,[14−16] photovoltaic cells,[17] nanopore fabrication,[18] and chromatographic detectors.[19] A PCB and microcontroller-based platform for the rapid execution of field-effect transistor measurements would provide a means of efficiently correlating design decisions to device metrics without the need for high-capital equipment. Additionally, the transparency of PCB-based technology and open-source software allows for easy customization, meaning that the same platform can be reprogrammed and used for a variety of electrical tests.

In this work, we present a low-cost automated test station for electronic transport measurements called ATLAS-MAP. The system was designed with PCB-based technology, leveraging microcontrollers to conduct sequential measurements without user intervention. All instrument control code was written via open-source Python libraries. The system conducted two common electrical measurements for semiconductors, specifically the transfer curve and van der Pauw analyses. To validate the instrument performance, transistors of a well-studied material, zinc oxide,[20,21] were fabricated and compared with literature results. The aim of this work was twofold: (i) to develop a low-cost, customizable test station for the automated execution of gated electronic measurements and (ii) to highlight the opportunity for a paradigm shift toward data automatization in exploratory device fabrication research. The instrument was designed for broad implementation in multiple laboratories, and detailed descriptions of all parts are provided.

EXPERIMENTAL METHODS

Instrument Description

Our testing platform, called ATLAS-MAP, was intended to serve as an automated alternative to a traditional probe station. At a probe station (Figure 1a), the sample is electrically connected to commercial source-measure units (SMUs) via metallic probe needles. To reroute the signal of the sourcemeters to a different position or subsequent sample, the probes must be adjusted manually via micropositioners. Under a constraint of 1 h, Figure 1b shows an estimation of the time allotted to set up the system, adjust the probes between scans, and measure device performance. This method requires intensive user involvement between scans to adjust probes to the next device under test. In contrast, the ATLAS-MAP test station (Figure 1c) was controlled via a computer and reroutes the sourcemeter signal to devices of interest automatically, without user intervention. In its current configuration, ATLAS can support up to three MAP units, though future iterations of its design could increase this number. Each MAP unit holds one sample, which itself hosts up to eight nanofabricated devices. This means that after loading three samples into ATLAS-MAP, the system can collect data from multiple measurements on up to 24 devices in rapid succession, without user involvement. Figure 1d shows the demarcation of time associated with measurement setup and testing using the ATLAS-MAP system within a 1 h constraint. Compared to the manual method (shown in Figure 1b), using the ATLAS-MAP system resulted in nearly a three-fold increase in data procurement with no in-person adjustments required between measurements. Eliminating user intervention further highlights the benefit of the ATLAS-MAP system as it enables the simultaneous advancement of other projects while collecting data with this tool.

The test station design, shown in Figure 2a, consisted of two main components, ATLAS and MAP. The MAP, or multiterminal automated platform, served as an individual testing unit and interfaced directly with the sample under evaluation. ATLAS (not an acronym, named such as it orchestrates a collection of MAPs) was the multiplexing unit responsible for routing the electronic signal from SMUs to the designated MAP in use. Signal rerouting to the desired

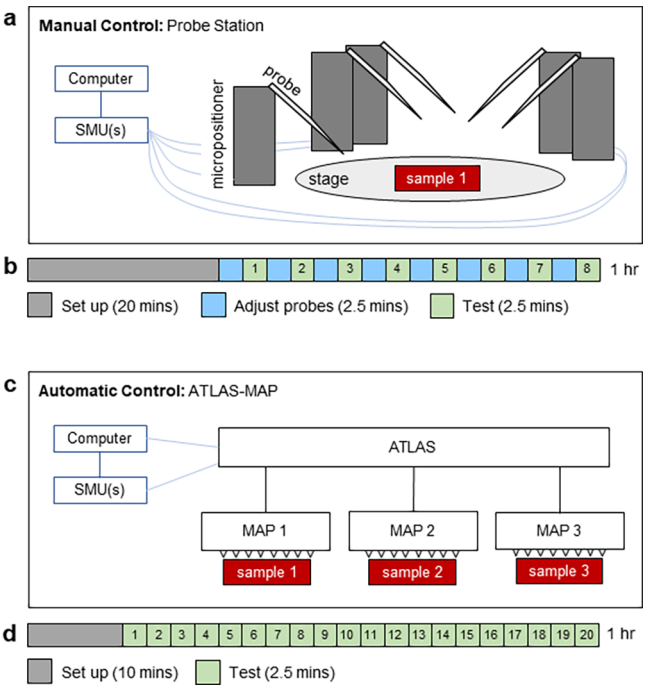


Figure 1. (a) Manual approach to electronic measurements via a probe station and (b) estimated time required to set up this system, adjust probes, and acquire data. (c) Automatic approach to electronic measurements via the ATLAS-MAP test station and (d) estimated time required to set up this system and acquire data automatically. SMU(s) stand for source-measure unit(s).

MAP and device under test was achieved via computer-controlled microcontrollers embedded in the PCB-based technology of both the MAP and ATLAS. Though industrial applications typically employ surface-mounted and multilayered PCB circuitry to minimize device footprint, we chose to utilize through-hole circuit components to minimize overall costs and improve ease of construction for experimentation. The sample, containing multiple devices of interest, sat on a retractable sample cartridge that mated with pushpins located on the underside of the MAP. This cartridge design enabled back-gating of the samples and easy reloading of devices. The ATLAS-MAP test station was interfaced with external SMUs but can also be paired with a variety of electrical analyzers possessing BNC connectors and operating within the relay specifications (parts listed in Table S1).

In ATLAS, the microcontroller first received commands from a central processing unit (CPU) to configure the relay pathways such that there was electrical continuity between the sourcemeter terminals and the specified MAP unit for testing (Figure 2b). The SMU sent and received electronic signals through ATLAS, which were then saved to the CPU for analysis. The internals of ATLAS are shown in Figure 2c. Power and computer commands from the CPU were sent to ATLAS via a bulkhead USB port (1) connected directly to the ATLAS Raspberry Pi Pico microcontroller (3). The microcontroller responded to the CPU commands by switching relays (4) to enable an electronic pathway between the sourcemeter(s) and MAP of interest. The current configuration of ATLAS was presented on an external display (the red screen shown in Figure 2a) via a second bulkhead USB port (2). Once ATLAS was electronically configured, the SMUs sent signal to the BNC inputs (5) of ATLAS. These signals traveled the relay pathways to a set of BNC outputs for one of the three MAP devices, named MAP 1 (6), MAP 2 (8), or MAP 3 (10). Electronic communication occured between ATLAS and the MAP units via Ethernet cords, which are labeled in Figure 2c as (7), (9), and (11), for MAP 1, MAP 2, and MAP 3, respectively. Overall, the development of ATLAS enabled measurement sequencing across multiple MAPs and added electrical routing to probe film isotropy in four orthogonal directions during the four-probe measurement.

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

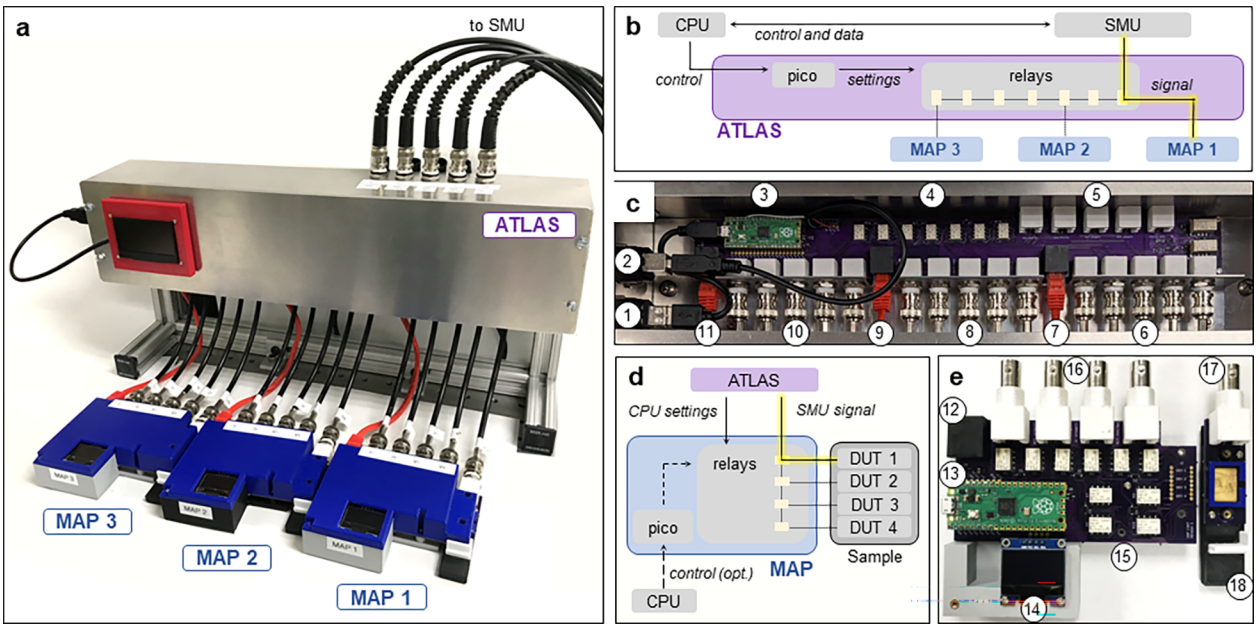


Figure 2. (a) Full instrument: SMU(s) connected to ATLAS and rerouted to three MAP units. (b) Simplified illustration of ATLAS functions. (c) Internals of ATLAS: (1) bulkhead USB port to CPU, (2) bulkhead USB port to the ATLAS external screen, (3) ATLAS microcontroller, (4) relays, (5) BNC inputs from the SMU, (6,8,10) BNC outputs for MAP 1, 2, and 3, and (7,9,11) Ethernet cords from ATLAS to MAP 1, 2, and 3. (d) Simplified illustration of MAP functions. (e) Internals of the MAP: (12) Ethernet from ATLAS, (13) optional MAP microcontroller, (14) MAP external screen, (15) relays, (16) BNC inputs from ATLAS or SMU, (17) BNC input for gate voltage, and (18) retractable sample cartridge.

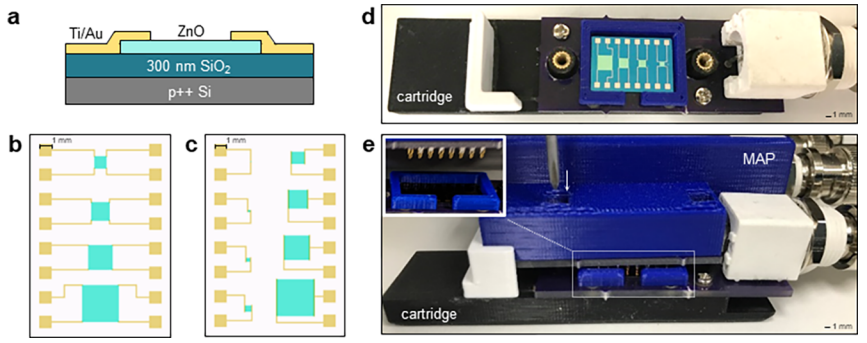


Figure 3. (a) 2D schematic of the fabricated transistor featuring the gate (p++ Si), dielectric (300 nm SiO_2), semiconducting channel (variable thicknesses of ZnO), and metallic contacts (5 nm Ti, 30 nm Au). The standard form factor for samples with (b) four-terminal devices and (c) two-terminal devices. (d) Van der Pauw sample loaded into the MAP sample cartridge. (e) Sample cartridge aligned and screwed into the MAP. The inset shows the retractable pushpins on the underside of the MAP which align over the sample contact pads.

In each MAP system, the sourcemeter signal was rerouted via relays to the specific device under test (DUT) on the inserted sample (Figure 2d). In addition to being compatible with ATLAS, each MAP unit can be operated independently via its own microcontroller and directly attached to the CPU and SMUs. The internals of the MAP are shown in Figure 2e. When orchestrated to ATLAS, a MAP unit received power and configuration settings via an Ethernet cord (12). To operate the MAP microcontroller independently from ATLAS, a cord from the computer can be plugged directly into the micro-USB port of the MAP microcontroller (13). MAP configuration settings were displayed on an external display (14) and control the routes of the relays (15) to the specific device of interest. Once the MAP was properly configured, BNC inputs (16) received signal from the sourcemeters connected to ATLAS. One BNC input (17) specifically directed the gate voltage input to the retractable sample cartridge (18) containing the devices of interest.

Instrument Materials and Assembly

PCB layouts for the MAP and ATLAS were designed in KiCad[22] and submitted to the company OSH Park for fabrication; see Section S1 for access to design files and Figures S1−S6 for circuit diagrams, schematics, and unit dimensions. General rules of thumb for PCB design were followed, including minimizing the number of through-hole vias, keeping traces large to ensure good electrical connection, maintaining an appropriate gap between traces to minimize signal interference, etc. The PCBs utilized two layers of conductive copper to minimize the overall footprint of the device. The Raspberry Pi Pico RP2040 microcontrollers were mated to the PCBs by using a pin and socket header. Instrument settings were displayed on a similarly mounted 0.96 in. or 2.4 in. OLED I2C screen. Communication and sourcemeter signals were transmitted between individual units via 6 in. Ethernet cords and BNC cables.

Multiple double-pole double-throw signal relays routed the input signal from the sourcemeters to the user-specified location of the DUT. Each relay had four connectors and was configured to control two distinct electronic pathways at once, thus minimizing the overall number of circuit components per PCB. An NPN bipolar transistor acted as a voltage amplifier and switch to control the configuration of the relay. To protect these circuit components, resistors were added to limit the current flow to the transistor and to pull down to ground any floating voltage remaining in the disconnected relays. A flywheel diode was inserted in parallel with each relay to dissipate the back

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

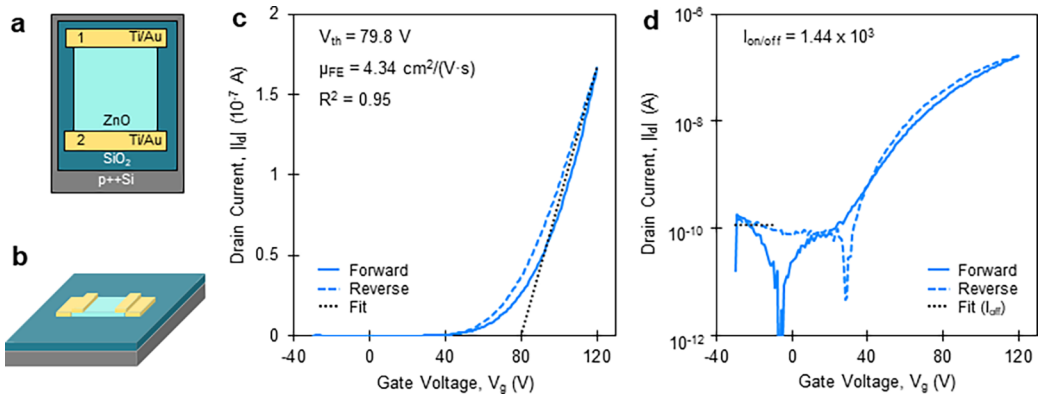


Figure 4. Two-terminal device shown in (a) 2D, top-down, and (b) 3D view. The drain current behavior of 10 nm ZnO film with a channel length and width of 50 μm as a function of gate voltage shown on a (c) linear and (d) semilog plot. The forward and reverse voltage sweeps are indicated with solid and dashed lines, respectively. The black dotted fits represent the (c) high-bias fitting to extract threshold voltage and (d) low-bias fitting to extract the off current.

electromagnetic fields upon relay switching. To smooth any irregularities in the USB power supply, a capacitor was added to the power line for filtering. All circuit components were soldered onto the board using a lead-free solder wire. The sample being tested rested on a custom cartridge that can be loaded and unloaded from the system. This cartridge enabled backside gate contact to the sample via a simple PCB with a large conductive copper area and one BNC connector. Spring pins protruding from the bottom of the MAP PCB were designed to fit precisely over the sample's fabricated contact points. To ensure sufficient electrical contact between the PCB push pins and sample contact points, the cartridge and main board were screwed together such that the pushpins underneath the MAP were aligned and lightly compressed against the sample's contact pads. 3D printer holders for the MAP units and cartridges were designed and fabricated using a Prusa i3MK3S+ 3D Printer with a PLA filament. A metal chassis was custom-built to house the ATLAS, complete with bulkhead USB ports to power the instrument and the external screen. The complete ATLAS-MAP apparatus was built for only $400; for a complete list and bill of materials, consult Table S1.

Sample Fabrication and Loading

Zinc oxide field-effect transistors were fabricated via multiple photolithographic and deposition steps outlined in Section S2 and displayed in Figure S7. A graphic of the final transistor device is shown in Figure 3a. In brief, commercial p++ Si wafers with 300 nm thermal SiO_2 underwent Ti/Au electron-beam deposition for alignment marks, atomic layer deposition and wet etching of ZnO for semiconducting channels, and 5 nm Ti/30 nm Au electron-beam deposition for electrical contacts and lift-off, all interspersed with photolithographic steps. The channel length and width varied from 50 μm to 3 mm, with the aspect ratio fixed at one. ZnO was grown at various nominal thicknesses: 5, 10, and 20 nm. Once the wafer was fully processed, individual samples were diced into rectangles of a uniform size. The back side of each sample was then scratched and coated in silver paint to improve the back-gated electrical contact.

To implement proper mating of the MAP to the samples, all fabricated samples followed a standard form factor. Figure 3b,c displays schematic illustrations of samples for the four-probe van der Pauw analysis and the two-probe transfer curve method, respectively. This standard geometry featured gold pads 1 mm by 1 mm with 1 mm spacing, centered 0.75 mm from each edge, on a 11.5 mm by 16.5 mm rectangular chip. The diameter and spacing of the pushpins protruding from the MAP PCB dictated the size and spacing of the gold pads. The overall chip geometry was selected to maximize the yield of 18 samples per wafer, with four four-terminal devices or eight two-terminal devices per sample. Utilizing this standard device layout with contact pads located on the perimeter of the sample allowed for time-efficient probe placement at submillimeter precision via the MAP. Notably, within the constraints of sample size and relative position of the contact pads, the channel size and shape could take any form, making a tailorable platform for a variety of device geometries. Once fabricated, the sample was loaded into the MAP sample cartridge (Figure 3d). Once in position, the MAP was lowered over the sample cartridge and screwed into place (Figure 3e). On the underside of the MAP, retractable pushpins compressed against the metallic contact pads on the loaded sample, enabling electrical contact. This methodology both reduced the time required for sample mounting and minimized user loading errors.

Instrument Software

Instrument drivers were developed to control the MAP units and ATLAS routing configurations with CircuitPython.[23] Individual graphical user interfaces (GUIs) for each form of electronic test were developed utilizing the open-source PyMeasure library.[24] User input variables included sample identification information, experimental parameters, and a list of samples to be sequenced for automated testing. Figure S11 shows a representative example of the transfer curve GUI. Refer to Section S1 for all code related to instrument control. The sourcemeters used for electrical measurements were the Keithley 2400 and 2611B. These were controlled remotely via their instrument drivers included in the PyMeasure framework.[24] For the various electrical connections to ATLAS, see Figure S12.

RESULTS AND DISCUSSION

Transfer Curves (Gated Two-Terminal Measurements)

The transfer curve is a common measurement to quantify the electronic properties of a field-effect transistor.[6,25] Material properties determined by this method include (i) the threshold voltage (V_{th}), the voltage required to fill deep trap energy band states and form a conductive channel, (ii) field-effect mobility of charge carriers (μ_{FE}), and (iii) the on−off ratio ($I_{on/off}$), the order of magnitude of manipulatable current across the semiconductor. This technique requires a two-terminal sample geometry, as shown in Figure 4a,b. To conduct this measurement across all samples, the gate voltage (V_g) was cycled between −30 and 120 V at a rate of 2 V/s, while the source and drain voltage (V_d) remained constant at 0 and 0.1 V vs ground, respectively.

Based on the performance of the transistor, the material parameters of the semiconductor can be determined. Under the conditions where $|V_g| > |V_{th}|$ and $|V_d| \ll |V_g - V_{th}|$, the drain current (I_d) varied linearly with the applied gate voltage according to the following equation[26]

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

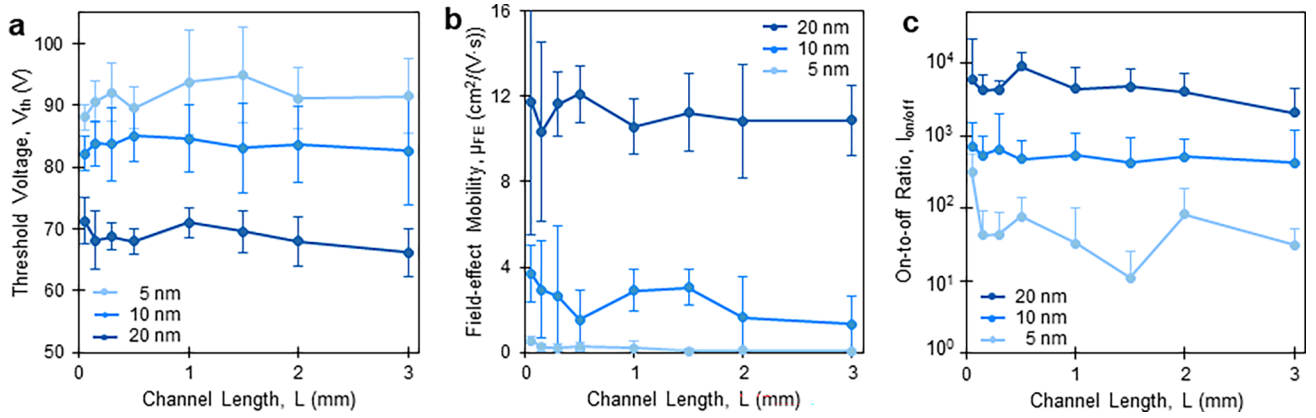


Figure 5. Calculated (a) threshold voltage, (b) field-effect mobility, and (c) on-to-off ratio of ZnO transistors of various thicknesses and channel lengths. For all samples, the aspect ratio was one. The error bars show a 95% confidence interval calculated using 2−5 samples or measurements per data point. No lower error bars are shown in panel (c) for visual clarity on a logarithmic plot. For all data points, the drain voltage was 0.1 V and the scan rate was 2.0 V/s.

$$I_d = \mu_{FE} C_I \frac{W}{L} |V_g - V_{th}| V_d \quad (1)$$

where $\frac{W}{L}$ is the aspect ratio and C_I is the specific capacitance of the insulating dielectric. All samples in this study featured 300 nm of SiO_2 as the dielectric. The specific capacitance of 300 nm silica, with a conservatively assumed dielectric constant of 3.2,[27] was calculated to be 9.44 nF/cm^2 according to the following equation

$$C_I = \frac{k\varepsilon_0}{d} \quad (2)$$

where k, ε_0, and d represent the dielectric constant, permittivity of vacuum, and thickness of the dielectric, respectively. To extract the charge carrier mobility, the slope of the average I_d versus V_g in the linear regime (100 to 120 V) was used.[28] The threshold voltage was calculated from the linear fit of I_d versus V_g at high gate voltages extrapolated to the point of zero drain current.[29,30] The off current was approximated as the absolute value of the average current from the forward scan between negative 30 and 0 V. The on-to-off ratio was defined as the ratio between the maximum drain current and the off current.

Figure 4c,d shows representative results of 10 nm ZnO films on 300 nm SiO_2/p++ Si with a channel length of 50 μm and aspect ratio of one. Current across the channel remained low until around a back-gate of 40 V, after which drain current, or carrier concentration, exponentially increased with gate voltage. This behavior was indicative of the n-type transistor turning on. The increase in drain current was reversible; the device turned off on the reverse sweep. Extracting the material properties of this device resulted in a threshold voltage of 79.8 V, a field-effect mobility of 4.34 cm^2/(V·s), and an on-to-off current ratio of 1.44×10^3. These results agree with similarly fabricated ZnO devices where the threshold voltage was 65.9 V, the field-effect mobility was 1.1 cm^2/(V·s), and the on-to-off current ratio was 2.59×10^3.[31,32] The minor counterclockwise hysteresis of the transfer curve is likely due to hole migration within the dielectric toward the dielectric−semiconductor interface, enhancing the strength of the gate, inducing extra charge carriers in the n-type film, and thus improving conduction.[33,34] The results acquired using the ATLAS-MAP system closely resemble those taken on a traditional probe station, though drain current and field-effect mobility seem to be slightly underestimated in the ATLAS-MAP system (see Figure S14 for additional discussion).

To further evaluate the performance of the MAP and ATLAS design, two-terminal measurements were repeated for multiple devices with variation of the channel size and thickness of zinc oxide. Figure 5 shows the threshold voltage, mobility, and on-to-off ratio for ZnO FETs of various thicknesses (5 to 20 nm) and channel lengths (50 μm to 3 mm, with equal widths). At each channel length, the threshold voltage decreased (Figure 5a), and the mobility and on-to-off ratio increased (Figure 5b,c) as the film thickness increased. This phenomenon likely resulted from morphological changes within the film. As shown with other zinc-based transistors, enlarged channel thicknesses resulted in increased crystallinity, increased grain size, decreased film roughness, and decreased trap densities.[35,36] These changes result in a larger concentration of mobile charge carriers as thickness increased, lowering the voltage required to form a conductive channel.[35−37] The enhanced mobility for thicker films likely arose from a two-fold affect: (i) the decreased roughness of the channel decreased the number of scattering events and (ii) the increased thickness of the film lowered the strength of the electric field within the semiconductor, decreasing the attraction of charge carriers to the traps at the semiconductor−dielectric interface.[35,36] There was little impact of channel size on transistor performance; this is expected, as the aspect ratio remained constant at one. Table S2 summarizes the extracted material properties for each ZnO thickness. See Figures S15 and S16 for representative transfer curves for devices as a function of the thickness and channel size.

In addition to validating the operation and results from the ATLAS-MAP system, Figure 5 illustrates the extent of electronic information that can be achieved using an automated test station. In the manual method (a probe station), collecting a rich data set would require intensive user involvement to manually change probe, sample, and device orientation, culminating in a longer time to complete the experiment, user fatigue, and the cost of progress in other projects. With the ATLAS-MAP instrument, a long measurement queue of up to 24 devices can be set to run at once without the need for user intervention. This speeds up data collection for a large data set by up to three-fold, as shown in Figure 1b,d, and enables the completion of other work in

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

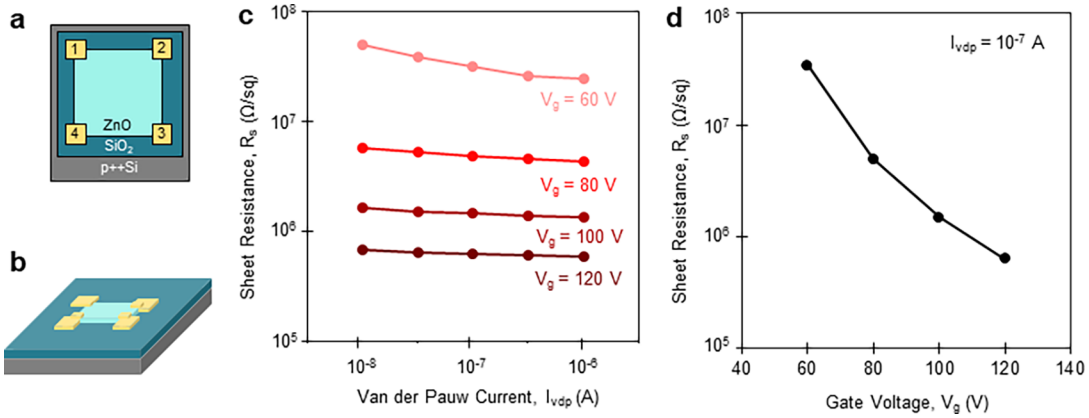


Figure 6. Four-terminal device shown in (a) 2D, top-down, and (b) 3D view. For a 10 nm ZnO/300 nm SiO_2/p++ Si device with a channel size of 50 μm by 50 μm, (c) sheet resistance as a function of applied current and gate voltage and (d) sheet resistance dependence on gate voltage at an applied current of 10^{-7} A.

parallel by circumventing the need for in-person adjustments, further highlighting the benefits of an automized test station.

Van der Pauw Measurements (Gated Four-Terminal Measurements)

The van der Pauw technique is another commonly implemented method for probing semiconductor characteristics, which utilizes four terminals to measure the sheet resistance of a film without the convolution of contact resistance.[38,39] To conduct this measurement, four Ti/Au contact pads were placed around the perimeter of the sample under test, as shown in Figure 6a,b. The sample area under the contact pads remained at or under 5% of the total sample area for all devices to ensure an accurate assessment of the semiconductor.[40] A current (I_{vdp}) was applied between two adjacent terminals, and the induced voltage was measured on the remaining terminals parallel to the current path. The ratio of voltage to current determined the sheet resistance, as per Ohm's law. Repeating this measurement in two orthogonal directions elucidates the film anisotropy.

The additional application of a gate voltage while performing van der Pauw measurements yields the dependence of sheet resistance and carrier concentration on gate voltage and the apparent mobility of the film.[41,42] To determine these film parameters, a series of calculations were performed, as detailed in Section S3 and summarized as follows. Beginning with the van der Pauw equation[38,40]

$$\exp\left(\frac{-\pi t}{\rho}R_{\parallel}\right) + \exp\left(\frac{-\pi t}{\rho}R_{\perp}\right) = 1 \tag{3}$$

where $R_{\parallel}$ and $R_{\perp}$ are average resistances calculated across perpendicular axes and ρ and t are the resistivity and thickness of the film of interest, respectively. Combining this with eq 1 for the linear regime of gated transistors, the final equations for the sheet resistance (R_S) and apparent mobility (μ_{app}) are reported as follows

$$R_S = \frac{\pi}{\ln 2}\left(\frac{R_{\parallel} + R_{\perp}}{2}\right) \tag{4}$$

$$\mu_{app} = \frac{1}{R_S C_I |V_G - V_{Th}|} \tag{5}$$

For this project, the applied current (I_{vdp}) was varied logarithmically between 10^{-8} and 10^{-6} A. The back-gate was varied at 20 V intervals between 60 and 120 V. For voltages lower than 60 V, the semiconductor film was in the off state and therefore exhibited a minimal conductance below the detection limit of the Keithley 2400 sourcemeter (5 nS, or 200 MΩ).[43] The ZnO resistance was isotropic (Figure S17), and the reported resistances represent the average of two orthogonal current-flow configurations. Figure 6c shows a representative plot of sheet resistance versus applied current using the van der Pauw technique for a 10 nm ZnO on 300 nm SiO_2/p++ Si device with a channel size of 50 μm by 50 μm. In Figure 6c, the measured sheet resistance was largely independent of the applied current across the film, indicative of ohmic contact with the semiconductor and an absence of significant heating effects. The slight nonlinearity at 60 V is likely due to the channel beginning to turn on (i.e., the voltage was insufficiently inducing charge carriers for conduction). Like the drain current during the transfer curve analysis (Figure 4d), the measured sheet resistance varied logarithmically (6.32×10^5 to 3.40×10^7 Ω/sq) with gate voltage (60 to 120 V), as shown in Figure 6d.

These gated van der Pauw measurements were repeated as functions of thickness and channel size. Figure 7 depicts the sheet resistance and apparent mobility of zinc oxide, four-terminal devices as a function of thickness (10 and 20 nm), and channel length (50 μm to 3 mm, with an aspect ratio of one). (For the data replotted as a function of channel size, see Figure S18.) As shown in Figure 7a, the sheet resistance decreased as a function of the gate voltage for all devices, as expected. Additionally, as thickness increased, the resistance decreased, likely due to increased crystallinity of the thicker zinc oxide as discussed above. From the same figure, the 20 nm-thick ZnO devices showed no impact of channel length on sheet resistance, whereas the 10 nm-thick devices showed that decreasing the channel length lowered the sheet resistance for all gate voltages. This is possibly due to increased trap densities and lateral inhomogeneities in the thinner film, which is exacerbated as channel length increases[40] or a decrease in the accuracy of the van der Pauw method for ultrathin, large-channel films.[44] Figure 7b shows the apparent mobility of the 10 and 20 nm films, which were comparable to the values extracted via the two-terminal measurements (Figure 5b).

Gate-Sweeping van der Pauw Measurements

For further exploration, the van der Pauw procedure was changed to continually measure the sheet resistance while

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

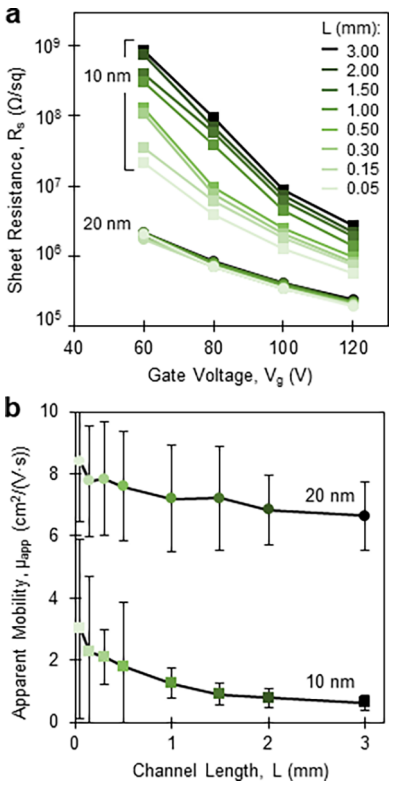


Figure 7. (a) Measured sheet resistance and (b) calculated apparent mobility of ZnO transistors as a function of gate voltage, thickness, and channel lengths. For all samples, the aspect ratio was one. The error bars show a 90% confidence interval calculated using 2−4 samples or measurements per data point. For all measurements, I_{vdp} was held at 10^{-7} A.

applying a sweeping gate voltage.[41] Reprogramming and operating this new procedure required minimal effort from the user, highlighting the benefits of the highly transparent instrument control of the ATLAS-MAP system. In this new procedure, current applied (10^{-7} A) across two adjacent contact pads induced a parallel voltage which varied as gate voltage scanned from −20 to 120 at 1.0 V/s.

Coupling the transfer curve and van der Pauw results enabled the extraction of the contact resistance of the film. At the interface of the metal contact and semiconductor, there exists an injection barrier which inhibits charge conduction into the semiconductor, thus lowering the impact of source-drain polarization on the channel's conduction.[45,46] Contact resistance can be evaluated using a variety of techniques.[46] In this method, the difference in sheet resistance measured via the transfer curve and sweeping gate-voltage van der Pauw methods represents the contact resistance. The resistance measured via the transfer curve measurement (R_{total}) includes resistive losses at the Ti/Au and ZnO interface, whereas the resistance measured via the van der Pauw method (R_{sample}) circumvents the effect of contact resistance. As a result, the total contact resistance ($R_{contact}$) can be calculated via the following equation

$$R_{contact} = R_{total} - R_{sample} \quad (6)$$

In Figure 8, the resistances from the two- and four-terminal measurements and the calculated contact resistance are shown as a function of gate voltage for a 20 nm-thick, 1 mm² ZnO channel. As the gate voltage increased, the sheet resistance

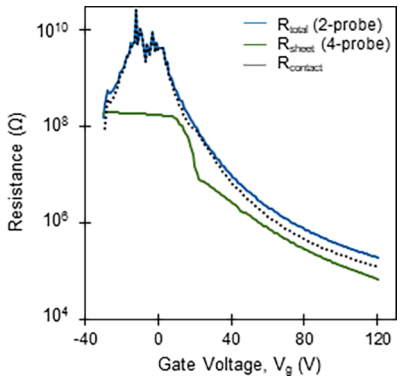


Figure 8. Resistance as measured from the two-(blue) and four-terminal (green) measurements of a 20 nm ZnO transistor with a channel length and width of 1 mm superimposed with the calculated contact resistance (dashed black). Only forward scans shown for visual clarity.

logarithmically decreased for both measurements. As expected, the two-terminal resistance was larger than the four-terminal resistance due to the inclusion of contact resistance. In the four-terminal measurement, the plateau at 200 MΩ represents the limit of the 2400 Keithley sourcemeter.[43] Like the two- and four-terminal resistances, the extracted contact resistance varies logarithmically as a function of the gate voltage. Contact resistance is dependent on the bulk resistance of the semiconductor, as well as the mobility of free charge carriers in the channel, leading to the sensitivity of channel resistance on gate voltage.[45,47,48] These results show that contact resistance was comparable to the overall resistance of the film, indicating the need for further device optimization and the benefit of an easily accessible electronics characterization toolkit. Figure S19 shows resistances derived from the gate-sweeping van der Pauw method as a function of ZnO thickness.

CONCLUSIONS

In response to the growing design space for device fabrication, we have designed and built a low-cost test station to automate electronic transport measurements of back-gated, coplanar field-effect transistor architectures. The instrument consisted of a central platform called ATLAS with three multiterminal automated platforms (MAPs). The ATLAS-MAP system enabled the multiplexing and automatic sequencing of two- and four-terminal measurements, namely, the transfer curve and van der Pauw analysis, via a programmable graphical interface coordinating commercial sourcemeters and the PCB-based test station. Utilizing PCB technology, microcontrollers, and standard device layouts allowed for submillimeter-precise probe placement with signal integrity comparable to manual methods at inexpensive costs. All measurement procedures were written using existing open-source Python libraries and generated standardly formatted data compatible with metadata sorting and automatic data processing.

The design and programming flexibility of the test station enable adaptation to a wide variety of applications, testing methods, and differing transistor architectures. To adapt the test station for individually back-gated samples, the sample cartridge can be redesigned to incorporate PCB relay components to route the gate voltage signal to individual copper gating pads. The single-routing design of this cartridge can be modeled after the circuitry in the current ATLAS-MAP

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667

system. To enable top-gated architectures, the gate voltage BNC input can be relocated from the sample cartridge to the MAP and additional relays and pathways can be added to the MAP to control the gate voltage routing. In this design, the sample cartridge would act only as a retractable container for inserting and aligning the sample to the MAP, and the gate voltage would be applied via the MAP's pushpins in contact with the top-side gate of the device of interest.

To validate the design of the ATLAS-MAP system for globally back-gated transistors, we fabricated ZnO devices with various channel sizes and thicknesses. Values obtained from ATLAS-MAP agreed with those in the literature, and these devices performed as expected for an n-type semiconductor: the conductivity of zinc oxide increased as a function of gate voltage due to increased charge carrier densities. Likewise, the channel conductivity increased as the thickness of ZnO increased, likely due to increased grain sizes and decreased charge scattering. These findings were consistent across two- and four-terminal measurements with static and sweeping gate voltages, all conducted in the ATLAS-MAP system. Higher testing throughput provides an increased capability for data generation and the correlation of device performance to fabrication procedures such as deposition tools, growth conditions, and annealing. Ultimately, this can be leveraged to better inform material design choices to achieve the optimal devices. In performing multiple types of electronic measurements using a known material, we demonstrated the capability of this instrument to be used as a low-cost, customizable station for efficiently assessing device properties in exploratory research.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsmeasuresciau.4c00034.

Sample fabrication, ATLAS-MAP circuitry and parts, and device performance (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

C. Daniel Frisbie − *Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis 55455 Minnesota, United States; Department of Chemical Engineering and Materials Science, Center for Programmable Energy Catalysis, University of Minnesota, Minneapolis 55455 Minnesota, United States;* orcid.org/0000-0002-4735-2228; Email: frisbie@umn.edu

Daniel McDonald − *Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis 55455 Minnesota, United States; Department of Chemical Engineering and Materials Science, Center for Programmable Energy Catalysis, University of Minnesota, Minneapolis 55455 Minnesota, United States;* orcid.org/0009-0008-8198-6305; Email: mcdo0486@umn.edu

Authors

Amber Walton − *Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis 55455 Minnesota, United States; Department of Chemical Engineering and Materials Science, Center for Programmable Energy Catalysis, University of Minnesota, Minneapolis 55455 Minnesota, United States;* orcid.org/0000-0003-0600-1613

Michael Manno − *Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis 55455 Minnesota, United States*

Paul J. Dauenhauer − *Department of Chemical Engineering and Materials Science, University of Minnesota, Minneapolis 55455 Minnesota, United States; Department of Chemical Engineering and Materials Science, Center for Programmable Energy Catalysis, University of Minnesota, Minneapolis 55455 Minnesota, United States;* orcid.org/0000-0001-5810-1953

Complete contact information is available at: https://pubs.acs.org/10.1021/acsmeasuresciau.4c00034

Author Contributions

A.W. fabricated transistors, performed experiments, analyzed data, and wrote the manuscript. D.M. designed and constructed the MAP and ATLAS and developed instrument drivers. M.M. aided in the discussion of experimental methods and the manuscript. A.W. and D.M. co-developed test scripts to run experimental methods. P.J.D. and C.D.F. supervised the project and reviewed the manuscript. All authors have given approval to the final version of the manuscript.

Funding

This work was supported as part of the Center for Programmable Energy Catalysis, an Energy Frontier Research Center funded by the U.S. Department of Energy, Office of Science, Basic Energy Sciences at the University of Minnesota under award number DE-SC0023464. Additional funding for this work was supplied via the U.S. Department of Energy on sponsor award number DE-SC0021163. Portions of this work were conducted in the Minnesota Nano Center, which is supported by the National Science Foundation through the National Nano Coordinated Infrastructure Network (NNCI) under award number ECCS-2025124.

Notes

The authors declare no competing financial interest.

■ REFERENCES

(1) Goasduff, L. *Gartner Forecasts Worldwide Semiconductor Revenue to Decline 11% in 2023*; Gartner. https://www.gartner.com/en/newsroom/press-releases/2023-04-26-gartner-forecasts-worldwide-semiconductor-revenue-to-decline-11-percent-in-2023 (accessed 2024-03-18).

(2) Franssila, S. *Introduction to Microfabrication*; John Wiley & Sons, 2010.

(3) Zant, P. V. *Microchip Fabrication*, 5th Ed.; McGraw Hill Professional, 2004.

(4) Vossen, J. L.; Kern, W. *Thin Film Processes II*; Gulf Professional Publishing, 1991.

(5) Schroder, D. K. *Semiconductor Material and Device Characterization*, 3 ed.; Wiley-Interscience: Hoboken, NJ, 2006.

(6) Cheng, Z.; Pang, C.-S.; Wang, P.; Le, S. T.; Wu, Y.; Shahrjerdi, D.; Radu, I.; Lemme, M. C.; Peng, L.-M.; Duan, X.; Chen, Z.; Appenzeller, J.; Koester, S. J.; Pop, E.; Franklin, A. D.; Richter, C. A. How to Report and Benchmark Emerging Field-Effect Transistors. *Nat. Electron.* **2022**, *5* (7), 416−423.

(7) Mitta, S. B.; Choi, M. S.; Nipane, A.; Ali, F.; Kim, C.; Teherani, J. T.; Hone, J.; Yoo, W. J. Electrical Characterization of 2D Materials-Based Field-Effect Transistors. *2D Mater.* **2021**, *8* (1), 012002.

(8) Orji, N. G.; Badaroglu, M.; Barnes, B. M.; Beitia, C.; Bunday, B. D.; Celano, U.; Kline, R. J.; Neisser, M.; Obeng, Y.; Vladar, A. E.

Metrology for the next Generation of Semiconductor Devices. *Nat. Electron.* **2018**, *1* (10), 532−547.
(9) Ebayyeh, A. A. R. M. A.; Mousavi, A. A Review and Analysis of Automatic Optical Inspection and Quality Monitoring Methods in Electronics Industry. *IEEE Access* **2020**, *8*, 183192−183271.
(10) Grochowski, A.; Bhattacharya, D.; Viswanathan, T. R.; Laker, K. Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and Future Trends. *IEEE Trans. Circuits Syst.* **1997**, *44* (8), 610−633.
(11) Roco, M. C. The Long View of Nanotechnology Development: The National Nanotechnology Initiative at 10 Years. *J. Nanoparticle Res.* **2011**, *13* (2), 427−445.
(12) Kregel, S. J.; Thompson, B. J.; Nathanson, G. M.; Bertram, T. H. The Wisconsin Oscillator: A Low-Cost Circuit for Powering Ion Guides, Funnels, and Traps. *J. Am. Soc. Mass Spectrom.* **2021**, *32* (12), 2821−2826.
(13) Chahin, N.; Escobar-Nassar, S.; Osma, J.; Bashammakh, A. S.; AlYoubi, A. O.; Ortiz, M.; O'Sullivan, C. K. Low-Cost Platform for Multiplexed Electrochemical Melting Curve Analysis. *ACS Meas. Sci. Au* **2022**, *2* (2), 147−156.
(14) Caux, M.; Achit, A.; Var, K.; Boitel-Aullen, G.; Rose, D.; Aubouy, A.; Argentieri, S.; Campagnolo, R.; Maisonhaute, E. PassStat a Simple but Fast, Precise and Versatile Open Source Potentiostat. *HardwareX* **2022**, *11*, No. e00290.
(15) Glasscott, M. W.; Verber, M. D.; Hall, J. R.; Pendergast, A. D.; McKinney, C. J.; Dick, J. E. SweepStat: A Build-It-Yourself, Two-Electrode Potentiostat for Macroelectrode and Ultramicroelectrode Studies. *J. Chem. Educ.* **2020**, *97* (1), 265−270.
(16) Elias, J. S. An Improved Potentiostat/Galvanostat for Undergraduate-Designed Electrochemical Laboratories. *J. Chem. Educ.* **2024**, *101* (4), 1703−1710.
(17) Zachariadou, K.; Yiasemides, K.; Trougkakos, N. A Low-Cost Computer-Controlled Arduino-Based Educational Laboratory System for Teaching the Fundamentals of Photovoltaic Cells. *Eur. J. Phys.* **2012**, *33* (6), 1599−1610.
(18) Bandara, Y. M.; Karawdeniya, B. I.; Dutt, S.; Kluth, P.; Tricoli, A. Nanopore Fabrication Made Easy: A Portable, Affordable Microcontroller-Assisted Approach for Tailored Pore Formation via Controlled Breakdown. *Anal. Chem.* **2024**, *96* (5), 2124−2134.
(19) Foster, S. W.; Alirangues, M. J.; Naese, J. A.; Constans, E.; Grinias, J. P. A Low-Cost, Open-Source Digital Stripchart Recorder for Chromatographic Detectors Using a Raspberry Pi. *J. Chromatogr. A* **2019**, *1603*, 396−400.
(20) Özgür, Ü.; Hofstetter, D.; Morkoç, H. ZnO Devices and Applications: A Review of Current Status and Future Prospects. *Proc. IEEE* **2010**, *98* (7), 1255−1268.
(21) Vyas, S. A Short Review on Properties and Applications of Zinc Oxide Based Thin Films and Devices: ZnO as a Promising Material for Applications in Electronics, Optoelectronics, Biomedical and Sensors. *Johns. Matthey Technol. Rev.* **2020**, *64* (2), 202−218.
(22) KiCad Developers. *KiCad*, Version 8.0.3. https://www.kicad.org/(accessed 2024-06-10).
(23) CircuitPython Developers. *CircuitPython*, Version 9.0.5. https://circuitpython.org/(accessed 2024-06-10).
(24) PyMeasure Developers. *PyMeasure*, Version 0.13.1. https://github.com/pymeasure/pymeasure/releases/tag/v0.13.1 (accessed 2024-06-10).
(25) Wager, J. F. Transfer-Curve Assessment of Oxide Thin-Film Transistors. *J. Soc. Inf. Disp.* **2010**, *18* (10), 749−752.
(26) Zaumseil, J.; Sirringhaus, H. Electron and Ambipolar Transport in Organic Field-Effect Transistors. *Chem. Rev.* **2007**, *107* (4), 1296−1323.
(27) Volksen, W.; Miller, R. D.; Dubois, G. Low Dielectric Constant Materials. *Chem. Rev.* **2010**, *110* (1), 56−110.
(28) Choi, H. H.; Cho, K.; Frisbie, C. D.; Sirringhaus, H.; Podzorov, V. Critical Assessment of Charge Mobility Extraction in FETs. *Nat. Mater.* **2018**, *17* (1), 2−7.
(29) Boudinet, D.; Le Blevennec, G.; Serbutoviez, C.; Verilhac, J.-M.; Yan, H.; Horowitz, G. Contact Resistance and Threshold Voltage Extraction in N-Channel Organic Thin Film Transistors on Plastic Substrates. *J. Appl. Phys.* **2009**, *105* (8), 084510.
(30) Terada, K.; Nishiyama, K.; Hatanaka, K.-I. Comparison of MOSFET-Threshold-Voltage Extraction Methods. *Solid-State Electron.* **2001**, *45* (1), 35−40.
(31) Kim, C.-H.; Frisbie, C. D. Field Effect Modulation of Outer-Sphere Electrochemistry at Back-Gated, Ultrathin ZnO Electrodes. *J. Am. Chem. Soc.* **2016**, *138* (23), 7220−7223.
(32) Kim, C. H. *Continuous and Reversible Modulation of Interfacial Electrochemical Phenomena on Back-Gated Two Dimensional Semiconductors*, University of Minnesota, 2017.
(33) Egginger, M.; Bauer, S.; Schwödiauer, R.; Neugebauer, H.; Sariciftci, N. S. Current versus Gate Voltage Hysteresis in Organic Field Effect Transistors. *Monatsh. Chem.* **2009**, *140* (7), 735−750.
(34) Ye, Z.; Yuan, Y.; Xu, H.; Liu, Y.; Luo, J.; Wong, M. Mechanism and Origin of Hysteresis in Oxide Thin-Film Transistor and Its Application on 3-D Nonvolatile Memory. *IEEE Trans. Electron Devices* **2017**, *64* (2), 438−446.
(35) Oh, B.-Y.; Jeong, M.-C.; Ham, M.-H.; Myoung, J.-M. Effects of the Channel Thickness on the Structural and Electrical Characteristics of Room-Temperature Fabricated ZnO Thin-Film Transistors. *Semicond. Sci. Technol.* **2007**, *22* (6), 608−612.
(36) Chen, A. H.; Cao, H. T.; Zhang, H. Z.; Liang, L. Y.; Liu, Z. M.; Yu, Z.; Wan, Q. Influence of the Channel Layer Thickness on Electrical Properties of Indium Zinc Oxide Thin-Film Transistor. *Microelectron. Eng.* **2010**, *87* (10), 2019−2023.
(37) Yang, Z.; Yang, J.; Meng, T.; Qu, M.; Zhang, Q. Influence of Channel Layer Thickness on the Stability of Amorphous Indium Zinc Oxide Thin Film Transistors. *Mater. Lett.* **2016**, *166*, 46−50.
(38) van der Pauw, L. J. A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape. *Semicond. Devices* **1991**, *13* (1), 174−182.
(39) Deen, M. J.; Pascal, F. Electrical Characterization of Semiconductor Materials and Devices—Review. *J. Mater. Sci.: Mater. Electron.* **2006**, *17* (8), 549−575.
(40) Hu, X.; Zhu, L.; Diao, K.; Liu, W.; Deng, X.; Wang, H. Electrostatic Derivation for the van Der Pauw Formula and Simulation Using Arbitrarily Shaped Resistive Materials. *AIP Adv.* **2022**, *12* (7), 075208.
(41) Rolin, C.; Kang, E.; Lee, J.-H.; Borghs, G.; Heremans, P.; Genoe, J. Charge Carrier Mobility in Thin Films of Organic Semiconductors by the Gated van Der Pauw Method. *Nat. Commun.* **2017**, *8* (1), 14975.
(42) Chen, C.; Hu, S.; Chen, Z.; Shen, Y.; Liu, C.; Wu, Q.; Yang, T.; Liu, C. Generalized Gated Four-Probe Method for Intrinsic Mobility Extraction With Van Der Pauw Structure. *IEEE Electron Device Lett.* **2020**, *41* (2), 244−247.
(43) Keithley. Models 2400, 2401, 2400-LV and 2400-C SourceMeter Specifications. https://www.tek.com/en/documents/specification/models-2400-2401-2400-lv-and-2400-c-sourcemeter-specifications (accessed 2024-06-10).
(44) Kasl, C.; Hoch, M. J. R. Effects of Sample Thickness on the van Der Pauw Technique for Resistivity Measurements. *Rev. Sci. Instrum.* **2005**, *76* (3), 033907.
(45) Richards, T. J.; Sirringhaus, H. Analysis of the Contact Resistance in Staggered, Top-Gate Organic Field-Effect Transistors. *J. Appl. Phys.* **2007**, *102* (9), 094510.
(46) Waldrip, M.; Jurchescu, O. D.; Gundlach, D. J.; Bittle, E. G. Contact Resistance in Organic Field-Effect Transistors: Conquering the Barrier. *Adv. Funct. Mater.* **2020**, *30* (20), 1904576.
(47) Kim, C. H.; Bonnassieux, Y.; Horowitz, G. Charge Distribution and Contact Resistance Model for Coplanar Organic Field-Effect Transistors. *IEEE Trans. Electron Devices* **2013**, *60* (1), 280−287.
(48) Luan, S.; Neudeck, G. W. An Experimental Study of the Source/Drain Parasitic Resistance Effects in Amorphous Silicon Thin Film Transistors. *J. Appl. Phys.* **1992**, *72* (2), 766−772.

https://doi.org/10.1021/acsmeasuresciau.4c00034
ACS Meas. Sci. Au 2024, 4, 659−667