



OPEN

Polymer ferroelectric field-effect memory device with SnO channel layer exhibits record hole mobility

J. A. Caraveo-Frescas*, M. A. Khan* & H. N. Alshareef

Materials Science and Engineering, King Abdullah University of Science & Technology (KAUST), Thuwal 23955-6900, Saudi Arabia.

SUBJECT AREAS:
MATERIALS SCIENCE
ELECTRONIC DEVICESReceived
3 February 2014Accepted
23 May 2014Published
10 June 2014Correspondence and
requests for materials
should be addressed to
H.N.A. (husam.
alshareef@kaust.edu.
sa)* These authors
contributed equally to
this work.

Here we report for the first time a hybrid *p*-channel polymer ferroelectric field-effect transistor memory device with record mobility. The memory device, fabricated at 200 °C on both plastic polyimide and glass substrates, uses ferroelectric polymer P(VDF-TrFE) as the gate dielectric and transparent *p*-type oxide (SnO) as the active channel layer. A record mobility of 3.3 cm²V⁻¹s⁻¹, large memory window (~16 V), low read voltages (~−1 V), and excellent retention characteristics up to 5000 sec have been achieved. The mobility achieved in our devices is over 10 times higher than previously reported polymer ferroelectric field-effect transistor memory with *p*-type channel. This demonstration opens the door for the development of non-volatile memory devices based on dual channel for emerging transparent and flexible electronic devices.

With the projected growth in the flexible electronics industry, there is renewed interest in the research community to develop high performance polymeric memory, which can be an essential component of many flexible electronic circuits. Some of the efforts in polymer memories are based on different mechanisms such as filamentary conduction, charge trapping effects, dipole alignment, and reduction-oxidation to name a few. One promising flexible memory technology is based on the principle of ferroelectricity. Polymer ferroelectric memories are attractive due to their non-volatility, transparency, low processing temperature, sufficiently large spontaneous polarization, and excellent chemical stability^{1–3}. Among the polymer ferroelectric materials, Poly(vinylidene fluoride) [P(VDF)] and its copolymer with trifluoroethylene [P(VDF-TrFE)] are the most widely used materials due to their many attractive features^{1,4}.

Ferroelectric capacitors make use of the hysteresis property of the polarization by associating the +Pr and −Pr states to Boolean 1 and 0 logic states. The problem with memories based on using ferroelectric capacitors is that they suffer from destructive data read-out, as the voltage applied to read the memory state of the device reverses the polarization state of the ferroelectric. Ferroelectric field-effect transistor (FeFET) memories solve this problem because they can be read out non-destructively. During the read operation, a small drain voltage is applied to measure channel conductance without the need to switch polarization state in the active ferroelectric material.

Almost all previous reports on organic FeFETs use the small molecule, *p*-type semiconductor pentacene^{2,5} (please see Table S1 in supplementary information). As noted by several authors, combining pentacene with P(VDF-TrFE) is problematic due to the high surface roughness of the P(VDF-TrFE) thin films³. It is very difficult to avoid this interface roughness problem by reversing the layer order, i.e., by depositing the P(VDF-TrFE) on top of the pentacene. The organic solvents that are required for the deposition of P(VDF-TrFE) onto pentacene are known to be detrimental to the pentacene surface. As a result, the reported mobilities are relatively low. The highest mobility attained thus far in pentacene/P(VDF-TrFE) based FeFETs is about 0.1 cm²V⁻¹s⁻¹^{16–8}. Similarly, even upon using other *p*-type polymeric semiconductors like MEH-PPV⁹, TIPS pentacene¹⁰, and rr-P3HT¹¹ the mobility in FeFETs is usually well below 1 cm²V⁻¹s⁻¹, with a maximum mobility 0.29 cm²V⁻¹s⁻¹ when *p*-type TIPS pentacene is used as channel semiconductor¹⁰. On the other hand, reports on FeFETs based on P(VDF-TrFE) with *n*-type organic semiconductor are very scarce due to the lack of robust high mobility *n*-type organic semiconductors.

To solve the problem of low mobility in *p*-type and *n*-type FeFETs, the community has adopted an alternate approach. Hybrid organic–inorganic nonvolatile ferroelectric thin-film transistor (FeFET) memories were investigated. In these hybrid devices, the polymeric ferroelectric P(VDF-TrFE) is used as gate dielectric, and an inorganic (oxide) channel semiconductor is used as channel layer^{17,12}. This seems to be a good option, as oxide



channel TFTs have gained legitimacy for use in active matrix (AM) backplanes of liquid-crystal displays (LCD) and in organic light-emitting diode (OLED) display applications¹³. It has been shown that TFTs employing oxide semiconductor channels exhibit several beneficial features such as high field-effect mobility, excellent uniformity, robust device stability, transparency and low temperature deposition possibility on plastic substrates for flexible electronic applications^{14,15}. However, most reports on hybrid (organic-inorganic) ferroelectric field effect memories have exclusively focused on *n*-type oxide semiconductors¹. This effort resulted in promising results, with field effect mobility $>30 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ reported in hybrid FeFET memories on both rigid and flexible devices using semiconducting ZnO as the thin film channel material and P(VDF-TrFE) ferroelectric gate dielectric^{12,16}, and $\sim 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ in fully flexible FeFETs using amorphous indium gallium zinc oxide (a-IGZO)¹⁷.

In contrast, there have been no similar reports on hybrid FeFET memory where *p*-type oxide semiconductor channel film is used with P(VDF-TrFE) ferroelectric gate dielectric. The main reason for this lack of reports on hybrid *p*-type FeFETs is the challenge of making *p*-type oxide semiconductors with sufficiently high mobility. From an applications point of view, however, complementary metal oxide semiconductor (CMOS) logic can offer important advantages when compared with unipolar logic. These include low power consumption and dissipation, higher operating frequencies, good noise margin, and more circuit functionality. A ferroelectric CMOS device is attractive because it can act both as logic and memory element in circuits where low power consumption is critical¹⁸. Takahashi et al.¹⁸ have demonstrated a Si-based ferroelectric CMOS device which performs both logic and memory functions based on the operating voltage. This Si-based device is not suitable for flexible and transparent electronics applications. Thus, having a transparent *p*-type semiconductor can enable the use of ferroelectric CMOS devices in flexible and transparent electronics, which provides both logic and memory functions depending on the operation voltage. At low operation voltages (where no significant hysteresis is achieved) the FeFET behaves as a transistor that can therefore be used for logic operations. At high operating voltages (where hysteresis is present), the device can be used for memory applications. Secondly, *p*-type materials have been demonstrated to be useful as active elements for sensing applications^{19,20}; therefore, it is advantageous from a fabrication point of view to use the same material (SnO in our case) for both the sensing transistor and the memory that is often needed to along with the sensor element.

Stannous oxide (SnO) and cuprous oxide (Cu₂O) have been recently shown as promising transparent *p*-type oxide semiconductors and were used for the fabrication of TFTs by different methods^{21–29}. Transparent and flexible TFTs based on SnO processed at low temperatures (180°C) have been already demonstrated by our group exhibiting record mobility³⁰. The *p*-type character of SnO originates from the Sn²⁺ vacancies while its high hole mobility is attributed to the hybridized Sn 5s and O 2p orbitals near the valence band maxima^{31–33}. With an optical band gap, E_G , ~ 2.7 to 2.9 eV ^{28–30,32} (compared to $E_G \sim 2.1$ of Cu₂O)^{23,24} and a demonstrated field effect mobility as high as $6.75 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ by our group, SnO is becoming a more worthwhile candidate *p*-type semiconductor material in the emerging field of transparent electronics³⁰.

In this study, we present a novel hybrid FeFETs memory device in which P(VDF-TrFE) is used as the gate dielectric and *p*-type SnO is used as the semiconducting channel. To the best of our knowledge, this is the first report of *p*-type oxide channel/polymer ferroelectric FeFET memory device. We have fabricated the memory devices at low temperatures ($\sim 200^\circ\text{C}$) on both rigid and flexible substrates. Our devices show very high mobility ($\sim 3.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), large memory window ($\sim 16 \text{ V}$), relatively low SS ($\sim -4 \text{ Vdec}^{-1}$), low read voltages ($\sim -1 \text{ V}$), and excellent retention characteristics up to 5000 sec. Our hybrid devices show mobility, which is 10 times higher

than previous reports on all organic *p*-type FeFETs. As we will discuss throughout the manuscript, many processing challenges had to be overcome to make functional *p*-type SnO/P(VDF-TrFE) FeFET devices and to optimize their performance.

Results and discussion

Figure 1a and 1b show the conceptual design of the top gate/top contact FeFETs on the flexible and rigid substrates, respectively. Bottom gate devices could not be fabricated, as the sputtering process and annealing process required for the SnO channel layer would damage the ferroelectric polymer. The active channel was a 30 nm thick *p*-type SnO semiconductor layer deposited by sputtering, and patterned by optical lithography. The source and drain contacts were then deposited by thermal evaporation using 10 nm Ti/40 nm Au thin films. A 300 nm thick global layer of ferroelectric P(VDF-TrFE) was then deposited by spin-coating over the entire substrate. Finally, 80 nm thick aluminum metal was thermally evaporated and patterned to form the top gate of the ferroelectric transistor memory. The entire fabrication process was carried out at the low temperature of 200°C , which is compatible with flexible substrates. Many facets of the fabrication process were actually quite challenging. For example, several of the solvents we used for the ferroelectric polymer deposition chemically attacked (etched) the SnO film. Thus, we had to test a few solvents to identify the optimum one to use for best device performance. In addition, we could not use acetone to remove the photoresist after patterning the devices, nor could we use oxygen plasma, as both attacked the ferroelectric polymer. Instead, methanol had to be used and the entire lift-off process was developed and optimized. The details of the fabrication steps are described in the methods section of the manuscript. Figure 1c shows the transmission spectra of the bare glass substrate, SnO film on glass, and ferroelectric polymer/SnO/glass, indicating the stack has reasonably good transparency.

Figure 1d shows a cross-sectional transmission electron microscopy (TEM) image of the rigid device focusing on the semiconductor/ferroelectric interface. It can be seen that the ferroelectric P(VDF-TrFE) polymer grows nicely on the flat surface of SnO without causing any damage to the oxide layer. This good quality interface was realized by using dimethyl-formamide (DMF) as the P(VDF-TrFE) solvent. Other solvents such as Methyl-Ethyl-Ketone (MEK) and cyclohexanone did not work so well with SnO. The inset in Fig. 1d shows a Zygo optical profilometer scan illustrating the device and contact pad regions.

The ferroelectric properties of P(VDF-TrFE) were characterized by measuring a capacitor with similar thickness of the film used in the FeFETs with Au (bottom) and Al (top) electrodes, as used for the source/drain and gate electrodes in our FeFETs respectively. The films were annealed at 130°C for 2 hours identical to our FeFETs. The remnant polarization was measured to be $\sim 7.1 \mu\text{Ccm}^{-2}$ and with coercive fields $\sim 55 \text{ MVm}^{-1}$ (Figure S1). Hall effect measurements were performed at room temperature in greek-cross patterned, 150 nm thick, SnO thin films with the Van der Pauw configuration yielding a Hall mobility of $18.71 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, carrier density of $2.18 \times 10^{17} \text{ cm}^{-3}$ and conductivity of 0.656 Scm^{-1} .

Figure 2 shows the static characteristics of the rigid and flexible devices with a width-to-length ratio (W/L) of 10 and a channel length of 100 μm . Clear linear and saturation regions can be observed in the output characteristics shown in Fig. 2a and 2b for the rigid and flexible devices, respectively. The absence of current crowding at low source-to-drain voltage (V_{DS}) indicates a good Ohmic contact between the SnO and the source and drain electrodes. Figures 2c and 2d show the transfer characteristics measured in the linear region at $V_{\text{DS}} = -1 \text{ V}$. The *p*-type conduction is observed for both devices since holes are accumulated when a negative gate voltage (V_{GS}) is applied. The arrows in the transfer characteristics show clockwise hysteresis of the drain current (I_{DS}), which is a signature of the

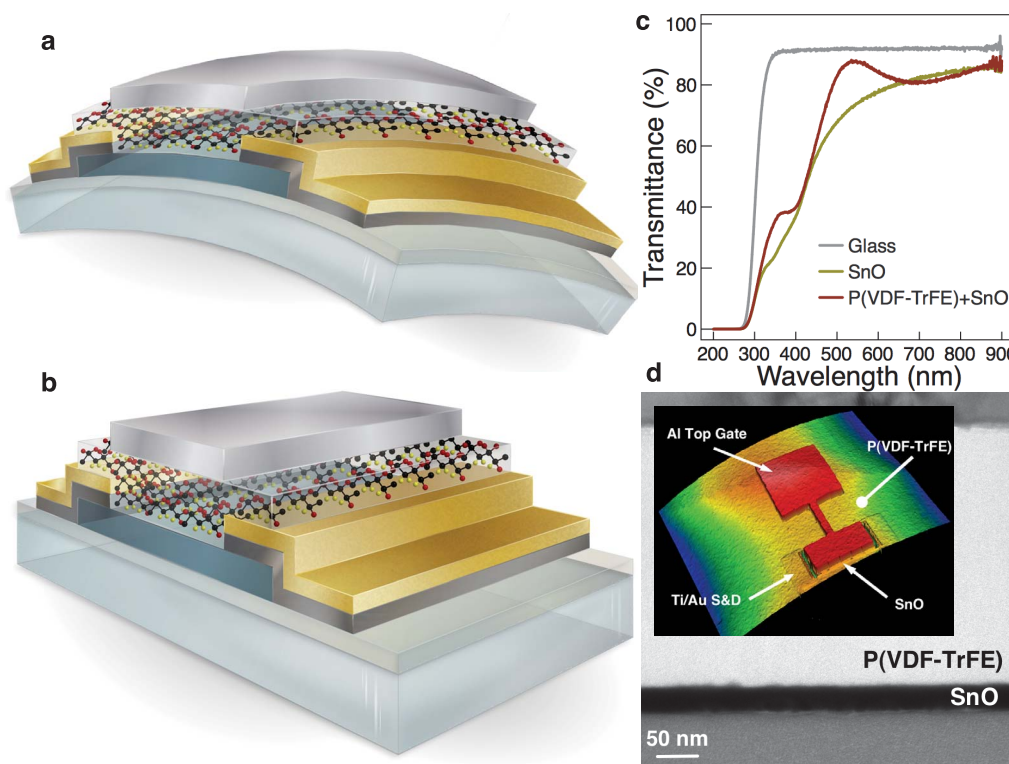


Figure 1 | **Conceptual design of the devices.** (a), polyimide substrate; (b), glass substrate: the following layers make up the device stack (from bottom to top): substrate, 200 nm Si₃N₄ layer, 30 nm SnO active layer, 10 nm Ti/40 nm Au source and drain contacts, 300 nm P(VDF-TrFE) ferroelectric layer and 80 nm Al top gate; (c), optical transmission characteristics of the glass substrate, SnO/glass, and P(VDF-TrFE)/glass, and (d), TEM image showing cross section of the SnO/P(VDF-TrFE) interface, and optical profilometer scan (inset) showing the major parts of the device.

ferroelectric polarization in these ferroelectric field-effect devices⁸. Field effect mobilities (μ_{FE}), calculated in the linear regime, were $3.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $2.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for the rigid and flexible devices, respectively. To our knowledge, these are the highest mobility values reported for *p*-type ferroelectric transistor memory device, and are over 10 times higher than previously reported FeFETs based on *p*-type organic semiconductors^{6–8}. On-to-off current ratio (I_{ON}/I_{OFF}) measured at $V_{GS} = 0 \text{ V}$ was found to be around 10^2 and is mainly limited by the relatively high gate current (I_C) of 10^{-8} amps, which seriously impacts the FeFETs off current and need to be improved. On the other hand, subthreshold swing (SS) of 4 V dec^{-1} is obtained, which is lower than reported SnO TFTs using a high-*k* oxide gate dielectric^{25,30}. A memory window, calculated from the shift in the on voltage (V_{ON}) of the negative-going scan (accumulation mode) and the positive-going scan (depletion mode) of 16 V is observed for FeFETs on both substrates.

The memory window in a FeFET is a function of the thickness of ferroelectric layer as well as the gate bias applied. We see that for a field of 100 MV/m applied to the gate electrode in our FeFETs we get a memory window of $\sim 16 \text{ V}$. Upon application of a similar bias field to the ferroelectric capacitor we get a coercive field of $E_c \sim 45 \text{ MV/m}$. Therefore ideally we expect the total memory window to be $\sim 27 \text{ V}$ for a 300 nm thick P(VDF-TrFE) film which is much higher than the actual memory window we get in our FeFETs. This difference has been previously studied for hybrid FeFETs using oxide semiconductors. The lower memory window has been attributed to accumulation/depletion operation of the oxide semiconductor³⁴. In the off state, the SnO channel is in a fully or partially depleted state and acts as an insulating layer, therefore, the voltage applied to the gate electrode is distributed with the capacitance coupling. In the on state, the induced charge density at the surface of the semiconductor is much smaller than the ferroelectric Pr, as a consequence of the relatively low initial carrier concentration in the semiconductor

(10^{17} cm^{-3}). Therefore, the memory window of FeFETs with oxide semiconductors is highly dependent in the semiconductor thickness and initial carrier concentration.

Figure 3 shows the material characterization of both the SnO active layer as well as the ferroelectric P(VDF-TrFE) layer. Figure 3a shows the x-ray diffraction (XRD) pattern of SnO where mixed phase tin monoxide is shown. It has been previously demonstrated that the presence of metallic phase in a SnO matrix enhances mobility by promoting orbital delocalization in the valence band of SnO^{30,33}. We have used our previously optimized deposition conditions of SnO, where the highest mobility occurs, to fabricate the FeFETs devices. The deposition conditions where maximum mobility is observed were found to be at a deposition pressure of 1.8 mTorr and relative oxygen partial pressure (O_{PP}) of 9%, where around 3 at% metallic tin is present³⁰. The SnO film is polycrystalline with an extracted crystallite size of around 12 nm. The grazing incidence (GI) XRD pattern shown in Figure 3b shows the presence of the ferroelectric β phase of P(VDF-TrFE). The peak centered at $2\theta = 19.7^\circ$ is consistent with the (100) and (200) planes yielding an interplanar distance of 4.5 \AA consistent with earlier reports^{35,36}. Figure 3c and 3d show the $2 \mu\text{m} \times 2 \mu\text{m}$ atomic force microscope (AFM) phase diagrams of SnO and P(VDF-TrFE) layers respectively, deposited on the rigid substrate. The SnO films show very smooth surfaces with a root mean square roughness of $\sim 1.4 \text{ nm}$. It's very critical to have a smooth interface to achieve high mobility devices. Previous report on bottom gate polymer FeFETs have reported poor mobility of the charge carriers due to the high surface roughness of P(VDF-TrFE) thin films^{2,3}. Inverting the stack by fabricating top gate devices can help but it is difficult to fabricate in all-polymer structures. This is because the solvent used for spin coating P(VDF-TrFE) can be detrimental to many organic semiconductors³. This can be solved using hybrid organic/inorganic structures for achieving high mobility in FeFETs¹. P(VDF-TrFE) grows nicely on the relatively flat SnO

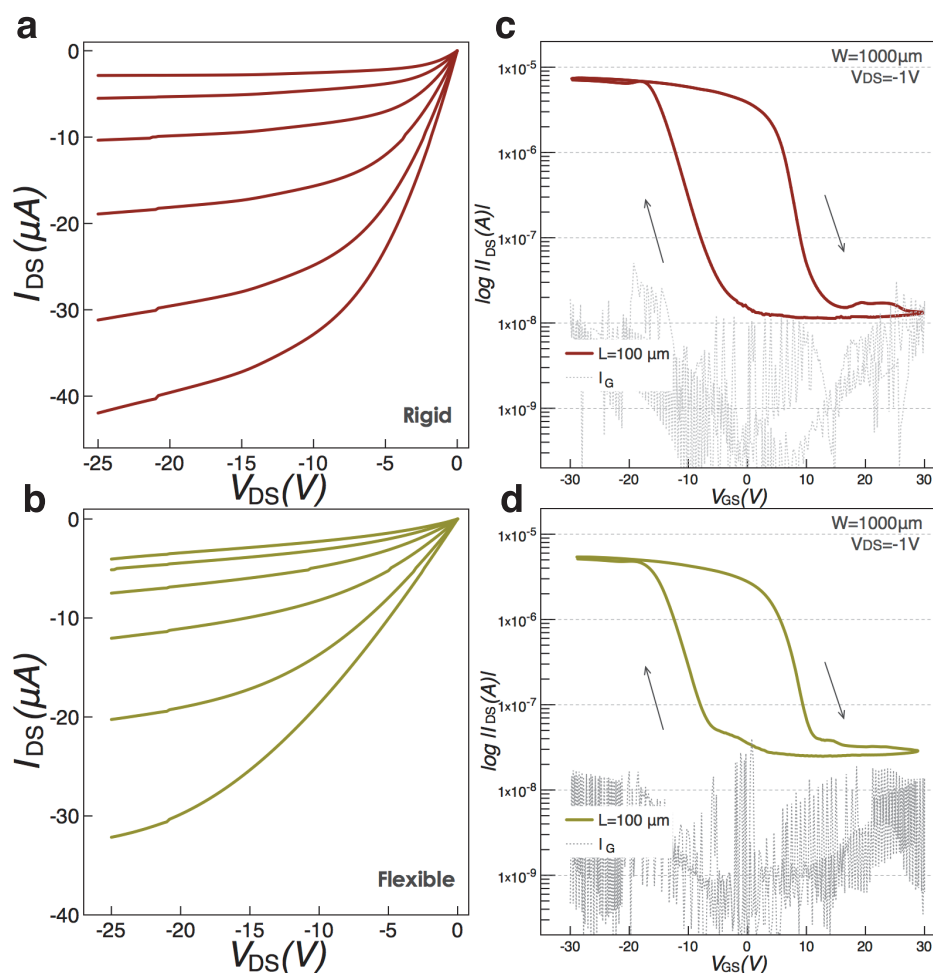


Figure 2 | FeFET static characteristics. Output characteristics from $V_{GS} = 0$ V to -15 V at -3 V steps of (a), glass substrate; (b), flexible substrate; Transfer characteristics at $V_{DS} = -1$ V of (c), rigid device; (d), flexible device.

surface (rms surface roughness ~ 6.18 nm) with an average grain size of ~ 160 nm, which can be clearly observed on the AFM image, consistent with our earlier reports³⁷. The large grains are important to get maximum polarization from the ferroelectric layer. Flexible devices show a higher surface roughness of ~ 9.77 nm, mainly due to the higher substrate roughness of the polyimide when compared to glass. This difference in the surface roughness is of particular importance when comparing devices on both substrates, as it is known that large surface roughness degrades the FeFET performance^{2,3,6}.

Table 1 summarizes the important transistor parameters of devices with W/L ratios of 10, 5 and 2 on both rigid and flexible devices. Comparable performance is observed for the devices regardless of the channel dimensions. Furthermore, several measurements were performed on each device type, and reproducible behavior was observed (statistical analysis shown in Table S2). It can be seen that rigid devices exhibit higher mobility and I_{ON}/I_{OFF} . From the transfer characteristics in Figure 2, a higher I_G can be observed for the flexible devices, which in turn increases the device off current. We surmise that carrier scattering arising from higher surface roughness in the case of flexible devices (plastic substrate) is the reason for the lower device performance when compared to the rigid ones (glass substrates). The higher surface roughness also makes the spin coating process of the ferroelectric layer less uniform, giving rise to a higher probability of leakage paths due to a non-uniform electric field distribution. The use of an interfacial layer might be required to help decrease the gate current, as it has been demonstrated when using *n*-type oxide semiconductors^{38,39}. Device resistance to mechanical deformation has been analyzed for the flexible sample with an

approximate bending radius of 10 mm. No significant degradation of the FeFET performance has been observed up to 100 cycles and around 20% decrease in the mobility after 200 cycles, as shown in the transfer curves of Fig. S3.

From a memory point of view, data retention characteristics are of paramount importance. Figure 4a and 4b shows the retention characteristics obtained by measuring the remnant I_{DS} as a function of time for rigid and flexible devices, respectively. The ON/OFF states were produced at gate voltages of $-30/+30$ V with a 1 sec pulse and the retention was measured at zero gate bias condition. Relatively good retention characteristics are observed for these devices, as they keep an I_{ON}/I_{OFF} of around two orders of magnitude even after 5000 seconds. The relatively low drain voltage required to read the current in these oxide channel semiconductors compared to the organic counterparts, does not disturb the polarization state of the ferroelectric dielectric. Thus, these hybrid memory devices can have excellent retention characteristics. Better retention characteristics and lower leakage current is observed for rigid devices. We surmise the higher leakage current and somewhat degraded retention characteristics of the flexible devices is due to higher non-uniform thickness of the ferroelectric layer in the flexible devices as a result of the accumulated surface roughness.

Conclusions

We have demonstrated the first ferroelectric polymer field effect transistor memory using *p*-channel oxide semiconductor (SnO) on both rigid and flexible substrates with record mobilities. The top-gated devices exhibit a field effect mobility of $3.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$

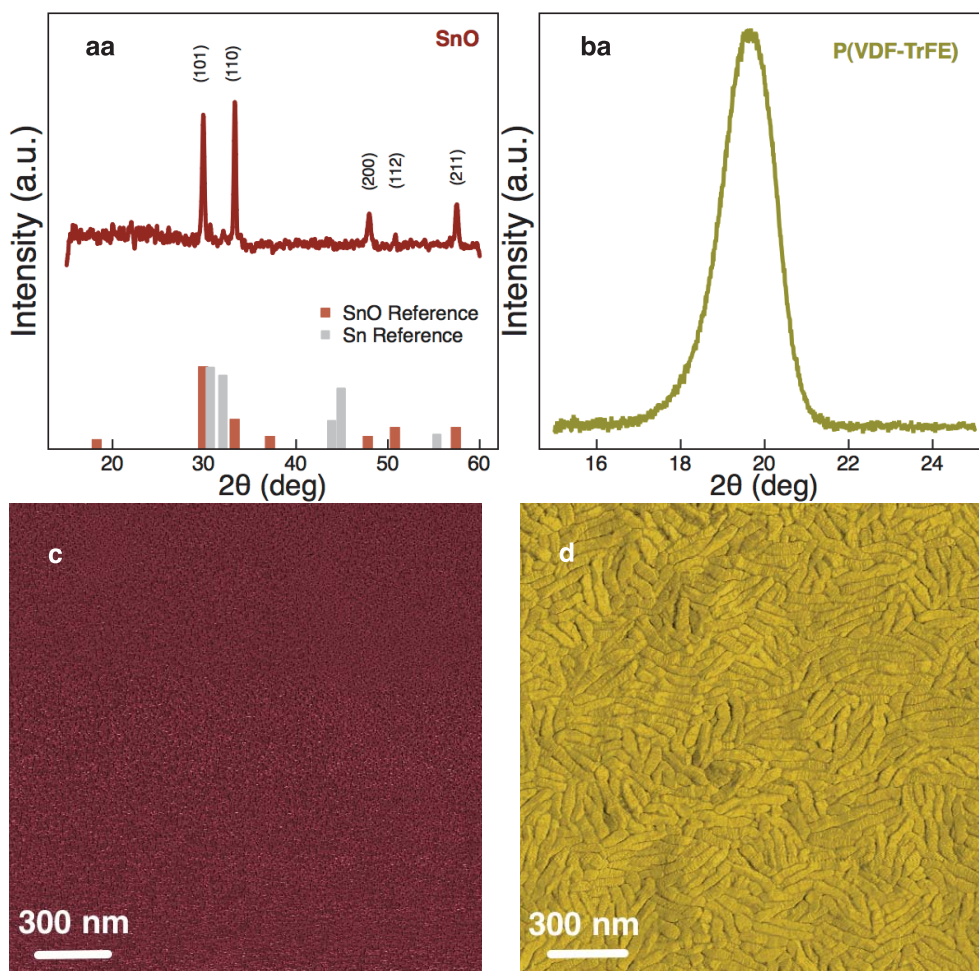


Figure 3 | Materials Characterization. (a), XRD pattern of SnO thin films. The lines at the bottom show the diffraction patterns of tetragonal SnO (JCPDS card No. 06-0395) and tetragonal Sn (JCPDS card No. 04-0673); (b), GIXRD pattern of P(VDF-TrFE) layer showing the dominant reflection corresponds to the ferroelectric β phase; (c), AFM image of the SnO surface. The SnO films show very smooth surfaces with a root mean square roughness of ~ 1.8 nm; (d), AFM image of the P(VDF-TrFE) surface morphology, with an average grain size of ~ 160 nm.

and $2.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ on the rigid and flexible substrates, respectively. This is a 10-fold increase over the best reported all-organic *p*-channel ferroelectric field-effect transistor memories. Furthermore, a high

memory window of 16 V has been achieved along with excellent retention characteristics of more than 5000 seconds.

Methods

The top gate structure was fabricated in a rigid glass substrate and a flexible polyimide films. In order to decrease the surface roughness of the polyimide film a 200 nm thick Si_3N_4 layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The SnO active layer was deposited by DC reactive magnetron sputtering from a $2''$ metal target, at room temperature, at a deposition pressure of 1.8 mTorr, relative oxygen partial pressure of 9%, and power density of $9.55 \text{ W}/\text{in}^2$. Source and drain electrodes (10 nm Ti, 40 nm Au) were electron-beam evaporated. The stack was annealed at 200°C after source and drain deposition in order to crystallize the SnO active layer. P(VDF-TrFE) copolymer (70–30 mol%) powder was dissolved in Dimethyl Formamide (DMF) to get a 4 wt.% solution. The filtered solution was then spun on the SnO film at 4000 rpm for 60 s followed by a soft bake for 30 min at 80°C . The films were then annealed in vacuum at 130°C for 2 h to improve the crystallinity. The resulting P(VDF-TrFE) film thickness was approx. ~ 300 nm. Aluminum top gate electrodes were thermally evaporated to complete the stack. Layers of the device were patterned by conventional photolithography technique and lift-off process. In order to prevent damage to the ferroelectric layer, methanol was used for lift-off. Devices were measured on a probe station at ambient conditions, in the dark, using a Keithley 4200 semiconductor parameter analyzer. The performance of the FeTFTs was evaluated from devices with width-to-length (W/L) ratios ranging from 2 to 10 at a fixed width $W = 1000 \mu\text{m}$. Field-effect mobility (μ_{FE}) was extracted using the conventional metal-oxide-semiconductor field-effect transistor model described in equation 1, by the transconductance, g_m , in the linear regime according to equation 2.

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ for } V_{DS} < V_{GS} - V_T \quad (1)$$

where C_{ox} is the capacitance per unit area of the gate insulator

Table 1 | Important transistor parameters for devices fabricated on both rigid and flexible substrates for three different W/L ratios. Threshold voltage extracted from the accumulation mode operation (negative-going scan)

W = 1000 μm	L (μm)		
	100	200	500
Rigid Substrate			
Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	3.30	3.24	3.28
Threshold Voltage (V)	-11.6	-11.6	-11.6
I_{ON}/I_{OFF}	2.51×10^2	2.40×10^2	2.62×10^2
SS (Vdec^{-1})	4.29	4.33	4.35
Memory Window (V)	15.9	16.1	16.3
	L (μm)		
	100	200	500
Flexible Substrate			
Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	2.53	2.48	2.51
Threshold Voltage (V)	-11.7	-11.8	-11.7
I_{ON}/I_{OFF}	0.94×10^2	0.92×10^2	0.90×10^2
SS (Vdec^{-1})	4.35	4.42	4.49
Memory Window (V)	16.3	14.2	14.6

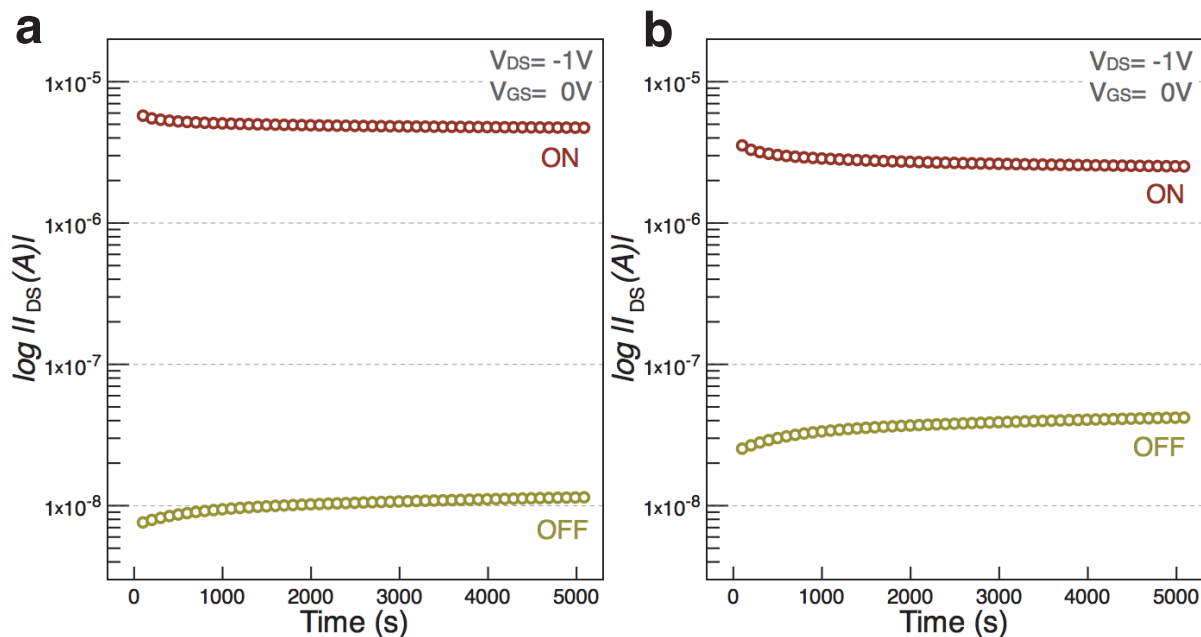


Figure 4 | Retention characteristics. (a), rigid device; (b), flexible device. The ON/OFF states were produced at gate voltages of $-30/+30$ V with a 1 sec pulse and the retention was measured at zero gate bias condition.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \approx \frac{W\mu_{FE}C_{ox}}{L} V_{DS} \quad (2)$$

The subthreshold swing (SS) was calculated by the inverse of the maximum slope of the transfer characteristics in the subthreshold region according to equation 3.

$$SS = \left(\frac{d(\log I_{DS})}{dV_{GS}} \Big|_{max} \right)^{-1} = \frac{\ln(10)nkT}{q} \quad (3)$$

The capacitance density of the ferroelectric layer was measured by the well-known parallel plate capacitor method using Ti/Au as the bottom electrode and Al as top electrode for consistency, yielding a $C_{ox} = 40$ nF cm $^{-2}$ at a frequency of 100 Hz. The on-to-off current ratio was calculated at $V_{GS} = 0$ V and the memory window as the difference in the on voltage of the positive-going and negative-going scans. The film thicknesses were measured using a Veeco Dektak 150 surface profilometer and confirmed by cross-sectional transmission electron microscopy (TEM) analysis performed with a FEI Titan ST. High-resolution X-ray diffraction patterns were obtained at room temperature in air by a Bruker D8 Discover diffractometer using the $\text{CuK}\alpha_1$ (1.5406 Å) radiation. Surface morphologies were imaged by an Agilent 5400 SPM AFM system.

1. Yoon, S.-M. *et al.* Nonvolatile memory thin-film transistors using an organic ferroelectric gate insulator and an oxide semiconducting channel. *Semicond. Sci. Technol.* **26**, 034007+034025 (2011).
2. Park, Y. J., Bae, I.-S., Kang, S. J., Chang, J. & Park, C. Control of Thin Ferroelectric Polymer Films for Non-volatile Memory Applications. *IEEE. T. DIELECT. EL. IN.* **17**, 1135–1163 (2010).
3. Naber, R. C. G., Asadi, K., Blom, P. W. M., Leeuw, D. M. D. & Boer, B. D. Organic Nonvolatile Memory Devices Based on Ferroelectricity. *Adv. Mater.* **22**, 933–945 (2010).
4. Ling, Q.-D. *et al.* Polymer electronic memories: Materials, devices and mechanisms. *Prog. Polym. Sci.* **33**, 917–978 (2008).
5. Naber, R. C. G., Asadi, K., Blom, P. W. M., Leeuw, D. M. D. & Boer, B. D. Organic Nonvolatile Memory Devices Based on Ferroelectricity. *Adv. Mater.* **22**, 933–945 (2010).
6. Khan, M. A., Bhansali, U. S. & Alshareef, H. N. High-Performance Non-Volatile Organic Ferroelectric Memory on Banknotes. *Adv. Mater.* **24**, 2165–2170 (2012).
7. Lee, K. H. *et al.* High-Mobility Nonvolatile Memory Thin-Film Transistors with a Ferroelectric Polymer Interfacing ZnO and Pentacene Channels. *Adv. Mater.* **21**, 4287–4291 (2009).
8. Nguyen, C. A., Mhaisalkar, S. G., Ma, J. & Lee, P. S. Enhanced organic ferroelectric field effect transistor characteristics with strained poly(vinylidene fluoride-trifluoroethylene) dielectric. *Org. Electron.* **9**, 1087–1092 (2008).
9. Naber, R. C. G. *et al.* High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Mater.* **4**, 243–248 (2005).
10. Kang, S. J. *et al.* Non-volatile Ferroelectric Poly(vinylidene fluoride-co-trifluoroethylene) Memory Based on a Single-Crystalline Tri-isopropylsilylethynyl Pentacene Field-Effect Transistor. *Adv. Mater.* **19**, 1609–1616 (2009).
11. Naber, R. C., Boer, B. D., Blom, P. W. & Leeuw, D. M. D. Low-voltage polymer field-effect transistors for nonvolatile memories. *Appl. Phys. Lett.* **87**, 2035509 (2005).
12. Yoon, S.-M. *et al.* Fully Transparent Non-volatile Memory Thin-Film Transistors Using an Organic Ferroelectric and Oxide Semiconductor Below 200°C. *Adv. Funct. Mater.* **20**, 921–926 (2010).
13. Ginley, D. S., Hosono, H. & Paine, D. C. *Handbook of Transparent Conductors* (Springer, 2010).
14. Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **24**, 2945–2986 (2012).
15. Wong, W. S. & Salleo, A. *Flexible Electronics: Materials and Applications*. (Springer, 2009).
16. Yoon, S.-M., Yang, S. & Park, S.-H. K. Flexible Nonvolatile Memory Thin-Film Transistor Using Ferroelectric Copolymer Gate Insulator and Oxide Semiconducting Channel. *J. Electrochem. Soc.* **158**, H892–H896 (2011).
17. Lee, G.-G. *et al.* The flexible non-volatile memory devices using oxide semiconductors and ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene). *Appl. Phys. Lett.* **99**, 012901–012903 (2011).
18. Takahashi, M. *et al.* Basic operation of novel ferroelectric CMOS circuits. *Electron. Lett.* **44**, (2008).
19. Korotcenkov, G. Metal oxides for solid-state gas sensors: What determines our choice? *Mater. Sci. Eng. B* **139**, 1–23 (2007).
20. Batzill, M. & Diebold, U. The surface and materials science of tin oxide. *Prog. Surf. Sci.* **79**, 47–154 (2005).
21. Yao, Z. Q. *et al.* Room temperature fabrication of p-channel Cu[sub 2]O thin-film transistors on flexible polyethylene terephthalate substrates. *Appl. Phys. Lett.* **101**, 042114 (2012).
22. Zou, X. *et al.* Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-k HfON Gate Dielectric. *Electron Devic. Lett.* **31**, 827–829 (2010).
23. Matsuzaki, K. *et al.* Epitaxial growth of high mobility Cu[sub 2]O thin films and application to p-channel thin film transistor. *Appl. Phys. Lett.* **93**, 202107 (2008).
24. Fortunato, E. *et al.* Thin-film transistors based on p-type Cu[sub 2]O thin films produced at room temperature. *Appl. Phys. Lett.* **96**, 192102 (2010).
25. Fortunato, E. *et al.* Transparent p-type SnO[sub x] thin film transistors produced by reactive rf magnetron sputtering followed by low temperature annealing. *Appl. Phys. Lett.* **97**, 052105–052103 (2010).
26. Lee, H.-N., Kim, H.-J. & Kim, C.-K. p-Channel Tin Monoxide Thin Film Transistor Fabricated by Vacuum Thermal Evaporation. *Jpn. J. Appl. Phys.* **49**, 020202 (2010).
27. Liang, J. Y. *et al.* The structural, optical and electrical properties of Y-doped SnO thin films and their p-type TFT application. *J. Phys. D: Appl. Phys.* **45**, 085101 (2012).
28. Ogo, Y. *et al.* p-channel thin-film transistor using p-type oxide semiconductor, SnO. *Appl. Phys. Lett.* **93**, 032113 (2008).



29. Yabuta, H. *et al.* Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits. *Appl. Phys. Lett.* **97**, 072111 (2010).
30. Caraveo-Frescas, J. A. *et al.* Record Mobility in Transparent p-Type Tin Monoxide Films and Devices by Phase Engineering. *ACS Nano* **7**, 5160–5167 (2013).
31. Togo, A., Oba, F., Tanaka, I. & Tatsumi, K. First-principles calculations of native defects in tin monoxide. *Phys. Rev. B* **74**, 195128 (2006).
32. Ogo, Y. *et al.* Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application. *Phys. Status Solidi A* **206**, 2187–2191 (2009).
33. Granato, D. B., Caraveo-Frescas, J. A., Alshareef, H. N. & Schwingenschlöggl, U. Enhancement of p-type mobility in tin monoxide by native defects. *Appl. Phys. Lett.* **102**, 212105–212105–212104 (2013).
34. Yoon, S.-M. *et al.* Nonvolatile memory transistors using solution-processed zinc-tin oxide and ferroelectric poly(vinylidene fluoride-trifluoroethylene). *Org. Electron.* **11**, 1746–1752 (2010).
35. Bhansali, U. S., Khan, M. A. & Alshareef, H. N. Electrical performance of polymer ferroelectric capacitors fabricated on plastic substrate using transparent electrodes. *Org. Electron.* **13**, 1541–1545 (2012).
36. Mao, D., Quevedo-Lopez, M. A., Stiegler, H., Gnade, B. E. & Alshareef, H. N. Optimization of poly(vinylidene fluoride-trifluoroethylene) films as non-volatile memory for flexible electronics. *Org. Electron.* **11**, 925–932 (2010).
37. Khan, M. A., Bhansali, U. S., Cha, D. & Alshareef, H. N. All-Polymer Bistable Resistive Memory Device Based on Nanoscale Phase-Separated PCBM-Ferroelectric Blends. *Adv. Funct. Mater.* **23**, 2145–2152 (2013).
38. Park, C. H., Lee, K. H., Lee, B. H., Sung, M. M. & Im, S. Channel/ferroelectric interface modification in ZnO non-volatile memory TFT with P(VDF-TrFE) polymer. *J. Mater. Chem.* **20**, 2638–2643 (2010).
39. Yoon, S. M. *et al.* Impact of interface controlling layer of Al_2O_3 for improving the retention behaviors of In-Ga-Zn

oxide-based ferroelectric memory transistor. *Appl. Phys. Lett.* **96**, 232903 (2010).

Acknowledgments

Research reported in this publication was supported by King Abdullah University of Science and Technology (KAUST). The authors thank Qingxiao Wang for the TEM imaging.

Author contributions

J.C., M.K. and H.A. designed the study. J.C. and M.K. carried out the experiments. All authors analyzed the data and co-wrote the manuscript.

Additional information

Supplementary information accompanies this paper at <http://www.nature.com/scientificreports>

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Caraveo-Frescas, J.A., Khan, M.A. & Alshareef, H.N. Polymer ferroelectric field-effect memory device with sno channel layer exhibits record hole mobility. *Sci. Rep.* **4**, 5243; DOI:10.1038/srep05243 (2014).



This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivs 3.0 Unported License. The images in this article are included in the article's Creative Commons license, unless indicated otherwise in the image credit; if the image is not included under the Creative Commons license, users will need to obtain permission from the license holder in order to reproduce the image. To view a copy of this license, visit <http://creativecommons.org/licenses/by-nc-nd/3.0/>