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Integrated Water-Level Sensor Using Thin-Film Transistor Technology

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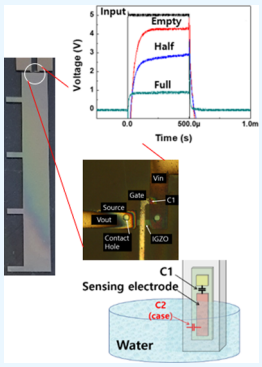
ABSTRACT: A low-cost water-level sensor was developed utilizing a capacitive sensor design with only one thin-film transistor (TFT). The integration of the a-IGZO TFT process facilitated the complete integration of the water-level sensor on a substrate, including essential components, such as the transistor, capacitor, wires, and sensing electrode. This integration eliminates the need for a separate mounting process, resulting in a robust sensor assembly. To comprehensively assess the performance of the developed water-level sensor, rigorous evaluations were conducted using both MOSFET and TFT integration. In the case of the water-level sensor featuring a-IGZO TFT integration, a voltage output of 4.2 V was measured when the tank was empty, while a voltage output of 0.9 V was measured when the tank was full. Notably, the integrated sensor system demonstrated a higher output voltage compared with the MOSFET sensor, primarily due to the significantly reduced parasitic capacitance of the TFT. The use of a-IGZO TFT in the integrated sensor system contributes to enhanced sensitivity and accuracy. The lower parasitic capacitance inherent in TFT technology allows for improved voltage measurement precision, resulting in more reliable and precise water-level sensing capability. The development of this integrated water-level sensor holds immense potential for a wide range of applications that require a combination of cost-effectiveness, accurate monitoring, and flexibility in form factor. With its affordability, the sensor is accessible for various industries and applications.



INTRODUCTION

Flat panel displays (FPDs), such as liquid crystal displays (LCDs) and organic light-emitting diode (OLED) displays, rely heavily on the performance of thin-film transistors (TFTs). These electronic devices function as switches, enabling precise control of the current flow within the display panel, allowing the precise manipulation of individual pixels. Display technology relies on several types of TFTs, each with distinct advantages and disadvantages. Hydrogenated amorphous silicon (a-Si:H), low-temperature polycrystalline silicon (LTPS), and oxide TFTs stand out as prominent and extensively employed TFT technologies in the field. Although a-Si:H TFTs continue to be widely utilized due to their cost-effectiveness, there is a growing preference for oxide and LTPS TFTs. In comparison to a-Si:H TFTs, these advanced technologies present compelling advantages, notably high-resolution displays, fast response times, and improved power efficiency, making them increasingly desirable in a wide range of applications.[1]

In addition to their widespread use in displays, TFTs have found diverse applications in sensors, circuits, and radio frequency identification (RFID) systems.[2−5] TFTs play a critical role in high-performance displays by serving as scan drivers and pixel circuits for the OLED panels. These TFTs are commonly integrated with TFTs on a glass substrate, forming an essential component of the display system.[6,7] Furthermore, TFTs have demonstrated their versatility in the development of diverse sensor types, including photo, fingerprint, temperature, gas, infrared (IR), and ultraviolet (UV) sensors. This is attributable to their compact form factor, energy efficiency, and scalability, making TFTs an ideal choice for sensor applications requiring miniaturization, low power consumption, and adaptability.[8−11] Consequently, the significance of TFTs is steadily rising in the realm of emerging technologies, notably, flexible electronics, medical devices, and wearable technology. Their distinctive properties offer new possibilities for innovation and growth.[12,13]

Water-level sensors play a crucial role in various industrial applications such as bidets, boilers, and tanks, where precise liquid-level measurement is essential for optimal performance. These sensors play a vital role in detecting precise liquid levels, facilitating the timely refilling or utilization of liquid based on the desired level. The precise liquid-level monitoring capability of TFTs facilitates optimal liquid management, mitigating the risks of underutilization or overdraining. This ensures the efficient utilization of liquids by providing accurate real-time

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monitoring, leading to enhanced operational effectiveness and resource conservation.

Despite advancements in the development of water-level sensors, there is still room for improvement, especially given the potential risks associated with the oxidation of the sensor's surface or any materials coated on it, which can cause incorrect behavior. To optimize the utility of water-level sensors, it is imperative to prioritize the advancement of novel technologies aimed at enhancing their accuracy and reliability. Recent advancements in water-level sensors have prompted extensive research into various sensor types for accurate water-level measurement. This includes exploring pressure sensors, optical sensors, resistive sensors, capacitive sensors, and other innovative technologies. The investigation of diverse sensor options aims to enhance the precision and reliability of water-level measurement systems, catering to a wide range of applications.[14−17] It is crucial to note that while accuracy and reliability are essential features of water-level sensors, their development should also prioritize other factors such as cost-effectiveness, ease of use, and durability. A comprehensive approach to sensor development that considers these factors is necessary. To meet the diverse needs of different users, it is imperative to prioritize the development of water-level sensors that exhibit accuracy, reliability, affordability, user-friendliness, and durability.

Among the plethora of sensor options available, the capacitive sensor utilizing TFTs stands out as a superior choice. Unlike optical water-level sensors that can experience reduced accuracy due to dirt or contaminants, capacitive sensors with TFTs remain unaffected by external environmental factors on their surface. This inherent immunity ensures consistent and reliable measurements even under the most challenging conditions. Low power consumption is an advantage of the capacitive water-level sensor compared to active optical sensors, which need continuous illumination. Capacitive sensors do not require direct physical contact with water, which mitigates concerns related to sensor corrosion or fouling commonly experienced with resistive sensors. This noncontact capability ensures consistent and accurate readings over extended periods. One of the most remarkable features of capacitive sensors is their solid-state design, devoid of any mechanical components such as those found in float-level sensors. This absence of moving parts ensures enhanced durability and significantly reduces the risk of sensor failure due to wear and tear.

Water-level measurement methods are commonly classified into two categories: continuous-level measurement, which is utilized for process monitoring, and point-level measurement, which enables alarms or trips to be triggered.[18] Capacitive sensors, which utilize a metal electrode connected to an oscillator circuit, have gained widespread application in water-level detection. In this method, the detected object itself can serve as the next metal electrode in the capacitor, allowing for a simplified setup. However, conventional water sensors often face challenges, such as weak detection signals and the requirement for additional amplifiers. These limitations necessitate the development of advanced sensor technologies to overcome these obstacles and enhance the accuracy and sensitivity of water-level detection systems. To tackle this issue, researchers have presented diverse methodologies in the literature to enhance sensor performance.[19−21]

In traditional electrical sensing systems, soldering is often involved, which can introduce potential points of failure. To enhance the reliability of the module, a solder-free integration approach can be adopted where circuits are seamlessly integrated into the water-level sensor. The integration of sensor devices by TFTs on a substrate provides a solder-free approach, facilitating miniaturization and enabling the amplification of sensing signals. This integration technique empowers the development of compact sensors with improved performance and reliability.[22]

Oxide-based TFTs offer desirable properties for sensing systems, including long-term stability and superior electrical performance when compared with a-Si:H TFTs. Among various oxide TFT types, amorphous indium−gallium−zinc oxide (a-IGZO) TFTs stand out as the most widely utilized oxide semiconducting material. They exhibit well-defined electrical characteristics with high mobility, surpassing a-Si:H TFTs, while also enabling low-temperature processing and cost-effectiveness. These attributes make a-IGZO TFTs highly suitable for application on diverse substrates, including flexible ones, presenting them as promising candidates with favorable properties.[23,24]

This study presents a novel and cost-effective approach to developing a water-level sensor using a-IGZO TFTs. The sensor incorporates all of the necessary components, including capacitance, wiring, amplifying device, and sensing electrodes, on a single substrate without the need for soldering. By eliminating the soldering process, the implementation of the water-level sensor is streamlined, minimizing errors and enhancing reliability. Notably, the proposed sensor-integrated circuit includes a TFT that eliminates the need for an external amplifier, resulting in a reduced noise and improved reliability.

EXPERIMENTS

Device Fabrication. In this study, an IGZO TFT instrument has been developed and integrated on a glass substrate for water-level sensing. The TFT structure employed in this study was a top-gate coplanar structure specifically selected to significantly reduce parasitic capacitance. The cross-sectional view of the fabricated a-IGZO TFTs is illustrated in Figure 1.

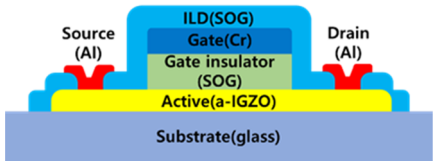

Figure 1. Cross-sectional view of the coplanar structured top-gate a-IGZO TFT used in the water-level sensor.

A 50 nm thick layer of a-IGZO was deposited onto a cleaned glass substrate at room temperature using RF magnetron sputtering, employing an IGZO target with a composition ratio of In/Ga/Zn = 1:1:1 atom %. The deposition process ensured uniform coverage of the a-IGZO layer on the substrate. Subsequently, a photolithography process was employed to pattern the a-IGZO layer, followed by wet etching using a diluted buffered oxide etch (BOE) solution with a ratio of deionized (DI) water to BOE of 500:1. Subsequently, the patterned active layer was annealed at 250 °C for 1 h under an oxygen atmosphere to reduce the oxygen vacancies and process-related defects.

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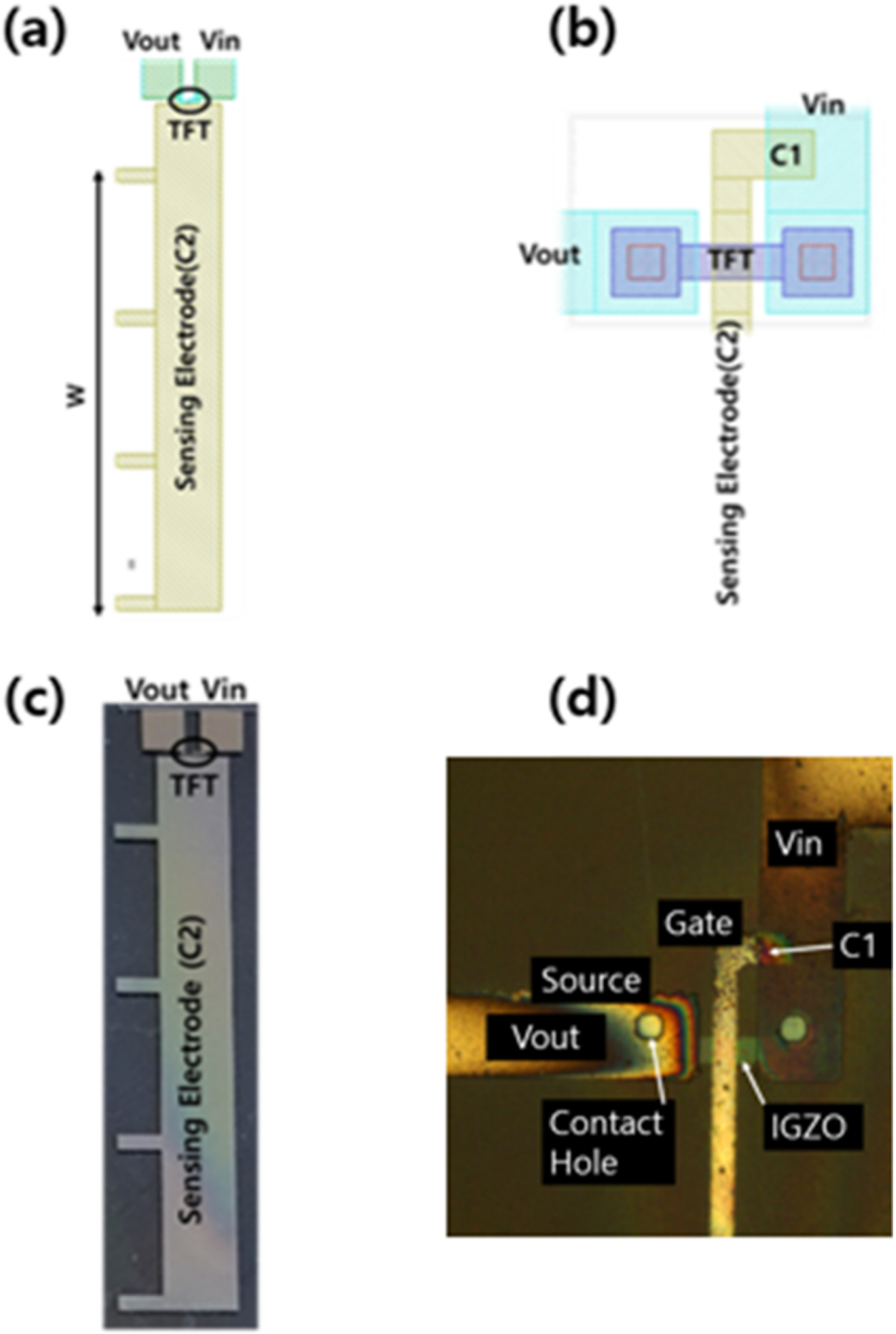

Figure 2. Schematic illustration of the water-level sensor, highlighting the TFT (a), a close-up view of the TFT part (b), the image of the fabricated a-IGZO TFT water-level sensor (c), and magnified view of the a-IGZO TFT of the water-level sensor.

The gate insulator layer was fabricated by applying a spin-on-glass (SOG) solution to the active layer. Following the spin coating process, the layer underwent a prebaking step at 180 °C for 3 min, ensuring the removal of any residual solvents. Subsequently, an annealing process was performed at 450 °C for 1 h, facilitating the formation of a well-structured and robust gate-insulating layer. The optimized parameters for the SOG process were previously reported in our work.[25]

After the SOG gate insulator was fabricated, a gate electrode was created by depositing a chromium (Cr) layer through sputtering. The patterned Cr gate electrode played a role as a protective mask during the subsequent reactive-ion-etching (RIE) process, which precisely removed the excess SOG gate insulator material. The RIE process utilized CF_4 and O_2 gases as etching agents, effectively etching away the SOG gate insulator material that was not protected by the patterned Cr gate electrode.

After patterning of the gate insulator, the areas of the a-IGZO layer that were not covered by the gate electrode became exposed. To increase the carrier density and improve

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ACS Omega 2023, 8, 36868−36875

conductivity in the exposed regions, O_2 plasma treatment was applied for 30 s. During this process, the reactive oxygen ions bombarded the a-IGZO layer, inducing the controlled formation of defects. These defects played a crucial role in increasing the carrier density and reducing the resistivity of the a-IGZO layer. By selectively treating the exposed parts of the a-IGZO layer, we achieved a more optimized and efficient performance of the a-IGZO TFT.

In the subsequent step, contact holes were etched to establish connections between the source−drain regions of the a-IGZO layer and the source−drain metal electrodes. For the creation of the source−drain electrodes, a 150 nm thick layer of aluminum (Al) was deposited onto the substrate through DC magnetron sputtering. After the patterning of the Al layer using a photolithography process, a dielectric layer was deposited on top of the fabricated a-IGZO TFT. The deposition of the dielectric layer followed the same method as the SOG gate insulator as an interlayer dielectric (ILD). This dielectric layer served as passivation for the TFT. The resulting structure is a top-gate coplanar a-IGZO TFT with channel dimensions of W/L = 100/20 μm. This integrated structure, incorporating the water-level sensor, is depicted in Figure 2.

A schematic view of the water-level sensor integrated on a substrate is shown in Figure 2a, with the TFT section highlighted in the circled area. A closer look at the TFT part is shown in Figure 2b. Additionally, Figure 2c showcases a photograph of the fabricated sensor, and Figure 2d provides microscopic images of the TFT section.

Evaluation. In order to evaluate the performance of the proposed water-level sensor, a MOSFET-based sensor was employed as a reference. The MOSFET-based sensor was fabricated by using soldering on a printed circuit board (PCB) with copper patterns. The soldering is not utilized in the fabrication process of the integrated water-level sensor. Following fabrication, the sensor was carefully enclosed within a protective case and encapsulated with epoxy resin. This encapsulation ensures durability and safeguards the sensor against environmental factors, allowing for reliable and long-lasting performance. Due to its noncontact nature, the capacitive water-level sensor is easily shielded from direct water contact, making it suitable for use in humid environments when protected with epoxy or similar materials. The water typically employed in applications often contains a high concentration of ions, resulting in a resistivity range of 5−50 Ω·cm for tap water. Consequently, the water effectively functions as an electrode to the ground.

A homemade measurement system was developed to evaluate the water-level sensor, as illustrated with an actual image in Figure 3. Figure 3 presents a setting for the measurements. The inset shows a schematic diagram illustrating the interconnections among the measuring instruments, including an oscilloscope, a waveform generator, and the sensors employed in the measurement system. The sensor's output waveform was connected to the oscilloscope, allowing for the observation of the waveform variations corresponding to the water-level changes. To effectively minimize the influence of external factors, such as illumination stress, vibration, wind, and other potential interferences on the a-IGZO TFT, a series of measures were implemented within a grounded shielded chamber. These measures were specifically designed to enhance the reliability and accuracy of the measurements.

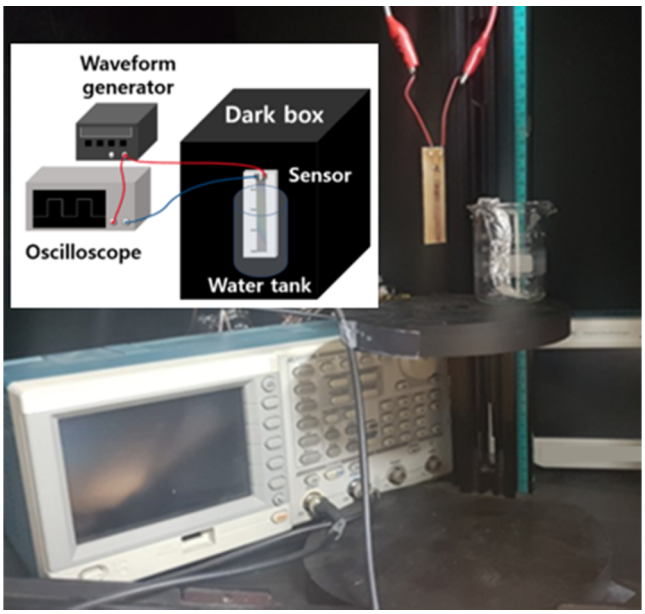

Figure 3. Measurement system is shown in a dark box, and the inset shows the schematic diagram of the measurement.

RESULTS AND DISCUSSION

Electrical Characteristics of the Fabricated a-IGZO TFT. The transfer characteristics of the fabricated a-IGZO TFT are shown in Figure 4, which shows the relationship

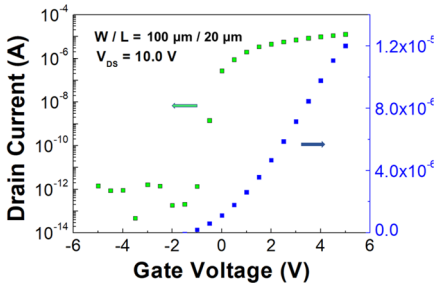

Figure 4. Transfer curve of the fabricated a-IGZO TFT.

between the gate voltages and the drain currents. The device performance was comprehensively evaluated by measuring several key parameters, including the threshold voltage, on/off ratio, subthreshold swing, and mobility. The results obtained highlight the impressive capabilities of the fabricated a-IGZO TFT. The threshold voltage (V_{TH}) of the fabricated a-IGZO TFT was determined to be 0.27 V. The on/off ratio (I_{ON}/I_{OFF}) was measured to be 10^7. The subthreshold swing (S.S.) and the mobility (μ_{FE}) were 0.71 V/decade and 7.31 $cm^2/V{\cdot}s$, respectively.

Proposed Integrated Water-Level Sensor. Figure 5 illustrates the water-level sensor circuit proposed in this study, featuring a single a-IGZO TFT integrated onto a glass substrate. The circuit operates by applying an input pulse to Vin, resulting in a proportional variation in the gate voltage of the TFT based on the capacitance ratio of C_1 to C_2. Specifically, when the input pulse voltage rises from a low to a high level, the gate voltage of T_1 increases accordingly, thereby influencing the current flowing through the TFT.[26]

Consequently, variations in the capacitance ratio of C_1 to C_2 result in changes in the current flowing to the readout line

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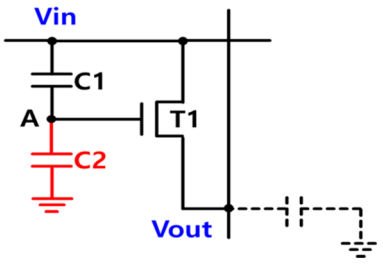

Figure 5. Equivalent circuit of the proposed water-level sensor.

through the TFT. Therefore, the flowing current charges a parasitic capacitance represented by the dotted line, resulting in an increase in voltage and subsequently inducing a proportional alteration in the output voltage.

C_1 is a capacitor that is integrated into a substrate during the TFT process. On the other hand, C_2 denotes the capacitor established between a sensing electrode and the water, where its capacitance is directly influenced by the level of the water present. The C_2 is represented in Figure 6a,b. When an input

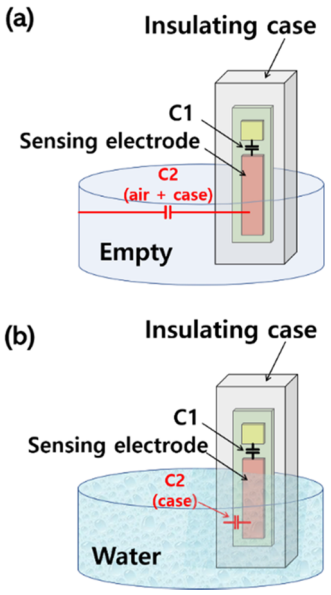

Figure 6. Schematic diagrams showing the capacitances in (a) an empty tank and (b) a filled tank with water.

pulse is applied, the T1 gate voltage is bootstrapped by the equation specified in eq 1.

$$V_G = \Delta V(C_1 + C_{gd})/(C_1 + C_{gd} + C_2 + C_{gs}) \quad (1)$$

where C_{gd} is the parasitic capacitance between the gate and drain, C_{gs} is the parasitic capacitance between the gate and source, and ΔV is the input voltage increase from low to high voltage. As node A is floated, the voltage at node A is determined through charge conservation at that node, resulting in eq 1.

The capacitance C_2 between the sensing electrode and the water is significantly higher compared to when the container is empty, primarily due to the conducting properties of water, which exhibit a resistivity range of 5−50 Ω·cm for tap water. When the container is filled with water, the distance between the count electrode and the sensing electrode is much shorter than that in the empty state. For the water-level sensor to operate optimally, it is crucial that the capacitance of C_1 is higher than the capacitance of C_2 at low water levels and lower than the capacitance of C_2 at high water levels. This emphasizes the significance of capacitance design in ensuring the proper functioning of the water-level sensor as the gate voltage (V_G) relies on the ratio of capacitance between C_1 and C_2 in relation to the water level. A variation in the voltage at node A causes a corresponding change in the current flowing through TFT T_1, thereby influencing the voltage of the readout line.

Figure 6a,b provides a visual representation of the operational principle of the proposed water-level sensor within a water tank. It presents a schematic depiction of how the capacitance C_2 varies based on the water height in relation to C_1. The sensing electrode is strategically designed as a long, rectangular strip positioned parallel to the water depth. The length of the sensing electrode is carefully determined based on the anticipated maximum water level that the tank can accommodate.

In the experimental setup, depicted in Figure 6a, the capacitance C_2 is established between the sensing electrode and a distant ground electrode when the tank is empty. Conversely, when the tank is filled with water, as illustrated in Figure 6b, capacitance C_2 is formed between the sensing electrode and the water itself due to water's conductive properties as an electrolyte. As a result, capacitance C_2 exhibits an incremental rise corresponding to the increasing water level within the tank. Consequently, in the sensor configuration depicted in Figure 6b, when the input pulse is applied, an increase in the capacitance of C_2 leads to a proportional decrease in the output pulse voltages. This is attributed to the reduction of the gate voltage of TFT T_1 as governed by eq 1. Conversely, in the case of an empty tank similar to Figure 6a, a lower value of capacitance C_2 causes a decrease in the output voltage due to the elevated gate voltage of TFT T_2, as indicated by eq 1.

The simulation results of the proposed water-level sensor are illustrated in Figure 7. For the simulations, typical oxide TFT model parameters were utilized. Figure 7a shows the input pulse applied to Vin, featuring a pulse width of 10 μs, where the input low is set at 0 V and the input high at 5 V to ensure accurate simulation of the water-level sensor; meticulous calculations of C_1 were conducted for both the tank filled with water and the empty tank. For the full tank, the water level

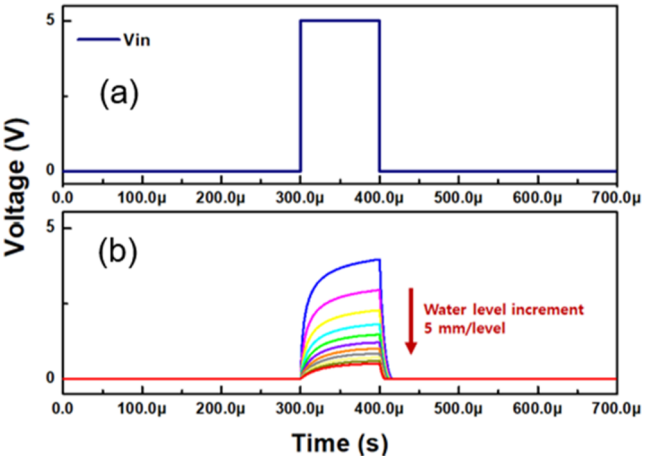

Figure 7. Simulated output waveforms, (a) input pulses, and (b) outputs.

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ACS Omega 2023, 8, 36868−36875

reached the top of the sensor electrode, whereas, for the empty tank, the water level remained below the sensor electrode. The resulting values are detailed in Table 1. The reference capacitance C_1, connected between the drain and gate of TFT T_1, was established as 1.47 pF, while a load capacitance of 10 pF was considered for the system.

Table 1. Calculated Capacitances Used in the Simulation for Both an Empty Tank and a Tank Filled with Water

capacitance		value
C_1		1.47 pF
C_2	empty tank	2.16 fF
	filled tank	4.68 pF

As the water level rises, the area of the electrode between the water and the sensing electrode increases, leading to a corresponding increase in the capacitance of C_2. This higher capacitance (C_2) results in decreased output voltages, as demonstrated in Figure 7b, where the water level was raised by 5 mm.

To determine the capacitance of C_2, factors such as the distance between the water and the sensing electrode, along with a sensing electrode area of 150 mm^2, were carefully considered during the calculations. For the tank filled with water, the capacitance between the sensing electrode and water was determined to be 4.68 pF, considering the 150 mm^2 area of the sensing electrode and the 1 mm distance between the water and the sensing electrode. On the other hand, in the case of the empty tank, the capacitance C_2 was calculated to be 2.16 fF between the sensing electrode and the ground electrode of the tank, assuming a distance of 1 m between the ground electrode and the sensing electrode.

The measurement results are listed in Figure 8. When the water level is low, the capacitance of C_2 is smaller compared to C_1, which leads to an increase in the gate voltage. Consequently, there is an increased output voltage, as depicted in Figure 8. Conversely, when the water level is high, the capacitance of C_2 becomes larger than C_1. This causes the gate voltage to decrease, resulting in the TFT switching off. As a result, no current flows through the circuit, leading to a low output voltage, as shown in Figure 8. The reference capacitance C_1 is formed between the gate electrode and the input electrode Vin.

The measurement results of the water-level sensor fabricated using the a-IGZO TFT process and the MOSFET sensor on PCB are presented in Figure 9a,b, respectively. In these measurements, a square wave input signal with a pulse width of 500 μs and an amplitude ranging from −2 to 5 V was applied. The output signal was captured using an oscilloscope, while the sensor was immersed in the tank, and the water level was systematically adjusted to observe the corresponding changes.

When the water level is low, the capacitance of C_2 is smaller than that of C_1. In this scenario, bootstrapping takes place through C_1, causing an increase in the gate voltage as the input signal reaches a high voltage. Consequently, the transistor effectively boosts the current passing through it, resulting in a significant increase in the output voltage. However, as the water level gradually increases, the capacitance of C_2 becomes larger than that of C_1. Consequently, even if the input signal reaches a high voltage, the gate voltage does not rise in accordance with eq 1. This leads to a decrease in the output voltage as the water level continues to rise. However, it is

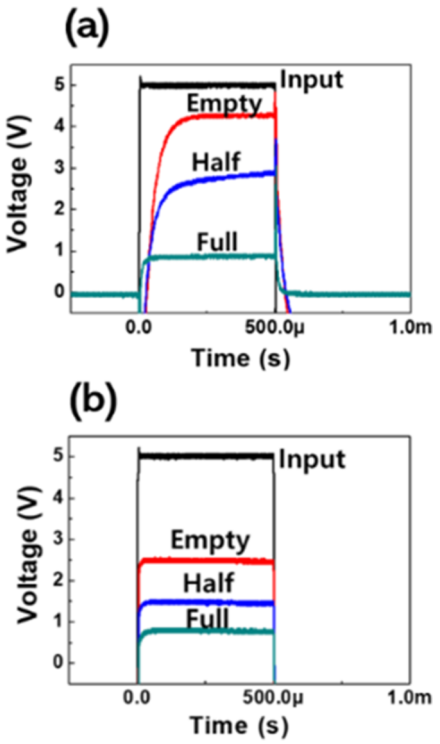

Figure 8. Measured output voltages of the water-level sensors: (a) water-level sensor integrated with a-IGZO TFT, and (b) water-level sensor configured with MOSFET.

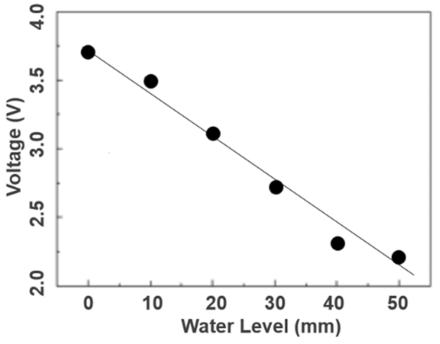

Figure 9. Output voltages correspond to different water levels.

crucial to acknowledge that even though capacitance shows a linear increase, the TFT used in this context can introduce nonlinearity in its characteristics, leading to deviations in the output linearity. To address this, we optimized the water-level MOSFET PCB sensor. Subsequently, we conducted measurements of the resulting outputs to observe and analyze variations corresponding to different water levels, as visually depicted in Figure 9.

As shown in Figure 8a, the integrated sensor exhibits significantly longer rise and fall times in its output pulses compared to the reference sensor employing MOSFET. The speed at which the signal rises and falls is influenced by the time constant, which can be calculated by multiplying the on-resistance of the TFT with the capacitance of the readout line. The longer rise and fall times can be attributed to the significantly lower mobility of the TFTs compared to MOSFETs. This disparity in mobility results in a higher on-resistance for the TFTs, leading to the observed longer rise and fall times in the integrated sensor. As demonstrated in Figure

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ACS Omega 2023, 8, 36868−36875

8a,b, the rise time is notably longer than the fall time, which is a distinctive characteristic of the N-channel TFT in the oxide TFT technology.

On the other hand, when comparing the output voltage of the integrated sensor to that of the MOSFET PCB sensor, the integrated sensor exhibits a notably higher output voltage. This higher output voltage provides a distinct advantage over the MOSFET PCB sensor. Indeed, TFTs and MOSFETs have different structures that contribute to the disparity in their parasitic capacitances. TFTs typically employ an insulating substrate, such as glass, while MOSFETs use a semiconductor layer, typically a Si wafer, as the substrate. The conductive substrate in MOSFETs and the thinner gate insulator in MOSFETs compared with TFTs contribute to higher parasitic capacitances in MOSFETs. The conductive substrate of MOSFETs can introduce additional capacitance between the substrate and the gate, which increases the overall capacitance. Additionally, the thinner gate insulator in MOSFETs allows for a closer proximity between the gate and the channel region, resulting in higher capacitance. These structural differences between TFTs and MOSFETs, specifically the insulating substrate in TFTs and the conductive substrate in MOSFETs, along with the thinner gate insulator in MOSFETs, contribute to the higher parasitic capacitances observed in MOSFETs compared to TFTs.

The larger parasitic capacitances inherent in MOSFETs compared to those of other devices play a significant role in explaining the observed lower output voltages. These capacitances introduce additional capacitive loading into the circuit, which, in turn, affects the voltage response. This relationship can be elucidated using eq 1, which demonstrates that an increase in the gate−source capacitance (C_{gs}) results in a decrease in the gate voltage (V_G). Consequently, this reduction in V_G leads to a decrease in the current flowing through TFT T_1. Ultimately, the decrease in current results in lower output voltages.

The gate−source capacitance (C_{gs}) and gate−drain capacitance (C_{gd}) hold crucial importance in governing the operation of a transistor. Therefore, it is imperative to comprehend the interplay between C_{gs}, C_{gd}, V_G, and the resulting current flow when designing and optimizing transistor performance. By carefully considering and managing the gate−source and gate−drain capacitances, it becomes feasible to control the output voltages and achieve the desired operational characteristics in electronic systems. In practical applications, it is essential to account for these parasitic capacitances to ensure a precise and reliable voltage output. However, when TFTs are incorporated into the design of a water-level sensor, a distinct engineering advantage emerges. Notably, the parasitic capacitances associated with TFTs are markedly smaller in comparison to those of their MOSFET counterparts. As a result, the impact of parasitic capacitances on the overall performance of the water-level sensor becomes less significant. This characteristic represents a notable advantage of TFT-integrated water-level sensors. With smaller parasitic capacitances in TFTs, the influence on the voltage output and circuit behavior is diminished, allowing for a more straightforward design and optimization process. This reduced dependence on managing and mitigating parasitic capacitances simplifies the overall system implementation and enhances the reliability and accuracy of the voltage output in water-level sensing applications.

Consequently, the use of TFTs in water-level sensors offers added benefits, as the smaller parasitic capacitances minimize the need for intricate capacitance management techniques, streamlining the design process and improving the overall performance and functionality of the sensor.

CONCLUSIONS

A pioneering water-level sensor has been proposed, which incorporates a TFT circuit integrated into a substrate. Following the fabrication process, the sensor was thoroughly tested to evaluate its performance and functionality. The proposed water-level sensor offers a simplified design, employing just a single transistor, which significantly reduces the overall cost of production. Moreover, the sensor has been successfully implemented by integrating the circuit directly onto a glass substrate using the IGZO TFT process. This integration approach enhances the robustness of the sensor module as it eliminates the need for soldering and wiring, which can otherwise compromise the reliability of the assembly. By circumventing these potential sources of failure, the sensor module achieves a higher durability and improved long-term performance.

The integration of the TFT brings about a significant reduction in the parasitic capacitance between the drain and gate electrodes in comparison to a conventional MOSFET device. This reduction in parasitic capacitance leads to notable improvements in the reading voltage of the output signal. As a result, the water-level sensor becomes more sensitive and accurate and is capable of delivering precise measurements with enhanced reliability. The decreased parasitic capacitance ensures that the sensor responds more effectively to changes in the water level, enabling it to capture even subtle variations and provide highly accurate readings.

The IGZO TFT-integrated water-level sensor exhibited a voltage output of 4.2 V when the tank was empty and 0.9 V when the tank reached its full capacity. This reliable and consistent response allows for the accurate monitoring of the water level. An additional advantage of the TFT process is its versatility in being applied to diverse substrates, including films, papers, and metal foils. This characteristic opens up possibilities for flexible applications, expanding the potential uses of this sensor in various industries and environments. With its adaptability to different substrates, the IGZO TFT-integrated water-level sensor holds promise for a wide range of applications, providing flexibility and convenience in the installation and integration into different systems.

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Notes

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