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Article

Synergistic Approach of Interfacial Layer Engineering and READ-Voltage Optimization in HfO_2-Based FeFETs for In-Memory-Computing Applications

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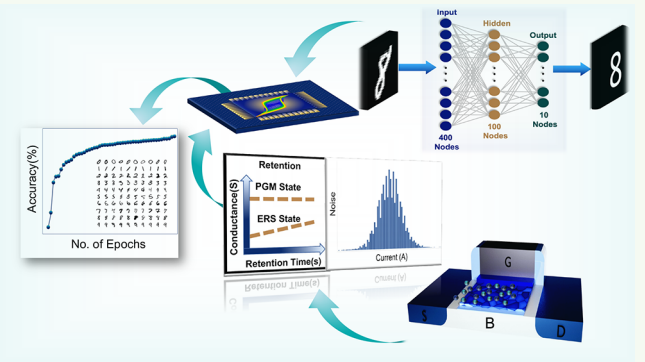
ABSTRACT: This article reports an improvement in the performance of the hafnium oxide-based (HfO_2) ferroelectric field-effect transistors (FeFET) achieved by a synergistic approach of interfacial layer (*IL*) engineering and *READ*-voltage optimization. FeFET devices with silicon dioxide (SiO_2) and silicon oxynitride (SiON) as *IL* were fabricated and characterized. Although the FeFETs with SiO_2 interfaces demonstrated better low-frequency characteristics compared to the FeFETs with SiON interfaces, the latter demonstrated better *WRITE* endurance and retention. Finally, the neuromorphic simulation was conducted to evaluate the performance of FeFETs with SiO_2 and SiON *IL* as synaptic devices. We observed that the *WRITE* endurance in both types of FeFETs was insufficient ($<10^8$) to carry out online neural network training. Therefore, we consider an inference-only operation with offline neural network training. The system-level simulation reveals that the impact of systematic degradation via retention degradation is much more significant for inference-only operation than low-frequency noise. The neural network with FeFETs based on SiON *IL* in the synaptic core shows 96% accuracy for the inference operation on the handwritten digit from the Modified National Institute of Standards and Technology (*MNIST*) data set in the presence of flicker noise and retention degradation, which is only a 2.5% deviation from the software baseline.



KEYWORDS: *neuromorphic computing, Flicker noise, interface traps, FeFET, hafnium oxide, interface treatments*

INTRODUCTION

The advent of neural networks (NN), especially the convolution neural network,[1−3] brought a historical change in the field of computing, and machine learning became the *bona fide* choice for solving many tasks. However, the software-based artificial neural networks (ANN) implemented in traditional *von Neumann* computing systems face severe bottlenecks due to the latency engendered by the data transfer between segregated memory units and processing units. This bottleneck has become more vivid with the plethora of edge devices in recent times. Their real-time data have manifested the need to overcome latency and energy costs induced by the data transfer between the processing unit and memory in *von Neumann* architecture. Therefore, researchers showed interest in building an in-memory-computing (IMC) based alternative paradigm,[4−8] where the computation is done inside the memory, reducing the latency and energy cost. The quintessential example of IMC is vector-matrix multiplication (VMM) with nonvolatile memories (NVMs), which is applied to solve many high-level applications such as neuromorphic computing and to solve computationally tricky problems.[9−12] During the execution of VMM for neuromorphic computing, the memory unit must perform computations using single-instruction data sets. The memory element used for calculation must be able to encode the data in physically realizable parameters such as charge, current, or voltage with low latency and also must be compatible with the scaling trend.

Among many emerging memory technologies like resistive random access memory (ReRAM)[13−15] and phase change memory (PCM),[16−19] ferroelectric field effect transistors (FeFETs) seem to be the most promising ones. The

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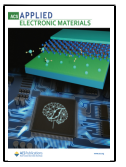

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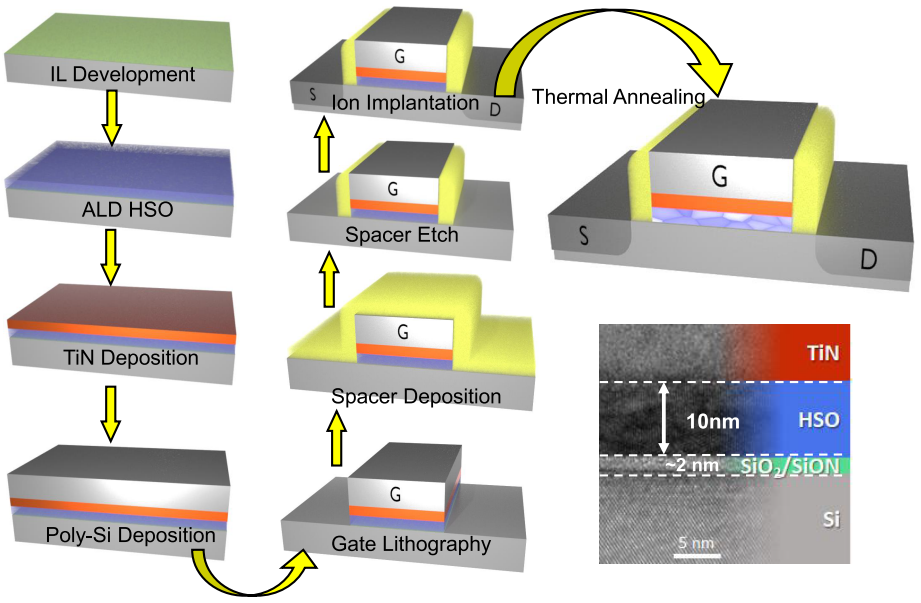

Figure 1. Schematic and process flow of the FeFET devices with a 10 nm Si:HfO_2 layer. The inset shows the transmission electron microscopy image of the material stack.

pronunciation of ferroelectricity in a single-layer thin film of hafnium oxide (HfO_2), fast switching, high on-current (I_{ON}) to off-current (I_{OFF}) ratio $\left(\frac{I_{ON}}{I_{OFF}}\right)$, excellent linearity in synaptic weight updates, bidirectional operation, and good endurance are the key technological factors that make FeFET superior to other methods.[20,23−30,21,22] However, the primary bottleneck in implementing the FeFET-based computing system lies in the intrinsic stochasticity owing to the polycrystalline nature of HfO_2-based ferroelectric thin film, as well as inherent defect sites that may capture electrons or holes from the channel side (CS) or gate side (GS).[31−33] Numerous efforts have been made to reduce the impacts of such nonidealities from the device process, and a circuit point of view.[34−39,23,25] Previously, it has been reported how the quality of the interface and the *READ*-Voltage play a pivotal role in the performance of FeFETs, especially for low-frequency noise response, retention, and endurance.[40,41,25,21,42−44] In this work, we aim to maximize the reliability and performance of FeFETs by adopting a synergistic approach of *READ*-voltage optimization and interfacial-layer engineering.

This paper begins with the fabrication and characterization of FeFET devices. We have fabricated FeFET devices with two different interfaces, SiON and SiO_2. Low-frequency noise, endurance and retention characteristics are used to gauge the impact of *IL* of the performance of the FeFETs. The noise spectrum, in terms of output power spectral density (*SID*) and the input gate voltage noise (*SvG*), are used to characterize the low-frequency noise characteristics. Although we observed that FeFETs based on SiO_2 show a wider memory window (MW) and better low-frequency noise response, FeFETs with SiON as *IL* outperform those with SiO_2 as *IL* in terms of endurance and retention. This phenomenon is discussed in detail in the following sections.

The second part of this article assesses the impact of *IL* engineering on neuromorphic computing applications. An artificial neural network has two primary operations: (i) training and (ii) inference. The goal of the training operation is to obtain the best possible values for the synaptic weights to minimize the cost function. Therefore, synaptic weights are constantly updated during training operations, necessitating high *WRITE* endurance in synaptic devices for online training. The other plausible option is offline training of neural networks and carrying out the inference-only operations in the hardware. During offline training, the synaptic weights are optimized in the software and are subsequently written into the hardware. Therefore, stable data-retention capability and low *READ* variations are necessary for carrying-out inference operations on the hardware without repeated retraining. With the endurance to *WRITE* limited to 3×10^4 cycles, online training of the neural network (NN) becomes tricky with the synaptic devices manufactured in the synaptic core. Therefore, we have considered an inference-only operation after training the neural network offline for a single time. We observed that optimizing the *READ* voltage could reduce the impact of low-frequency noise, especially during a *READ* operation. However, the systematic degradation in long-term data retention becomes crucial for conducting an inference operation without retraining. Devices with SiON interface demonstrate high immunity to such variations and maintain an inference accuracy of over 96% without retraining for MNIST handwritten data sets in the presence of noise and retention degradation.

EXPERIMENTS

Fabrication. The tested devices are FeFETs prepared on 300 mm bulk-Si wafers with CMOS-compatible industry-standard production tools. The size of the devices under consideration are 1 μm^2 (W = 1 μm and L = 1 μm), with 2 nm thick interface material of SiO_2 or SiON, and a 10 nm silicon-doped HfO_2 (HSO) layer. The transmission electron microscopic (TEM) image in Figure 1 confirms the thickness of the interfacial and ferroelectric layers. The interfacial layer of SiO_2 was grown by self-terminating chemical oxidation, and the SiON layer was formed by rapid thermal annealing (RTA). The quintessential process of preparing HfO_2 thin film is atomic layer deposition (ALD). The ALD process involves the sequential deposition of a self-limiting monolayer of precursor molecules with an oxidizer. We used $HfCl_4$ with $SiCl_4$ as precursors and H_2O as an oxidizing agent during ALD. The ALD of the 10 nm HSO layer was

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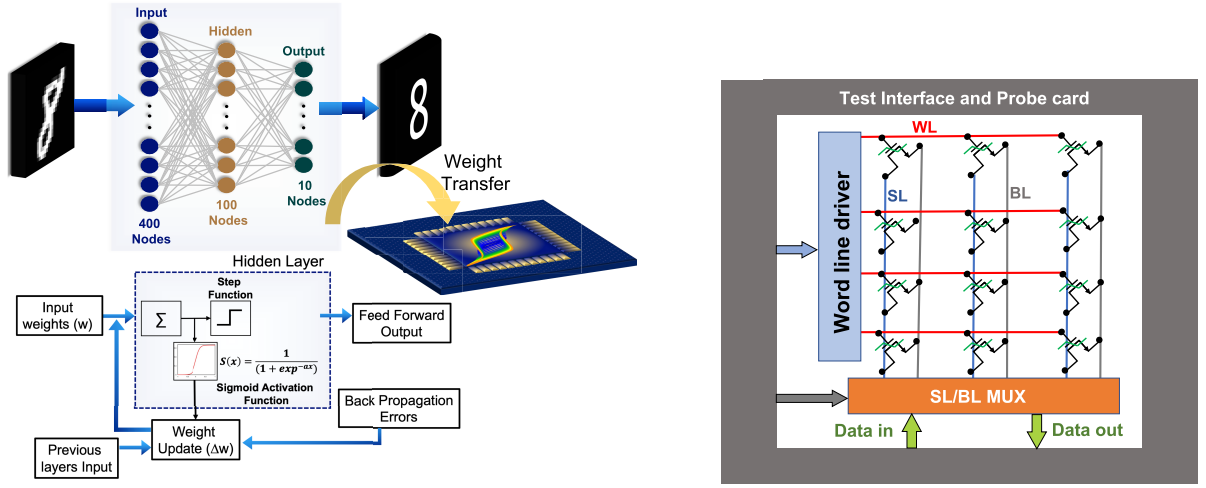

Figure 2. (a) Schematic representation of the neural network architecture used for simulating the performance of FeFET-based synaptic devices. The input is an image of the hand-written digits. To simplify the hardware implementation task, the image is reshaped with a size of 20 × 20 pixels. Therefore, the neural network has 400 input layers, 100 hidden layers, and 10 output layers. (b) Memory array architecture shows the synaptic core used for simulating the inference operation.

conducted at 300 °C. The cycling ratios for $HfCl_4$ and $SiCl_4$ were 16:1. The top electrode of titanium nitride (TiN) and amorphous silicon was deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD), respectively. The RTA for crystallization and dopant activation was conducted simultaneously at 1050 °C for 5 s. Figure 1 describes the detailed process flow of device fabrication.

Electrical Characterization. The electrical characterization was conducted using a *B1500A Semiconductor Analyzer*. The devices were subjected to wake-up cycling by 5 and −4.5 V pulses of 500 ns before *READ-WRITE*. The fabricated devices were programmed to binary levels using 500 ns pulses at the gate terminal. A positive pulse at the gate terminal of n-type FeFET programs the devices at a low threshold voltage (LVT) state, and the negative pulse programs the device at a high threshold voltage (HVT) state. Each *WRITE* pulse was preceded by a *RESET* pulse of 500 ns, which is −5 V for *WRITE-1* and 4.5 V for *WRITE-0*. The drain, source, and bulk terminals were biased at 0 V during the *WRITE* operation. The *WRITE*-pulses, applied at the gate terminal, align the ferroelectric dipoles according to their polarity, which manipulates the surface charge density of the channel, the conductance of channel (G_{ch}), and the threshold voltage (V_t). Each state's V_t was extracted at a constant drain current of 100 nA. A nondisturbing direct current (DC) sweep from −0.5 to +2 V was applied at the gate terminal for the *READ* operation. The drain to source voltage (V_{ds}) was 100 mV during the *READ* operation.

Noise and Reliability Characterization. Quintessentially, one observes the low-frequency or flicker noise as the aftermath of the dangling bonds at the semiconductor and gate dielectric interface and the defect states in the dielectric material. In FeFETs, during the *READ* operation of the FeFETs, the surface charge carriers of the semiconductor can be randomly trapped and detrapped inside the defect states of the dielectric, generating the flicker noise in the drain current. Flicker noise investigation and characterization were performed with a *ProPlus* noise measurement system along with the low noise amplifiers and the filtering of the system. For considering the ferroelectric influence and different noise behavior of the HVT and LVT states of the device, a more detailed description can be found elsewhere.[37] Multiple operating points were set for various measurements focusing on the linear region. We have analyzed input referred or gate input noise (*SvG*) and output or drain current noise *SID*. *SvG* is an important Figure of merit, which provides crucial information regarding the choice of the optimal operating point. The analytical expression of it are given by the relationship $SvG = \frac{SID}{(g_m)^2}$.[45,46] The parameter g_m is the transconductance of the MOSFET and is defined by the change of drain current I_D (device output current) to the change of the gate to source voltage V_{gs} (device input voltage). g_m is mathematically represented by, $g_m = \frac{\delta I_D}{\delta V_{gs}}$. The output power spectral density represents the drain current change in the frequency domain. The change of the current in time is translated into the frequency domain by Fourier transformation. The power spectral density can be described as $SID = SV_{fb}\left(1 + \frac{\alpha\mu_{eff}C_{ox}I_D}{gm}\right)^2 g_m^2$. The first term, SV_{fb}, is the flat band voltage spectral density. μ_{eff} is the effective mobility, C_{ox} is the effective oxide capacitance, and α is the Coulomb scattering factor. The *SvG* presentation is a powerful point of view to compare the input noise behavior for an equivalent gate voltage for different technologies and with different interface materials.[46] The detailed method of low-frequency noise investigation is demonstrated in our previous work.[37]

Electric field cycling was applied for endurance measurement with amplitudes in the ±6 V range and a pulse width of 500 ns.

Neural Network Simulation. Finally, the impact of low-frequency noise and retention degradation on FeFETs on their system-level performance, especially for neuromorphic applications, was evaluated by Neurosim simulation platform.[47] The experimentally calibrated conductance value with variation statistics was used to simulate the multilevel perception (MLP) neural network (NN) performance with the MNIST data set. The neural network's architecture is illustrated in Figure 2a. The MLP architecture comprises three layers, which are 400 input nodes, 100 hidden nodes, and 10 nodes in the output layer. In this work, we have considered offline training scenarios of neural networks. Although it has been mentioned in many previous works of literature that online training in the neural network can alleviate the impact of conductance drift of FeFETs,[48,49,26,40] it requires high endurance. It is power-hungry.[25,50] Therefore, we focus on an inference-only operation with offline neural network training. The back-propagation algorithm with the optimizer *Adam* was adopted to minimize the cost function during offline training. We have considered the step function as an activation function during forward-propagation and the sigmoid function as an activation function during back-propagation. After offline training, the synaptic weights, in terms of channel conductance of FeFETs, were updated on the hardware using a single-shot programming pulse. The synaptic weights were normalized between the minimum value (W_{min})

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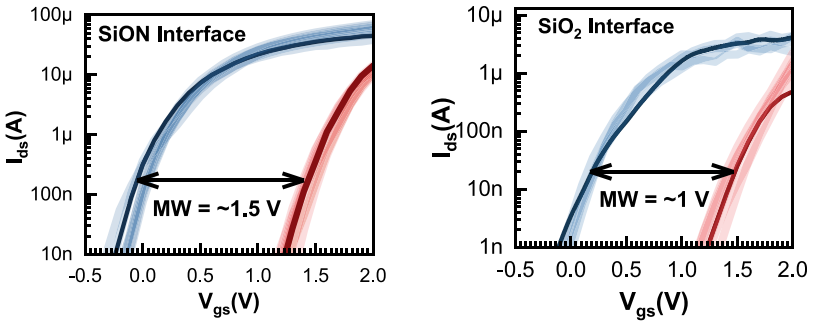

Figure 3. (a) Transfer characteristics of FeFETs with SiON interface for programmed and erased states show an average memory window of 1.5 V, (b) while the devices with SiO_2 interface have an average memory window of 1 V.

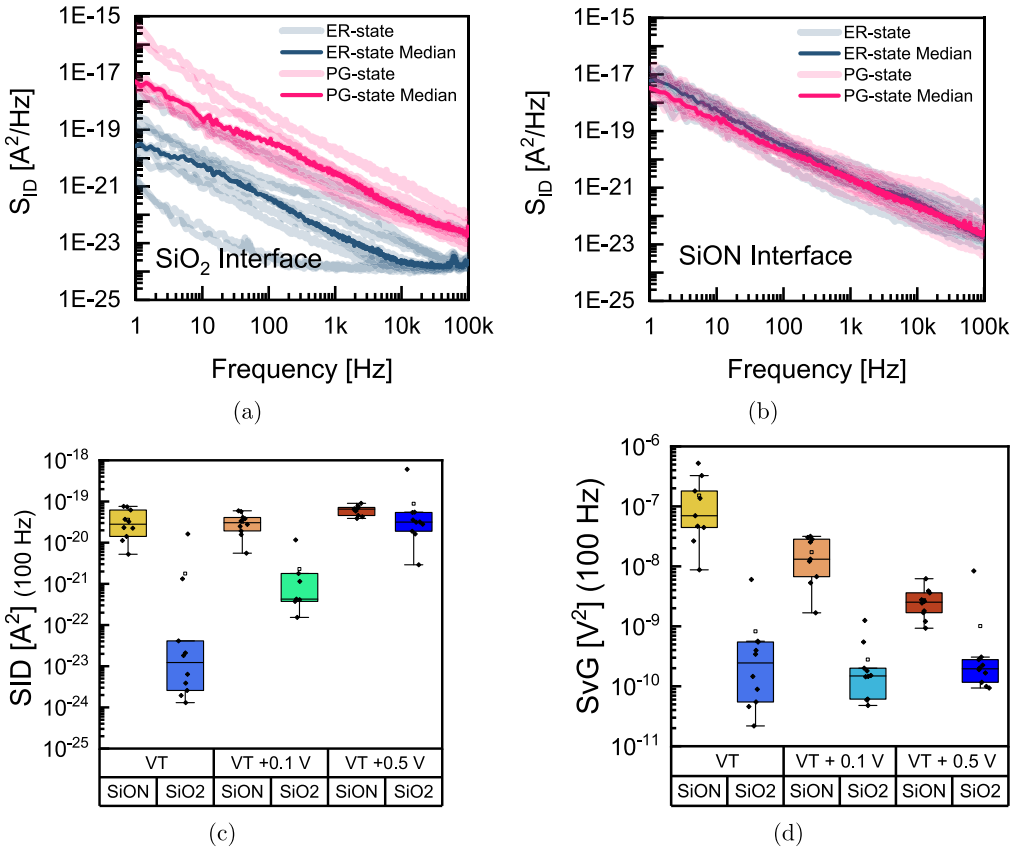

Figure 4. (a) Power spectral density (*SID*) noise behavior of the 10 nm HSO and SiO_2 interface structure. In blue the ferroelectric erase state (ER) and in red the programmed state (PG) are demonstrated. The operating point is set on V_t with an offset of 100 mV. (b) *SID* noise behavior of the 10 nm HSO and SiON interface structure. ER and PG state are on the same noise level. (c) Current normalized noise behavior with two different structures (one structure with SiON and the other with SiO_2 interface material) The noise level change for different operating points is demonstrated for a frequency of 100 Hz in erase state. (d) Equivalent input gate voltage noise (*SvG*) with two different structures (one structure with SiON and the other with SiO_2 interface material) The noise level change for different operating points is demonstrated for a frequency of 100 Hz.

of −1 and the maximum value (W_{max}) of 1. The I_{OFF} of the FeFETs was mapped with W_{min}, and the I_{ON} was mapped with W_{max}. The FeFET-based synaptic core, shown in Figure 2b, is used to carry out the vector−matrix−multiplication operation. The output of the vector−matrix−multiplication is directly digitized by using a current-to-digital converter.[47] An additional *READ* variation parameter simulated the impact of low-frequency noise with experimentally calibrated variation statistics. The impacts of retention degradation were simulated using the experimentally obtained channel conductance value with extrapolation up to 10 years. The cumulative impact was evaluated by turning on all sources of variations during inference operation. The results obtained from the experiments will be discussed in the following sections.

RESULTS AND DISCUSSION

Parts a and b of Figure 3 show the *READ* operation conducted after *WRITE* of the FeFETs with SiON and SiO_2 interface. FeFETs with SiON interface show a higher memory window than those with SiO_2. This trait can be attributed to the trapping and detrapping phenomena from the interface. Further analysis of the low-frequency noise provides a better

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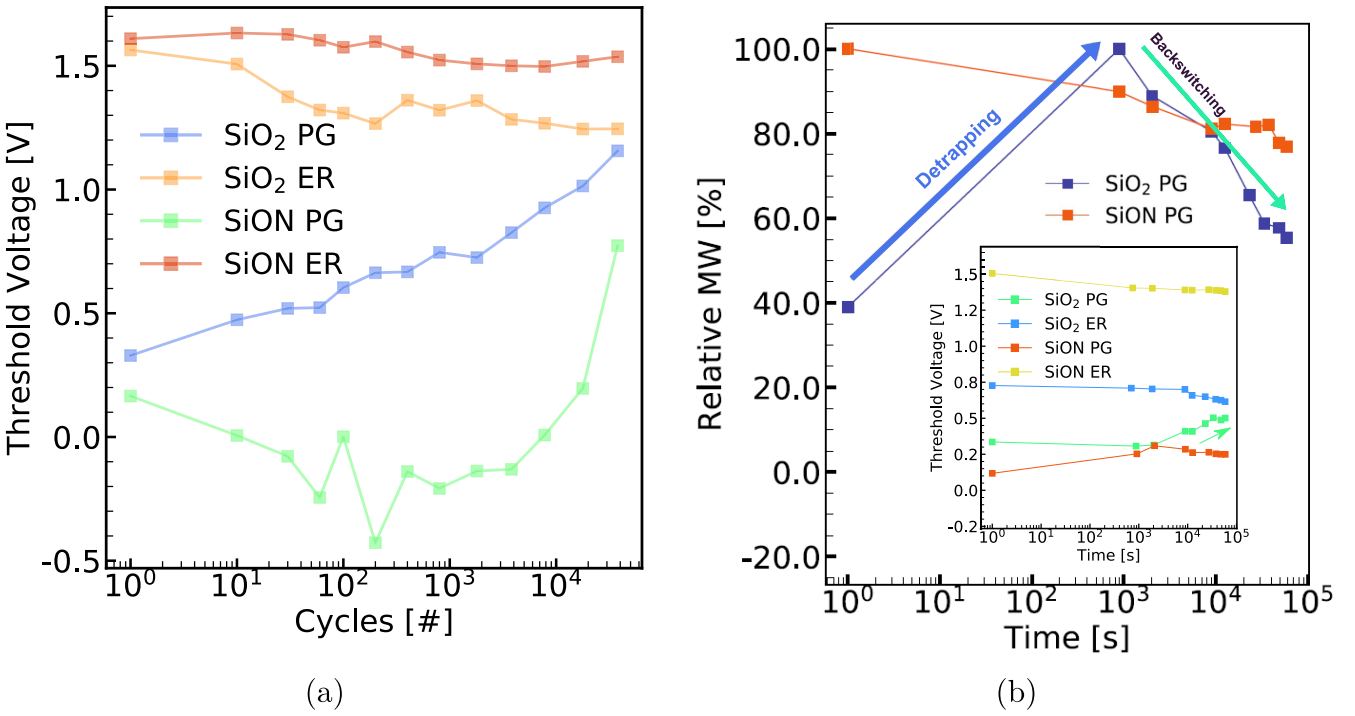

Figure 5. (a) Endurance characteristics of SiO_2 and SiON-based HSO FeFETs for a stress voltage amplitude of 6 V. (b) Retention of the high- and low V_t state of HSO FeFETs with SiO_2 and SiON interface layer.

insight into the root cause of memory window reduction in SiO_2-based FeFETs. However, the device-to-device variation and on-state current (I_{on}) to off-state current (I_{off}) ratio remain almost the same for both of the interfaces.

The spectral density of the drain current (*SID*) was measured with an operation point of 100 mV offset from V_t. In an erased and programmed state, the *SID* noise behavior for the 10 nm HSO SiO_2 interface structure is demonstrated up to a frequency of 100 kHz in Figure 4a. In light blue, the single-device measurements are included. Two of these measurements have a low noise level, and a different slope compared to the other single die measurements of the SiO_2 interface erases the state measurements; for these, the operating current for the used gate voltage was too low and reached the detection limit of the system. In Figure 4b, *SID* is shown for the 10 nm HSO SiON structure. For both states, ER and PG, the noise behavior does not show differences in the two states. Compared to dielectric devices in 22 nm technology (investigation on 22 nm FDX device was presented elsewhere[45]), the noise behavior in the lower frequency area for the PG-state is similar. For the higher frequencies, a difference of two magnitudes can be observed. For the SiO_2 interface structure, the noise level reaches higher frequencies than the system limit.

Figure 4c shows the noise current (*SID*) for different operating points and different interface materials (SiON, SiO_2). In direct comparison to the threshold voltage (V_t) operating point, the SiON structure has a higher noise level than the SiO_2 structure. The SiON structure shows a decrease in noise level with increasing gate voltage V_g, while for FeFETs with SiO_2 interface, the noise level remains the same for different values of V_g.

On the other hand, Figure 4d shows the equivalent input gate voltage noise for different operating points and interface materials. SiON structure shows a continuous decreasing trend with increasing V_g as in the normalized *SID*, and the SiO_2 interface structure has the same level of *SvG* for different operating points. The difference between SiON and SiO_2 for lower V_g operation points is similar in *SvG* and *SID*. The change for higher V_g voltages differs. The gate input for higher operating voltage is, for the SiON interface, lower than the total noise level of this structure. For SiO_2, an increase in the operating voltage does not influence both.

In HSO-based FeFETs,[51,37] a modification of the interface layer has been shown to improve reliability, especially the device's resistance. Figure 5a visualizes the cycling endurance of FeFETs based on FeFETs based on SiO_2 and SiON for a stress voltage amplitude of 6 V. Although continuous degradation of the MW is observed for the SiO_2 interface layer, resulting in complete closure at approximately 3×10^4 cycles, the device based on SiON exhibits a stable and comprehensive MW up to 10^4 cycles. Although there have been several demonstrations of improvement of endurance in HfO_2 based ferroelectric films,[52,53] the WRITE-endurance of our devices are comparable with the 28 nm HKMG FeFETs from GlobalFoundries'.[27] At a higher number of cycles, a walkout of the low V_t state to the high V_t state is observable, most likely caused by trapped charges. Still, an MW exceeding 700 mV remains at 3×10^4 cycles. In the case of retention (see Figure 5b), stable V_t states are observed for both programmed and erased conditions in the case of the SiON-based devices. However, initial detrapping is observable. A back-switching trend is present for devices based on SiO_2, as indicated by the green arrow.

The origin of improved retention in SiON-based FeFETs can be related to the depolarization field change. Due to the higher relative permittivity of SiON compared to SiO_2, the depolarization field is reduced.[51] However, (de)trapping behavior for these is not understood in detail. The Flicker noise results here, however, clearly indicate an increased noise

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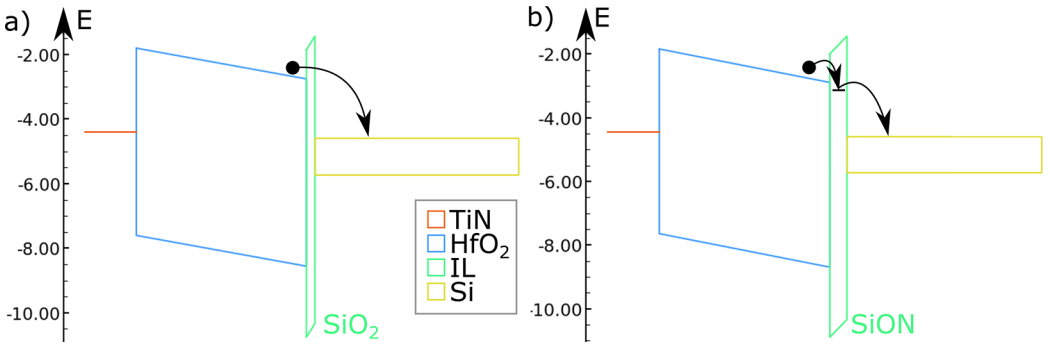

Figure 6. Schematic illustration of the band structure of a SiO_2- (a) and a SiON- (b) based FeFET. An electron pocket is observed at the ferroelectric−insulator interface.

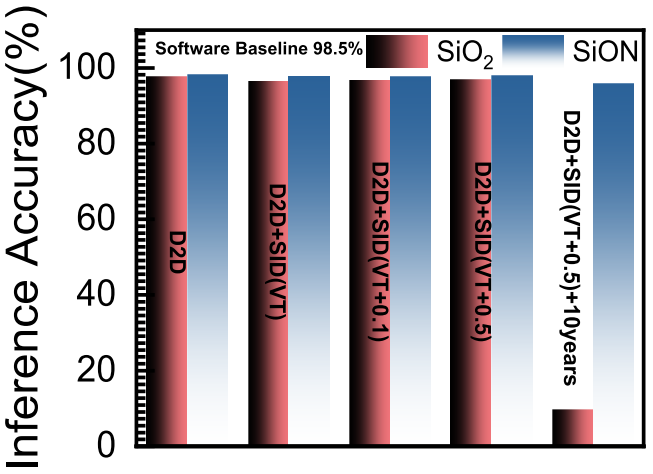

Figure 7. Inference accuracy shows that the systematic variation due to retention degradation has a higher impact on the inference operation than the random variation caused by low-frequency noise during the *READ* operation. The higher on-current to off-current ratio ensures better inference accuracy for MLP-NN built with SiON interfacial layer-based FeFETs as synaptic devices.

level for the SiON devices, close to V_t. This indicates increased trapping and detrapping of charges. As a result, charges can detrap faster after the writing pulse, resulting in an already open MW after writing in the case of SiON interface, whereas the SiO_2-based devices show this pronounced detrapping effect. The strong back-switching trend afterward can be explained by the displacement field as mentioned above and additional charge-trapping from the other interface at the electrode, which cannot be detrapped easily due to the presence of the electron pocket in the band structure (see Figure 6).

In the case of endurance, a similar origin can be deduced. As for retention, charges are trapped inside the electron pocket in the band structure. As observed in the retention case where an opening of the MW is observed for SiO_2-based devices due to initially trapped charges, repeated cycling results in a similar effect, only that, with extensive cycling, many more charges are trapped. As they cannot easily detrap, compared to SiON, a memory closure is observable, as these charges will pin domains and shift the internal bias field. This effect has recently been explored as well for fluorinated interfaces,[37] reporting consistent results with the here presented data.

Finally, the cumulative impact of device variation, flicker noise, and retention degradation of FeFETs on neural network applications have been evaluated. We consider inference operations on MLP-NN with *MNIST* data sets. Only the *READ* operation is performed during the inference operation. In this case, the retention of the data and the low-frequency noise-induced *READ* variation become crucial. The software baseline for the inference operation was 98.5%. Figure 7 shows the device-to-device variation (D2D), with the impact of low-frequency noise and retention degradation on the inference accuracy. The high on-current to the off-current ratio in FeFETs with SiON-based *IL* engenders better inference accuracy in NNs built with them. Low-frequency noise originates from intrinsic defects in the interface and ferroelectric layer, and each defect site has a different ionization energy [TSA_2]. This is why we observe a dependence of noise current and inference accuracy on the bias voltage. However, device variations and low-frequency noise impact are marginal in NNs with a synaptic core built with any type of FeFETs. The retention degradation causes closure of the MW in FeFETs with SiO_2*IL*, which is the pivotal reason behind the failure of them to operate as synaptic devices after aging. We have evaluated the cumulative impact of device variation, low-frequency noise, and retention degradation in the inference accuracy degradation, which shows that MLP-NN built with FeFETs with SiON-based *IL* shows excellent immunity to all three sources of variations and maintains accuracy over 96% after 10 years of programming without retraining.

CONCLUSION

We have fabricated FeFET devices with silicon-doped hafnium oxide as a ferroelectric layer. Fabrication was carried out in two

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different splits with SiO_2 and SiON as the interfacial layer between the semiconductor and the ferroelectric layer. Although the FeFET devices with the SiO_2 interface demonstrated excellent noise immunity, FeFET with the SiON interface showed a one order increase in the write endurance, without retention penalty. This improvement paved the way for this device to be implemented as the synaptic cells in inference engine applications.

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Yannick Raffel, Sourav De, and Maximilian Lederer contributed equally to this work.

Notes

The authors declare no competing financial interest.

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