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An Improved 4H-SiC MESFET with a Partially Low Doped Channel

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Abstract: An improved 4H-SiC metal semiconductor field effect transistor (MESFET) based on the double-recessed MESFET (DR-MESFET) for high power added efficiency (PAE) is designed and simulated in this paper and its mechanism is explored by co-simulation of ADS and ISE-TCAD software. This structure has a partially low doped channel (PLDC) under the gate, which increases the PAE of the device by decreasing the absolute value of the threshold voltage (V_t), gate-source capacitance (C_{gs}) and saturation current (I_d). The simulated results show that with the increase of H, the PAE of the device increases and then decreases when the value of N_{PLDC} is low enough. The doping concentration and thickness of the PLDC are respectively optimized to be $N_{PLDC} = 1 \times 10^{15}$ cm^{-3} and $H = 0.15$ μm to obtain the best PAE. The maximum PAE obtained from the PLDC-MESFET is 43.67%, while the PAE of the DR-MESFET is 23.43%; the optimized PAE is increased by 86.38%.

Keywords: 4H-SiC; MESFET; simulation; PAE

1. Introduction

With the development of the semiconductor industry, SiC, diamond and GaN, the third-generation semiconductor materials, have become a research hotspot because of their high critical field strength, wide band gap and high carrier saturation rate [1–6]. 4H-SiC is used to manufacture power devices such as MESFETs due to its larger band gap and higher electron mobility compared to those of 3C-SiC and 6H-SiC [7]. Nowadays, the mainstream research direction on 4H-SiC MESFETs is to achieve better output power density by making changes to the device structure [8,9]. However, in order to achieve green development, enabling devices to have higher energy conversion efficiency has become a new central issue of research. In the papers An Improved DRBL AlGaN/GaN HEMT with High Power Added Efficiency [10] and An Improved UU-MESFET with High Power Added Efficiency [11], a higher power added efficiency (PAE) was obtained by balancing the parameters of the devices. The PAE of the improved with an ultrahigh upper gate MESFET (IUU-MESFET) and the double recessed barrier layer (DRBL) AlGaN/GaN HEMT increased 18% and 48%, respectively. In the aforementioned research works, PAE simply replaces the RF output power with the difference between output and input power in the drain efficiency equation. A larger PAE means that a larger output power can be obtained under the same input power. This is crucial for sustainable development.

In this paper, an improved 4H-SiC MESFET with a partially low doped channel (PLDC) is designed and simulated to improve the PAE of the 4H-SiC DR-MESFET [12] using ISE-TCAD and ADS. A partially low doped channel is used to balance the parameters of the device by adjusting the doping concentration and thickness. The key to this structure is to improve the AC/RF characteristics of the device and improve the PAE of the device. This ensures that the device has lower energy consumption at the same output power, which has great significance for RF power amplifier applications. In the second part of this paper, the basic features and simulation process of the PLDC-MESFET are introduced, as are the models used in the simulation. In the third section, the main impact of the PLDC on the parameters and PAE of the device is introduced and the mechanism is discussed. In the fourth section, we conclude that the PLDC is helpful for the improvement of the PAE of the DR-MESFET.

2. Device Structure

The 2D schematic cross-sections of the DR-MESFET and PLDC-MESFET structures are shown in Figure 1a,b, respectively. The difference between the two devices is that the PLDC-MESFET has a partially low doped channel under the gate. The PLDC was realized by high-energy ion implantation and high-temperature annealing processes. It should be noted that the P-type impurity is implanted to compensate for the formation of lightly doped regions [13]. The thickness and the concentration of the PLDC are denoted as H and N_{PLDC}, respectively. The N_{PLDC} was set to 1×10^{17} cm^{-3}, 1×10^{16} cm^{-3} and 1×10^{15} cm^{-3}. The H was set from 0 to 0.25 μm in a step of 0.05 μm.

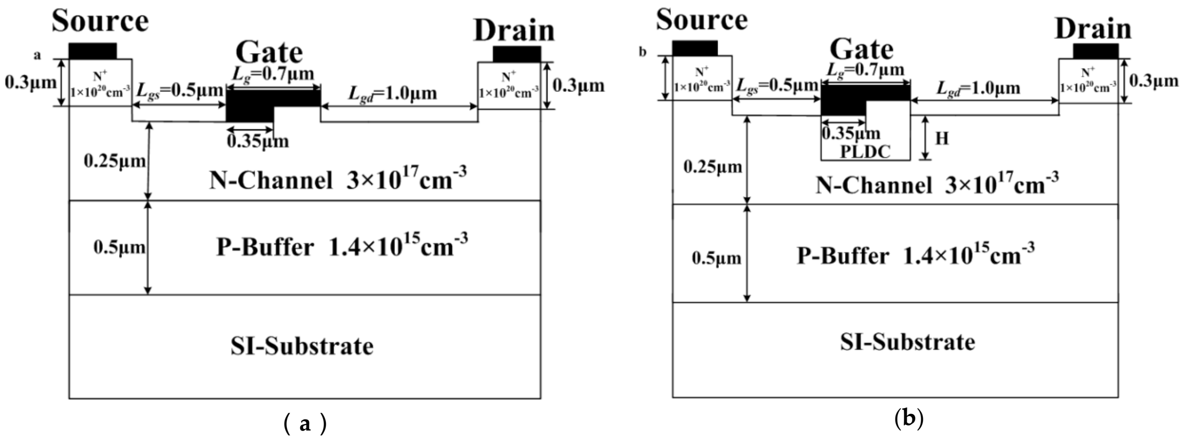


Figure 1. Schematic cross-sections of the (**a**) DR 4H-SiC MESFET, (**b**) partially low doped channel (PLDC) 4H-SiC MESFET.

The main physics models were applied in ISE-TCAD tools simulation [14], including Mobility (Doping Dep, HighFieldSat Enormal), Effective Intrinsic Density (Band Gap Narrowing (OldSlotboom), Incomplete Ionization, Recombination (SRH (Doping Dep) and Auger Avalanche (Eparallel). The criterion of breakdown was Break Criteria {Current (Contact = "gate" Absval = 1e3)}. The main solving model was Coupled {Poisson Electron Hole}. Mobility models were used to solve the phenomenon of the mobility of carriers being degraded by many factors. Recombination models were used to calculating the lifetime of carriers. The Effective Intrinsic Density model was used to calculate the effective band gap. Incomplete Ionization must be considered, as this occurs in the case of aluminum acceptors in silicon carbide. The temperature of the simulations was 300 K. The major parameters of the device measured were saturation current (I_{d}), threshold voltage (V_{t}), gate–source capacitance (C_{gs}) and transconductance (g_{m}). Those parameters are used in ADS to modify the EE_FET3 model. The modified EE_FET3 model and "Load-Pull PAE, Output Power Contours" model [15] were used to measure the PAE of the device under the same bias conditions. The working bias conditions were set as follows: V_{gs} was −8.0 V, V_{ds} was 28 V, RF was 850 MHz and Pavs_dBm was 28 dBm. Keeping the bias condition and changing the parameters obtained from ISE-TCAD, the PAE of the device under different thicknesses and doping concentrations can be calculated as follows [16].

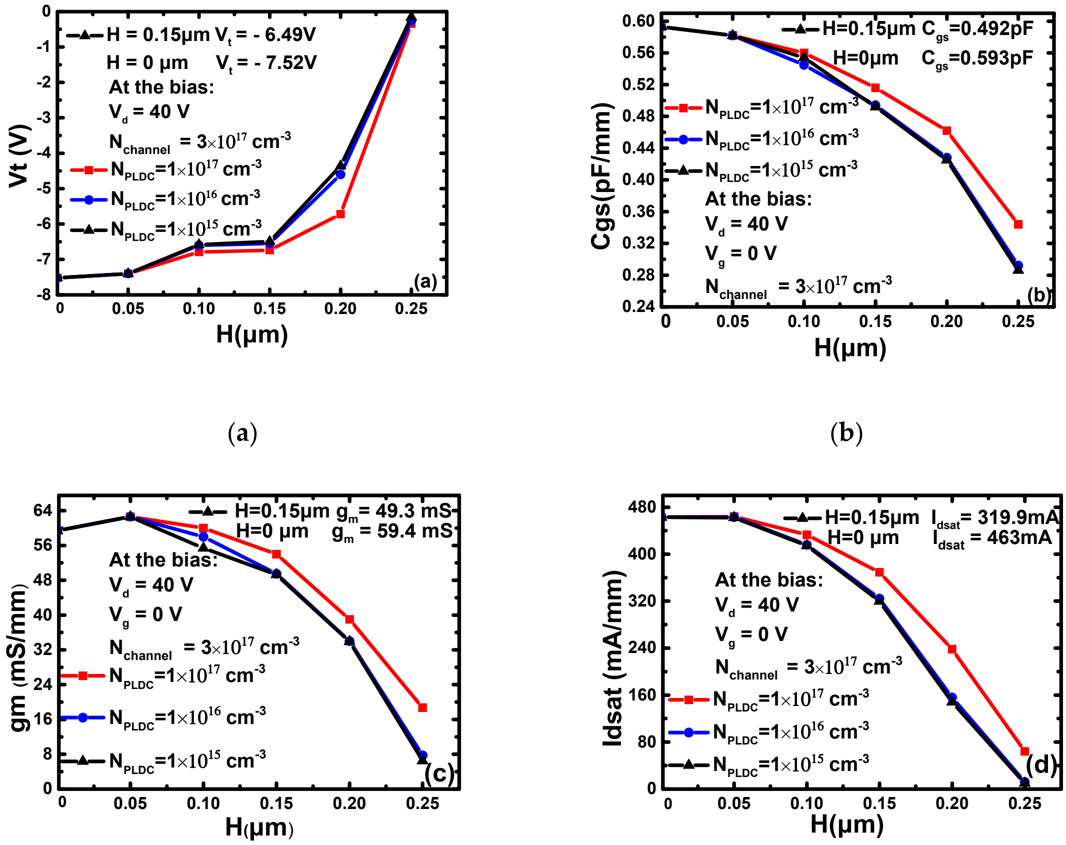
$$\eta(\mathrm{PAE}) = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} \quad (1)$$

where P_{out} is output power, P_{in} is input power and P_{dc} is DC power.

3. Results and Discussion

3.1. The Effect of Doping Concentration and Thickness On the Device Parameters

As showing in Figure 2, the parameters of the device are greatly affected by the doping concentration (N_{PLDC}) and thickness (H) of the PLDC. The effect of N_{PLDC} and H on V_{t} is shown in Figure 2a. With the decrease of N_{PLDC}, the absolute value of V_{t} decreases obviously. When H increases, the V_{t} overall trend is also decreasing. This is because the changes in N_{PLDC} and H directly control the total carrier concentration in the channel, and V_{t} is proportional to the total carrier. Figure 2b shows the effects of N_{PLDC} and H on C_{gs}. With the decrease of N_{PLDC} and the increase of H, C_{gs} decreases. On the one hand, the PLDC suppresses the under-gate depletion layer extending to the source side, and on the other hand, it reduces the total number of carriers in the channel, thereby reducing the input capacitance of the device. In the Figure 2c, g_{m} increases first and then decreases. The reason for this formation may be that the thinner low doped layer can increase the gate's ability to control the current by inhibiting the diffusion of the depletion layer to some extent. When H is thick enough, the ability of the gate to control the current will be reduced. So, g_{m} decreases. In Figure 2d, I_{dsat} is roughly decreased as H increases and N_{PLDC} decreases. This is mainly caused by the decrease of the channel carrier concentration. When H is 0.25 μm, the parameters exhibit a sharp decrease and the DC characteristic of the device becomes poor. It is indicated by the simulation results that the PLDC-MESFET has smaller values of C_{gs}, g_{m}, V_{t} and I_{dsat} as compared to those of the original device.



(a) (b)

(c) (d)

Figure 2. The effect of N_{PLDC} and H on the device parameters: (**a**) V_{t}-N_{PLDC} and H, (**b**) C_{gs}-N_{PLDC} and H, (**c**) g_{m}-N_{PLDC} and H, (**d**) I_{dsat}-N_{PLDC} and H.

3.2. The Influences of Doping Concentration and Thickness on the PAE

The influences of the doping concentration and thickness on the PAE are shown in Figure 3. It can be seen that when H is smaller than 0.20 µm, the PAE of the device increases with the decrease of N_{PLDC}. When H is 0.20 µm and N_{PLDC} is 1×10^{15} cm^{-3} or 1×10^{16} cm^{-3}, the PAE of the device decreases sharply. When H is 0.20 µm and N_{PLDC} is 1×10^{17} cm^{-3}, the PAE of the device increases. When H is 0.25 µm, the simulation results show that the DC characteristics and AC characteristics of the device are poor, and the PAE of these structures is low. The maximum value of the PAE is obtained when the N_{PLDC} is 1×10^{15} cm^{-3}, the H is 0.15 µm. The PAE of the new device is 43.67% while the PAE of the original device is 23.43%. The optimized PAE is increased by 86.38%. The PAE of the IUU-MESFET and DRBL AlGaN/GaN HEMT increase 18% and 48%, respectively. So, the PLDC has a great effect on improving the PAE of the device. In the paper *107 W CW SiC MESFET with 48.1% PAE*, the experimental PAE of the device at 2 W (33 dBm) is close to 25% [17]. The PAE of the DR-MESFET is 23.43% at 0.63 W (28 dBm). This is essentially consistent with the simulation results.

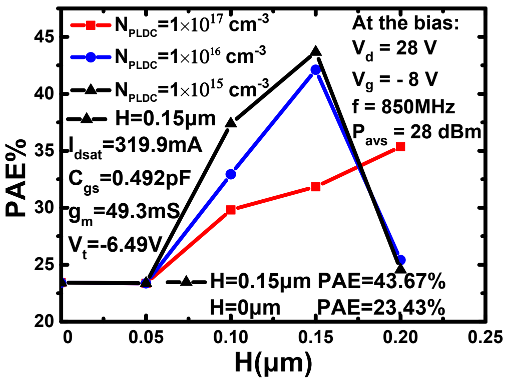
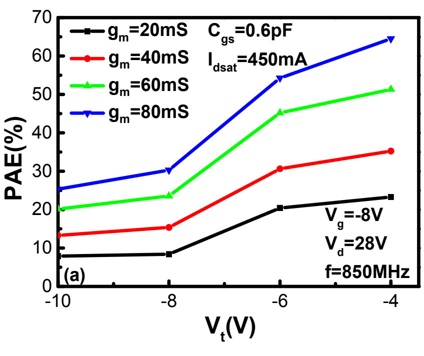


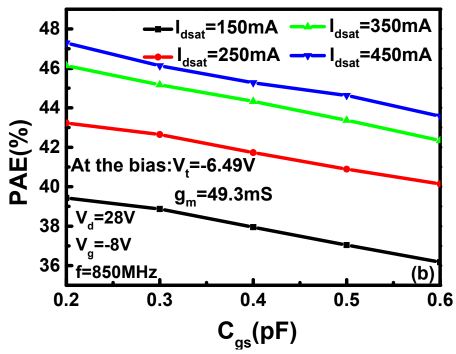
Figure 3. The effects of N_{PLDC} and H on the PAE.

3.3. Mechanism Discussion

Figure 4a,b shows the influence of the parameters on PAE at the same bias when V_{gs} is −8.0 V, V_{ds} is 28 V, RF is 850 MHz and Pavs_dBm is 28 dBm. As shown in Figure 4a, the PAE increases with the increase of V_{t} when g_{m} is a constant. When V_{t} is a constant, the PAE also increases with the increase of g_{m}. When g_{m} is between 40 and 60 mS, the PAE of the device has the biggest change. This can be observed by the distance between the two curves. Figure 4b shows the influence of I_{dsat} and C_{gs} on the PAE. With the increase of C_{gs}, the PAE decreases. With the increase of I_{dsat}, the PAE increase. Furthermore, the larger I_{dsat} is, the slower PAE increases.



(**a**)



(**b**)

Figure 4. The effect of device parameters on PAE: (**a**) PAE-V_t and g_m, (**b**) PAE-C_{gs} and I_{dsat}.

From the analysis above, it can be concluded that the smaller the absolute value of V_t, the bigger the PAE, and the smaller the C_{gs}, the bigger the PAE. For g_m, a bigger g_m means a higher current gain, so it a larger output can be obtained under the same input. According to Figure 4a, the PAE is proportional to g_m. This is the reason why the PAE of the device decreases sharply when H is 0.20 µm and N_{PLDC} is 1×10^{15} cm^{-3} or 1×10^{16} cm^{-3}. When H is 0.20 µm and N_{PLDC} is 1×10^{17} cm^{-3}, the PAE of the device increases because g_m is not the key factor compared with V_t, I_{dsat} and C_{gs}. The PAE of the device is decided by the influences of those parameters.

It can be seen that the doping concentration and thickness of the PLDC are optimized to be N_{PLDC} = 1×10^{15} cm^{-3} and H = 0.15 µm. Table 1 shows some main parameters of the two devices. It can be seen that the PAE of the PLDC-MESFET is 43.67%, which is higher than the PAE of 23.43% of the DR-MESFET. Compared the two devices, the PLDC-MESFET has a smaller threshold voltage, smaller input capacitance, smaller transconductance and smaller saturation current than the DR-MESFET. The increase of the PAE is influenced by the combination of these parameters. When the absolute value of V_t decreases, the device is easier to turn on and gains a larger output current. So, the output power P_{out} increases and a higher PAE is reached. According to Formula (2) [16], a smaller input capacitance C_{gs} means the device has less energy loss when working in RF (charging and discharging).

$$P_{dyn} = E_{VD} - E_c = \int_0^\infty i_{vd}(t) V_d dt - \int_0^\infty i_{vd}(t) v_{out} dt = C V_D{}^2 - \frac{C V_D^2}{2} = \frac{C V_D^2}{2} \quad (2)$$

where P_{dyn} is the dynamic power consumption flipped once, E_{VD} is the energy obtained from the power source, E_c is the capacitor stored energy, C is the gate–source capacitor and V_D is the drain voltage. A small C_{gs} also increases the input impedance of the device. Therefore, P_{out} of the device increases and P_{in} decreases. For I_{dsat}, a small I_{dsat} indicates a small P_{out}. Under the influence of these parameters, the device has a big PAE. In there, g_m is sacrificed to obtain a higher PAE. Though a larger g_m is helpful to increase PAE, the influences of the other parameters on PAE are more obvious. So, the maximum value of PAE is 43.67% when N_{PLDC} is 1×10^{15} cm^{-3} and H is 0.15 µm, as obtained by sacrificing some of the DC performances of the device.

Table 1. Comparison of performance parameters of the two structures.

Parameters	DR 4H-SiC MESFET	PLDC 4H-SiC MESFET
I_{dsat} (mA/mm)	448.00	319.90
V_b (V)	125.35	130.20
g_m (mS/mm)	59.30	49.30
V_t (V)	−7.52	−6.49
C_{gs} (pF/mm)	0.59	0.49
PAE (%)	23.43	43.67

4. Conclusions

An improved 4H-SiC MESFET with a partially low doped channel is designed and simulated in this paper to increase the PAE of the device. The results show that the maximum PAE of the PLDC-MESFET is 43.67%, while the PAE of the DR-MESFET is 23.43%; the optimized PAE was increased by 86.38%. A way to design an energy efficient amplifier is proposed in this paper by balancing the parameters of the device. This ensures that the device has lower energy consumption at the same output power, which has great significance for RF power amplifier applications.

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Conflicts of Interest: The authors declare no conflict of interest.

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