Sb-mediated Ge quantum dots in Ti–oxide–Si diode: negative differential capacitance

Victor-Tapio Rangel-Kuoppa[1]**, Alexander Tonkikh**[2,3]**, Peter Werner**[2] **and Wolfgang Jantsch**[1]

[1] Institute of Semiconductor and Solid State Physics, Johannes Kepler Universität, A-4040 Linz, Austria
[2] Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany
[3] Institute for Physics of Microstructures RAS, Nizhniy Novgorod, Russia

E-mail: tapio.rangel@gmail.com and tonkikh@mpi-halle.mpg.de

Abstract
The negative differential capacitance (NDC) effect is observed on a titanium–oxide–silicon structure, formed on n-type silicon with embedded germanium quantum dots (QDs). The Ge QDs were grown by an Sb-mediated technique. The NDC effect was observed for temperatures below 200 K. We found that approximately six to eight electrons can be trapped in the valence band states of Ge QDs. We explain the NDC effect in terms of the emission of electrons from valence band states in the very narrow QD layer under reverse bias.

1. Introduction

SiGe quantum dots (QDs) have been a hot research topic in recent years. They are easily incorporated into the well-developed SiGe technology and they have been extensively studied with respect to their quantum confinement properties. It is expected that these confinement properties will open up the possibility of new technological and industrial applications. For example, photoresponse has been observed in the spectral range of $3–4\,\mu$m by several groups, making SiGe QDs candidates for midinfrared spectral photodetectors [1]. At the same time, if the QDs are small enough, they can confine down to single electrons in individual QDs, which makes them promising candidates for Si-compatible spin-based quantum information processing [2]. There have also been suggestions that they might serve as building blocks for quantum information

processing, due to entanglement of confined electrons, holes or excitons, in case the QDs are coupled [3].

Optical and photovoltaic energy saving applications have also been proposed. For example, SiGe QDs could improve the solar cell efficiency, via the introduction of an intermediate band [4, 5]. Regarding efficient energy use and applications, SiGe QDs have proven to significantly reduce the thermal conductivity while maintaining high electrical conductivity, opening the field for their thermoelectrical use [6, 7].

This vast spectrum of possibilities has triggered fundamental research on them. Several basic experimental and theoretical studies can be found [8–17].

At the same time, the negative differential capacitance (NDC) is an interesting effect, where the derivative of the capacitance voltage (CV) plot is negative in some voltage range [18]. It has found interesting applications, such as in a metal–semiconductor field-effect transistor [19]. So far, NDC has been reported in amorphous Si [20] and in n-GaN–p-Si heterojunctions [21]. If a SiGe-based device could be developed showing the NDC effect, it will widen even more the already vast technological application

spectrum of the SiGe system. It is the intention of this paper to report and explain the observation of NDC on a metal–oxide–semiconductor (MOS) structure, based on the SiGe system.

This paper is divided into the following sections. In section 2, the details of the fabrication process of samples are given together with the description of characterization methods of atomic force microscopy (AFM) and CV. In section 3, a model is proposed and applied. The discussion of experimental results and their interpretation based on the Gaussian distribution of an energy band within the valence band offset of the Ge QDs are given. We verify our model using simulations of CV measurements. Finally, a summary is given in section 4.

2. Experiment and results

Two samples were grown using molecular beam epitaxy on n-type Si(100) substrates having a resistivity of about $5\,\Omega\,\text{cm}$. One of the sample types we investigated consists of a 200 nm Si buffer layer, a Ge QD layer and a 66 nm thick Si cap layer. Both buffer and capping Si layers were doped with Sb up to a level of $1 \times 10^{18}\,\text{cm}^{-3}$. The doping of Si layers was performed at the growth temperature of $450\,^\circ\text{C}$ to reduce Sb segregation. The growth temperature of the Ge QD layer was $600\,^\circ\text{C}$, adopting the procedure of QD formation reported elsewhere [22]. Another reference sample was grown under the same growth conditions but without the Si cap layer. This sample was studied using AFM in order to determine the surface density of Ge QDs. We assume that despite the capping stage in the first type of samples, the surface density of Ge QDs is equal to that of the uncapped sample. However, the Ge QD sizes may differ in these two types of samples, since during their capping Sb affects processes of Si–Ge intermixing and Ge segregation [23].

Figure 1 shows an AFM image of the uncapped sample. The density of Ge QDs is $N_{\text{dot}} = 1.3 \times 10^{11}\,\text{cm}^{-2}$. These Ge islands have an average basis size of 13 nm and an average height of 1.2 nm. We have to point out that the mean height of capped Ge QDs is somewhat larger (up to 3.0 nm), as reported previously [14].

After growth the capped samples were prepared for electrical characterization in a similar way to our former studies [13–15]. Briefly, they were first covered with 200 nm SiO$_2$ by plasma-enhanced chemical vapor deposition. An alloyed AuSb ohmic contact had been formed before on the back of the substrate. The alloying temperature was $360\,^\circ\text{C}$ for 5 min in a N$_2$ atmosphere. The standard photolithographic techniques, reported in [24], were slightly modified and used in this study. In [24], the etching process was carried out to remove completely the SiO$_2$ layer in the desired places. As the intention of this work is to study a MOS structure, this process was slightly modified in the following way. In this work, the SiO$_2$ was etched using a buffered hydrofluoric acid solution from microposit$^\copyright$. The etching rate was approximately $2\,\text{nm s}^{-1}$. In the desired areas, SiO$_2$ was etched during a carefully monitored time of 95 s. With this procedure, an $\sim$10 nm SiO$_2$ was left in the desired positions. The area of
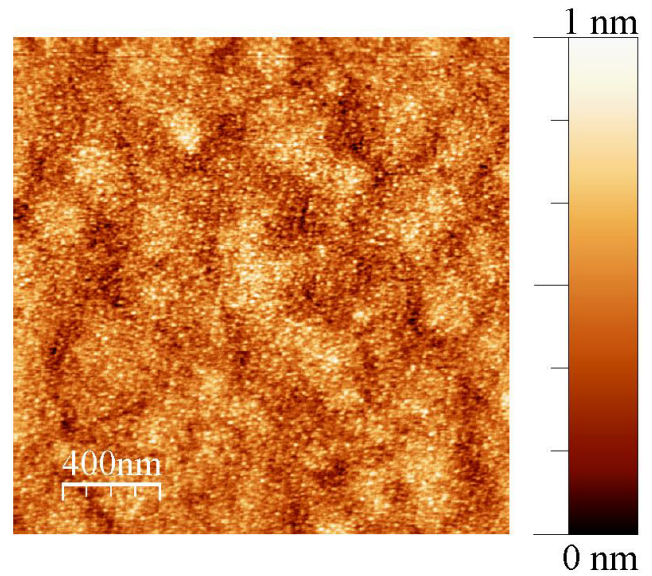

Figure 1. AFM image of the uncapped sample, which reveals a QD surface density of $1.3 \times 10^{11}\,\text{cm}^{-2}$. The Ge QDs are on average 1.2 nm high with lateral dimensions of 13 nm.

these etched positions was $A = 0.3\,\text{mm}^2$. Continuing with the usual photolithographic process, titanium was deposited on these places, to achieve the desired MOS structures. The sample was glued to the sample holder with fixogum, to ensure good thermal contact [25].

CV measurements were performed at temperatures T from 280 to 160 K, in 20 K steps. For clarity they are shown in two separate plots, figures 2(a) and (b). The measurement frequency ω was 1 MHz. At the same time, the equivalent series resistance R_s was measured at every temperature and reverse bias. The quality factor $Q = \omega C_S R_s$ was calculated, and it was found to be $Q = 1$. Thus, the measurements were not distorted by any large internal resistance effect [26].

The total capacitance C_{Tot} of a MOS structure (in the depletion region working range) is related to the capacitance due to the oxide layer C_{Oxi} and the applied reverse bias V by [27]

$$C_{\text{Tot}} = \frac{C_{\text{Oxi}}}{\sqrt{1 + \frac{2C_{\text{Oxi}}^2(V_{\text{FB}} - V)}{A^2 q \varepsilon_{\text{Si}} n}}}, \tag{1}$$

where V_{FB} is the flat band voltage, defined according to [27], $\varepsilon_{\text{Si}} = 11.7 \times \varepsilon_0$ is the dielectric permittivity of Si, $\varepsilon_0 = 8.85\,\text{pF m}^{-1}$ is the dielectric permittivity of vacuum, $q = 1.6 \times 10^{-19}\,\text{C}$ is the elementary charge of the electron, n is the electron charge carrier density and C_{Oxi} is a constant given by

$$C_{\text{Oxi}} = \frac{\varepsilon_{\text{SiO}_x} A}{t_{\text{Oxi}}}, \tag{2}$$

where $\varepsilon_{\text{SiO}_x} = 3.9 \times \varepsilon_0$ is the dielectric permittivity of SiO$_x$ and t_{Oxi} is the oxide thickness.

For completeness purposes, the definition V_{FB} is given by

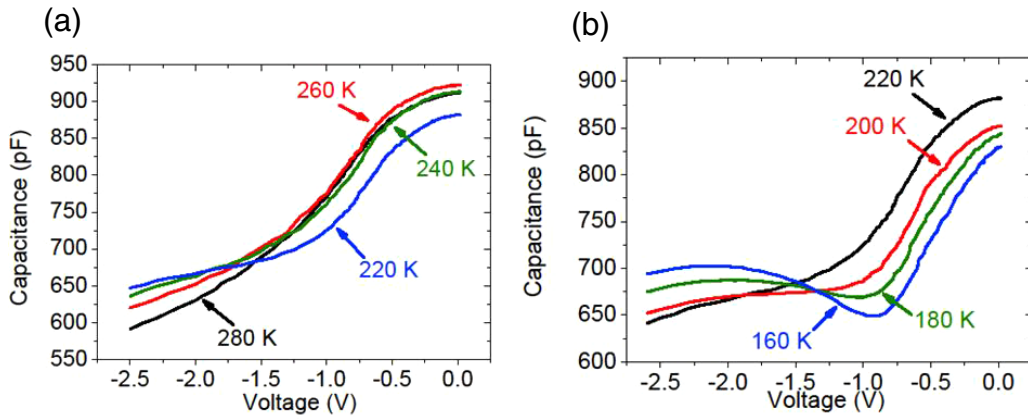$$V_{\text{FB}} = - (\varphi_{\text{n}+} - \varphi_{\text{n}}), \tag{3}$$

(a)

(b)

Figure 2. CV measurements done at (a) 280, 260, 240 and 220 K, and (b) 220, 200, 180 and 160 K.

where $\varphi_{n+} = 550\,\text{mV}$ and

$$\varphi_n = v_{th} \log_{10}\left(\frac{n}{n_i}\right), \tag{4}$$

where $v_{th} = \frac{kT}{q}$ (k is the Boltzmann constant and T is the absolute temperature) and n_i is the intrinsic carrier concentration of Si, given by $n_i = \left(9.38 \times 10^{19}\,\text{cm}^{-3}\right) \left(\frac{T}{300\,\text{K}}\right)^2 \exp\left(-\frac{6884\,\text{K}}{T}\right)$ [28]. Further details about equations (3) and (4) can be found in [27].

An alternative expression to equation (1) is

$$\frac{1}{C_{\text{Tot}}} = \frac{1}{C_{\text{Oxi}}} + \frac{1}{C_{\text{Sc}}}, \tag{5}$$

where C_{Sc} is the capacitance due to the depletion region within the semiconductor [27], and it is given by

$$C_{\text{Sc}} = \frac{\varepsilon_{\text{Si}} A}{t_{\text{Sc}}}, \tag{6}$$

where t_{Sc} is the depletion region inside the semiconductor, given by

$$t_{\text{Sc}} = \frac{t_{\text{Oxi}} \varepsilon_{\text{Si}}}{\varepsilon_{\text{SiO}_x}} \left\{ \sqrt{1 + \frac{2 C_{\text{Oxi}}^2 (V_{\text{FB}} - V)}{A^2 q \varepsilon_{\text{Si}} n}} - 1 \right\}. \tag{7}$$

Equations (1) and (5)–(7) are valid in the range where $V_T < V < V_{\text{FB}}$, where V_T is the threshold voltage defined according to [27].

Another important working region for MOS structures, which is used in this study, is the accumulation working region [27]. The accumulation region is defined by $V_{\text{FB}} < V$ [27]. In the accumulation region, $C_{\text{Tot}} = C_{\text{Oxi}}$, and particularly for MOS structures in n-type semiconductors (as is the case in this study), the accumulation region occurs already close to zero bias. This phenomenon is observed in figures 2(a) and (b) close to zero bias: the capacitance is almost constant. The value of C_{Tot} at zero bias decreases with temperature from 923 pF at room temperature to 829 pF at 160 K. Using equation (2), a value of t_{Oxi} between 11.2 and 12.4 nm is obtained, in reasonable agreement with the desired value that was aimed at during the processing of the

sample. The differences at zero bias at different temperatures can be explained assuming interfacial-oxide charge, varying with temperature. As shown below, the Fermi energy E_F gets closer to the conduction band minimum E_C as T decreases. This changes the population of interfacial or oxide charge, explaining the reduction of capacitance at zero bias as T decreases, as has been done in other studies [27, 29–31]. Also, the voltage region where C_{Tot} is roughly constant (close to zero bias) becomes smaller as T decreases. This is explained further below.

There is a third working region for a MOS structure, namely, the inversion region [27]. In the inversion region, $C_{\text{Tot}} = C_{\text{Oxi}}$. This working region occurs when $V < V_T$, where V_T is the threshold voltage, defined by $V_T = V_{\text{FB}} - 2\varphi_n - \frac{1}{C_{\text{ox}}} \sqrt{2 q \varepsilon_S n (2\varphi_n)}$ [27]. Calculations using the values reported below reveal that in this study always $V_T < -3\,\text{V}$. Hence, our sample is never reverse biased into the inversion region.

The usual C^{-2} versus V analysis [32] can also be used for MOS structures in the depletion region. In this case, using equation (1), the expression of C_{Tot}^{-2} is given by

$$C_{\text{Tot}}^{-2} = \left\{ \frac{1}{C_{\text{Oxi}}^2} + \frac{2 V_{\text{FB}}}{A^2 q \varepsilon_{\text{Si}} n} \right\} - \frac{2}{A^2 q \varepsilon_{\text{Si}} n} V. \tag{8}$$

The slope of the linear fit of the function C_{Tot}^{-2} versus V yields n. This is shown in figures 3(a)–(h).

The deduced values for n are plotted in figure 4 together with results for $E_C - E_F$, which have been derived using the usual relation for non-degenerate semiconductors [33]:

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right), \tag{9}$$

where $N_C = \left(6.2 \times 10^{15}\,\text{cm}^{-3}\right) T^{3/2}$ [33].

The expected value of n is obtained, and E_F evolves as a function of T as reported in [34]. It is useful to plot V_{FB} versus T to access the depletion region width used in the following analysis. These dependences are plotted in figures 4 and 5 using equations (4) and (5). The Debye length, $L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 n}}$, is also shown in figure 5. L_D characterizes the depth resolution of the CV doping profile technique [32]. The obtained parameters will be used in the subsequent analysis below.
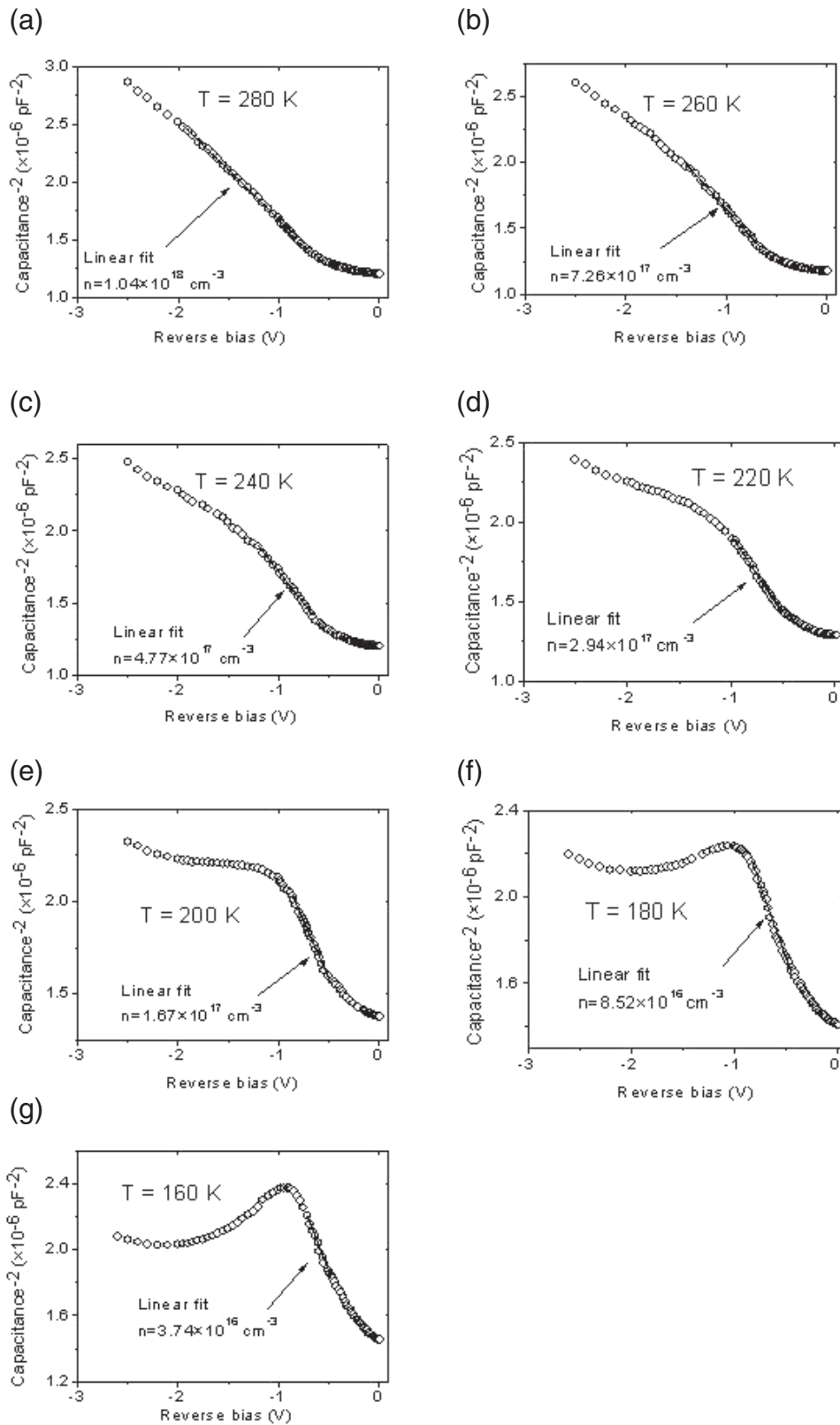
Figure 3. C^{-2} vs V analysis done at (a) 280, (b) 260, (c) 240, (d) 220, (e) 200, (f) 180 and (g) 160 K.

The value of V_{FB} increases from -60 to -10 mV, as T decreases from 280 to 160 K. This means that the accumulation working region becomes narrower, explaining why the voltage range where C_{Tot} is almost constant diminishes as T diminishes. This fact suggests that the best temperatures to analyze the electrical effect of Ge QDs are precisely those at the lowest temperatures, as most of the CV curve is in the depletion working region, i.e. where equation (1) is valid. At the same time, L_D is practically constant, around a value between 3.0 and 3.6 nm.
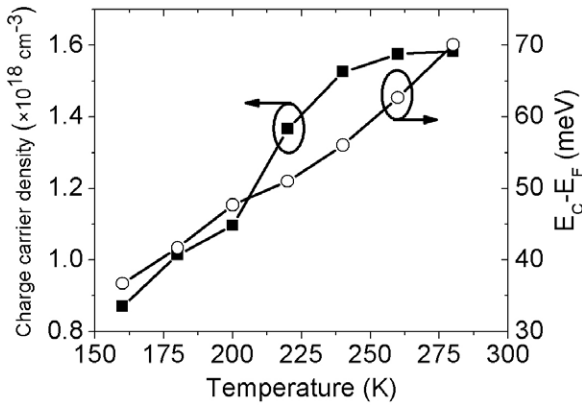
Figure 4. Charge carrier density n (using the left y-axis) and Fermi level position E_F relative to the bottom of the conduction band E_C, $E_C - E_F$ (using the right y-axis), as a function of temperature.
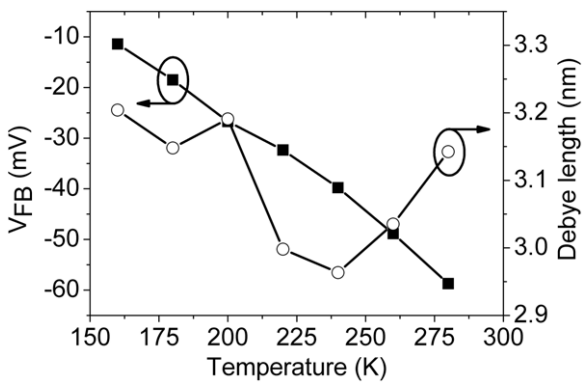

Figure 5. Flat-band voltage V_{FB} (using the left y-axis) and Debye length L_D (using the right y-axis), as a function of temperature.

In order to estimate the number of electrons (e$^-$s) that are trapped in Ge QDs, we investigate the plateau in the CV plot shown in figure 2(b) (the curve at $T = 200$ K). This plateau is due to electrons trapped in Ge QDs [35]. Their concentration is estimated by $\Delta Q = C_{plat} \Delta V$, where C_{plat} is the constant value of the capacitance in the plateau (in this case 673 pF), and ΔV is the voltage range where the plateau exists, in this case between -1.8 and -1.1 V, i.e. $\Delta V = -1.1$ V$-(-1.8$ V$) = +0.7$ V. Hence, $\Delta Q = 4.71 \times 10^{-10}$ C, which is equivalent to $N^e = 2.94 \times 10^9$ electrons. Thus, the density of electrons trapped per unit area can be obtained dividing N^e by A, yielding $N^e_{Area} = 9.8 \times 10^{11}$ electrons cm^{-2}. The density of electrons trapped per QD is obtained as N^e_{Area} by N_{dot}, resulting in $N^e_{Dot} \sim 7.5$ electrons per QD. These electrons are trapped from the surroundings of the Ge QDs, leaving behind ionized ions, i.e. forming a depletion region close to the Ge QDs.

3. Model and discussion

In order to understand well the CV measurements, it is important to estimate the width of the depletion region around the Ge QDs. As mentioned, the best temperature to analyze the CV measurement is the lowest one, i.e. 160 K. Thus, the analysis will be done at this value of T. The depleted volume

that is necessary to obtain N^e is given by the relation $nAl = N^e$, where l is the depletion region width and n is the charge carrier density (8.69×10^{17} cm^{-3} at 160 K). A value of $l = 16$ nm is obtained. It is natural to expect that, due to the homogeneous doping, half of the depletion region is located below the Ge QDs and half of the depletion region above the Ge QDs. This depletion region causes a parabolic increase of the conduction band edge, as it gets closer to Ge QDs. This increase can be estimated by integrating the Poisson equation $\nabla^2 V = qn/\varepsilon_{Si}$ two times within the depletion region close to the Ge QDs (i.e. from 0 to $l/2 = 8$ nm). This yields an increase of ~ 43 meV. Since $V_{FB} = -10$ mV at 160 K, for reverse biases larger than this value, the band structure of the MOS structure inside the semiconductor side approaches the band structure of a Schottky one [27]. At the same time, the Ge QDs affect only the semiconductor side. Therefore, for clarity, in the following only the band structure in the semiconductor side is shown. A schematic view of the band structure at $V = 0$ V and $T = 160$ K is depicted in figure 6(a). The depletion region within the semiconductor is represented by the gray area.

At -1.0 V, the band structure looks similar to figure 6(b). The depletion region from the oxide is close to 55 nm, which is, within L_D resolution, reaching the depletion region on the left side of the Ge layer, which starts at around 60 nm. This is in agreement with the observation of the NDC effect that is observed at 160 and 180 K, starting approximately at -1.0 V, as the cap layer has been fully depleted reaching the Ge layer. Notice that the quasi-Fermi level E_F^* in the semiconductor side is at -1.0 eV, the value of the applied reverse bias of -1.0 V multiplied by the charge of the electron q. The energetic position of E_F^* is above the Ge QD well; thus, the electrons trapped in the valence states continue to be trapped, as they are energetically below E_F^*. The NDC effect starts, as the electrons will be dynamically removed from the valence states of the Ge QDs, as E_F^* decreases, crossing the valence states of the Ge QDs, depopulating them of electrons.

At -2.0 V, the band structure looks as in figure 6(c). The depletion region has gone over the Ge layer, and the NDC has taken place. Electrons have been removed or almost completely removed from the valence states. The NDC effect disappears around this voltage, as can be observed in figure 2(b) at 160 and 180 K.

Lin *et al* [18] and Chiquito *et al* [36] reported their observation of NDC in InAs QDs embedded in GaAs. They explained it by electrons trapped in deep states, below the Fermi level, which were dynamically emitted as the quasi-Fermi level decreased. In this study we propose a similar analysis, which is slightly modified due to the nature of our Ge QDs. In the model by Lin *et al* and Chiquito *et al*, it was assumed that there are discrete energy levels for their electrons trapped in their InAs QDs. In our case we consider an energy band of states within the valence band offset Ge QD–Si matrix. Due to the size dispersion of our Ge QDs, we consider that this subband includes the whole valence band offset. At -1.2 V, this means that this subband spans the energy range between -1.2 and -2.0 V.
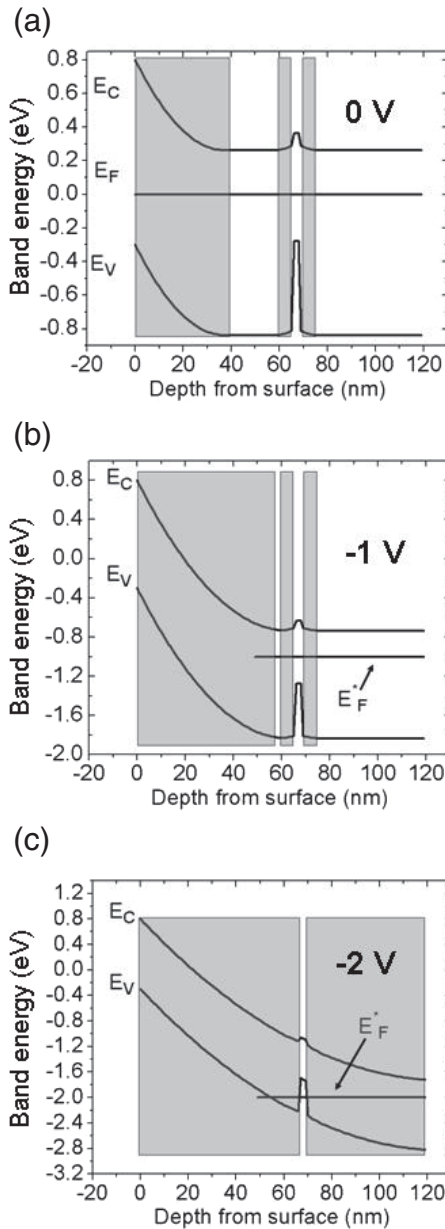
(a)

(b)

(c)

Figure 6. Schematic view of the band structure within the semiconductor side of the MOS structure at (a) 0 V, (b) -1.0 V and (c) -2.0 V. The gray areas represent depleted regions.

Hence, we assume density of states N_D with a Gaussian distribution per QD of the form

$$N_D = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(E-E_0)^2}{2\sigma^2}}. \tag{10}$$

The Fermi Dirac distribution of electrons at some energy E as a function of the reverse bias V will be given by

$$F_{FD} = \frac{1}{1+\exp\left(\frac{E-qV}{kT}\right)}, \tag{11}$$

where qV is the quasi-Fermi level within the semiconductor.

It is also necessary to introduce a parameter n_{QD}, which is the number of electrons trapped per QD, as the valence states
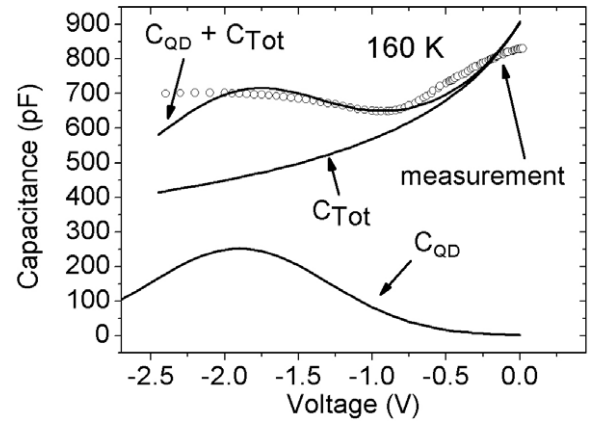

Figure 7. Measurement done at 160 K and simulations for the capacitance due to the MOS structure (C_{Tot}), the capacitance due to the QDs (C_{QD}) and the sum of both.

are not necessarily all populated with electrons. A reason for this may be Coulomb repulsion: once an electron is trapped, it will exert Coulomb repulsion on any other electron to be trapped. Thus, the total charge trapped in the QDs within the area A of our Schottky device (Q_{QD}) at some reverse bias V is given by

$$Q_{QD} = \int_{-\infty}^{\infty} q n_{QD} N_{dot} A N_D F_{FD} \, dE. \tag{12}$$

This expression has no analytical integral. It was computed numerically as a function of the reverse bias. Once this was done, the capacitance C_{QD} due to the emission of electrons from the Ge QDs is the derivative of equation (12) with respect to the reverse bias V:

$$C_{QD} = \frac{dQ_{QD}}{dV}. \tag{13}$$

Simulations were done to fit the CV measurement. An example of this simulation is shown in figure 7. The best fit of experimental results was achieved using a Gaussian distribution of electrons within the valence states of Ge QDs with fitting parameters $\sigma = 0.6$ V and $E_0 = -1.8$ eV, reasonably covering the valence band offset of the Ge QDs. Also, the value of n_{QD} close to 6.0 electrons per QD was obtained, in reasonable agreement with the 7.5 electrons per QD obtained from the plateau analysis at 200 K. It is noticeable that the largest discrepancy occurs for reverse biases larger than -2.0 V. This suggests that the Gaussian distribution approximation might not be valid for deep states close to the top of the valence band in Si, i.e. a larger density of states might happen as the energy gets closer to the top of the Si valence band.

4. Summary

The NDC effect was observed in Si-MOS structures. These MOS structures consist of Ti, 10 nm SiO$_2$ and the semiconductor structure. The semiconductor structure contains a Ge QD layer. The NDC effect is well explained

by electrons trapped in the valence states of the Ge QDs. These trapped electrons are emitted as the quasi-Fermi level in the semiconductor side crosses the electron trap energy levels depopulating them of electrons. This causes the appearance of the NDC effect. On average, approximately six to eight electrons are trapped per QD.

Acknowledgments

References

[1] Yakimov A I, Nikiforov A I, Timofeev V A, Bloshkin A A, Kirienko V V and Dvurechenskii A V 2011 *Semicond. Sci. Technol.* **26** 085018

[2] Ketharanathan S, Sinha S, Shumway J and Drucker J 2009 *J. Appl. Phys.* **105** 044312

[3] Yakimov A I, Mikhalyov G Y, Dvurechenskii A V and Nikiforov A I 2007 *J. Appl. Phys.* **102** 093714

[4] Kechiantz A M, Kocharyan L M and Kechiyants H M 2007 *Nanotechnology* **18** 405401

[5] Sun K W, Sue S H and Liu C W 2005 *Physica* E **28** 525

[6] Lacharmoise P D, Bernardi A, Goñi A R, Alonso M I, Garriga M, Lanzillotti-Kimura N D and Fainstein A 2007 *Phys. Rev.* B **76** 155311

[7] Alvarez-Quintana J, Alvarez X, Rodriguez-Viejo J, Jou D, Lacharmoise P D, Bernardi A, Goñi A R and Alonso M I 2008 *Appl. Phys. Lett.* **93** 013112

[8] Yakimov A, Dvurechenskii A V, Nikiforov A I, Bloshkin A A, Nenashev A V and Volodin V A 2006 *Phys. Rev.* B **73** 115333

[9] Yakimov A, Dvurechenskii A V, Volodin V A, Efremov M D, Nikiforov A I and Mikhalyov G Y 2005 *Phys. Rev.* B **72** 115318

[10] Drucker J 2002 *IEEE J. Quantum Electron.* **38** 975

[11] Brunner K 2002 *Rep. Prog. Phys.* **65** 27

[12] Zhang S K, Zhu H J, Lu F, Jiang Z M and Wang X 1998 *Phys. Rev. Lett.* **80** 3340

[13] Rangel-Kuoppa V-T, Chen G and Jantsch W 2011 *AIP Conf. Proc.* **1399** 379

[14] Rangel-Kuoppa V-T, Tonkikh A, Zakharov N, Werner P and Jantsch W 2011 *Solid State Phenom.* **178** 72

[15] Rangel-Kuoppa V-T, Chen G and Jantsch W 2011 *Solid State Phenom.* **178** 67

[16] Hérnandez-Hérnandez A, Rangel-Kuoppa V-T, Plach T, De Moure-Flores F, Quiñones-Galvan J G, Zepeda K E N, Zapata-Torres M and Meléndez-Lira M 2011 *Solid State Phenom.* **178** 61

[17] Hérnandez-Hérnandez A, Rangel-Kuoppa V-T, Plach T, De Moure-Flores F, Quiñones-Galvan J G, Zapata-Torres M, Hérnandez-Hérnandez L A and Meléndez-Lira M 2012 *J. Appl. Phys.* **111** 044327

[18] Lin S D, Ilchenko V V, Marin V V, Shkil N V, Buyanin A A, Panarin K Y and Tretyak O V 2007 *Appl. Phys. Lett.* **90** 263114

[19] Ershov M, Liu H C, Li L, Buchanan M, Wasilewski Z R and Jonscher A K 1998 *IEEE Trans. Electron Devices* **45** 2196

[20] Chen I and Jansen F 1990 *J. Appl. Phys.* **67** 7383

[21] Kumar M, Bhat T N, Rajpalke M K, Roul B, Sinha N, Kalghatgi A T and Krupanidhi S B 2011 *Solid State Commun.* **151** 356

[22] Tonkikh A, Zakharov N, Talalaev V and Werner P 2010 *Phys. Status Solidi RRL* **4** 224

[23] Tonkikh A A, Zakharov N D, Pippel E and Werner P 2011 *Thin Solid Films* **519** 3669

[24] Rangel-Kuoppa V-T and Conde-Gallardo A 2010 *Thin Solid Films* **519** 453

[25] Rangel-Kuoppa V-T and Chen G 2010 *Rev. Sci. Instrum.* **81** 036102

[26] Rangel-Kuoppa V-T and Pessa M 2003 *Rev. Sci. Instrum* **74** 4561

[27] Howe R T and Sodine Ch S 1997 *Microelectronis, an Integrated Approach* (Englewood Cliffs, NJ: Prentice-Hall) pp 136–92

[28] Sproul A B and Green M A 1991 *J. Appl. Phys.* **70** 846

[29] Fonstad C G 1994 *Microelectronic Devices and Circuits* (Singapore: McGraw-Hill) pp 241–65

[30] Rhoderick E H and Williams R H 1988 *Metal–Semiconductor Contacts* (Oxford: Oxford Science Publications) pp 15–24

[31] Pierret R F 1990 *Dispositivos de Efecto Campo* (Reading, MA: Addison-Wesley) pp 87–116

[32] Rangel-Kuoppa V-T 2007 Electrical characterization of nitrogen containing III–V semiconductors *Doctoral Thesis* Helsinki University of Technology, Finland, available at http://lib.tkk.fi/Diss/2007/isbn9789512286386/isbn9789512286386.pdf

[33] Sze S M 1969 *Physics of Semiconductor Devices* (New York: Wiley-Interscience) pp 363–417

[34] Grove A S 1967 *Physics and Technology of Semiconductor Devices* (New York: Wiley-Interscience) pp 50–77

[35] Wang J B, Lu F, Zhang S K, Zhang B, Gong D W, Sun H H and Wang X 1996 *Phys. Rev.* B **54** 7979

[36] Chiquito A J, Pusep Y A, Mergulhão S, Galzerani J C and Moshegov N T 2000 *Phys. Rev.* B **61** 5499