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High Anodic-Voltage Focusing of Charge Carriers in Silicon Enables the Etching of Regularly-Arranged Submicrometer Pores at High Density and High Aspect-Ratio

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The anodic dissolution of silicon in acidic electrolytes is a well-known technology enabling the silicon machining to be accurately controlled down to the micrometer scale in low-doped *n*-type silicon electrodes. Attempts to scale down this technology to the submicrometer scale has shown to be challenging, though it premises to enable the fabrication of meso and nano structures/systems that would greatly impact the fields of biosensors and nanomedicine. In this work, we report on the electrochemical etching at high anodic voltages (up to 40 V) of two-dimensional regular arrays of millions pores per square centimeter (up to 30×10^6 cm^{-2}) with sub-micrometric diameter (down to ∼860 nm), high depth (up to ∼40 μm), and high aspect-ratio (up to ∼45) using low-doped *n*-type silicon electrodes (resistivity 3–8 Ω cm). The use of high anodic voltages, which are over one order of magnitude higher than that commonly used in electrochemical etching of silicon, tremendously improves hole focusing at the pore tips during the etching and enables, in turn, the control of electrochemical etching of submicrometer-sized pores when spatial period reduces below 2 μm. A theoretical model allows experimental results to be interpreted in terms of an electric-field-enhanced focusing of holes at the tip apex of the pores at high anodic voltages, with respect to the pore base, which leads to a smaller curvature radius of the tip apex and enables, in turn, the etching of pore tips to be preferentially sustained over time and space.

Keywords: nanostructuring, anodization, porous silicon, submicrometer pores, carrier focusing, high voltage

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INTRODUCTION

From first discovery to modern days, the possibility of controlling the electrochemical preparation of pores in silicon at nano to micro scales in terms of both size and pattern has fascinated scientists for more than 50 years (Uhlir, 1956).

In 1990, Lehmann and Föll reported for the first time on how to control the anodic dissolution of *n*-type silicon electrodes in low concentration HF-based aqueous electrolytes by back-side illumination, so enabling the etching of regular two-dimensional lattices of pores at the micrometer scale (Lehmann and Föll, 1990). Once a lattice of pits is pre-defined on the silicon surface, size, position, and morphology of pores etched by back-side illumination electrochemical etching

(BIEE) on low-doped (i.e., a few Ω cm) *n*-type silicon electrodes was shown to be finely controlled by tuning the etching parameters, such as for instance, doping concentration of silicon, electrolyte composition and temperature, anodic voltage, and current density (Lehmann, 1993; Föll et al., 2002; Matthias et al., 2005; Barillaro and Strambini, 2010). A decade later, Barillaro et al. reported on how to broaden BIEE of silicon to fabricate lattices of linear trenches (Barillaro et al., 2002b), so enabling the fabrication of a multitude of microstructures besides pores (Barillaro et al., 2002a, 2005). In 2012, Barillaro et al. further pushed the BIEE of silicon ahead, showing how to control anodic dissolution anisotropy/isotropy in real-time to enable the fabrication of free-standing microstructures (Polito et al., 2013) and complex microsystems (Bassu et al., 2012) at the micrometer scale. Nowadays, the BIEE of silicon has evolved into a highly versatile microstructuring technology, namely electrochemical micromachining (ECM), with unique features, among which there are high aspect-ratio of etched structures (>100), low roughness of etched surfaces (<10 nm), high etching rate of high aspect-ratio structures (up to 10 μm min^{-1}) (Cozzi et al., 2017). As a matter of fact, applications of ECM encompass today a broad range of research fields, from microelectronics (Kemell et al., 2007) and photonics (Surdo et al., 2013), to (bio)sensing (Surdo et al., 2012, 2014) and (nano)medicine (Harding et al., 2016; Delalat et al., 2018).

In spite of the significant technological advancement that has been achieved over the last two decades, the controlled etching of pores with either very large (i.e., >20 μm) or very small (i.e., <1 μm) diameter/spacing has not been achieved yet with BIEE on low-doped *n*-type silicon (Barillaro, 2015). Specifically, maximum diameter and spacing of lattice of pores was shown to have an upper boundary value of about 10 and 20 μm, respectively; on the other hand, minimum size and spacing was reported to be restricted to about 1 and 2 μm, respectively. Both upper and lower boundary values can be ascribed to a poor focusing of photogenerated charge carriers at the pore tips, as both diameter and spacing of pores increase/decrease above/below these values. Moreover, using an anodization voltage value of about 1 V, it was shown that a minimum current density value exists, for a given spacing, setting the minimum diameter value above which the etching of pore lattice can be finely controlled, at least for low-doped *n*-type silicon electrodes (Barillaro and Strambini, 2010).

In this work, the controlled etching of regular arrays of pores with submicrometric diameter (<1 μm) was successfully addressed by back-side illumination electrochemical etching of silicon electrodes with low-resistivity (3–8 Ω cm), using high anodization voltage values (up to 40 V) to effectively focus charge carriers to the pore tips when the spacing of pores is below 2 μm. A theoretical model allowed experimental results to be interpreted in terms of an electric-field enhanced focusing of holes at the tip apex of the pores at high anodic voltages, with respect to the pore base, when pore spacing is smaller than the depletion region width in the silicon electrode. Although the use of high anodization voltages for the electrochemical etching of regular lattices of pores in silicon was already reported (Rönnebeck et al., 1999; Cozzi et al., 2015), this work represents the first report on the controlled etching of sub-micrometric pores with high-density and high aspect-ratio.

MATERIALS AND METHODS

Materials and Chemicals

CZ-grown *n*-type (100)-oriented silicon wafers with a resistivity of 3–8 Ω cm and covered with a 298-nm-thick silicon dioxide layer, either flat (i.e., without any pattern) or patterned with a two-dimensional (2D) lattice (1 × 1 cm^2) of square holes with side of 1 μm and spacing (s) of 1.8 μm (hole density ∼30 × 10^6 cm^{-2}), were provided by STMicroelectronics (Milan, Italy). Acetone 99 wt%, pentane 99 wt%, 2-propanol 99.8 wt%, and hydrofluoric acid (HF) 48 wt% were purchased from Sigma-Aldrich. Ethanol 99.8 wt% and potassium hydroxide (KOH), pure powder at 85%, were purchased from Fluka Analytical. Sodium lauryl sulfate (SLS) powder was purchased from Carlo Erba Reagents.

Electrochemical Characterization of *n*-Type Silicon Electrode in Aqueous HF-Based Electrolyte by Linear Sweep Voltammetry

A thorough electrochemical characterization (>3 replicates) of flat (i.e., not patterned) *n*-type silicon electrodes in contact with an aqueous HF-based electrolyte (5 vol% HF:95 vol% H_2O, with 1,000 ppm of Sodium Lauryl Sulfate—SLS—as wetting agent) was carried out by linear sweep voltammetry. Flat silicon electrodes were achieved by cutting the flat silicon wafers in slabs of 2 × 2 cm^2 and removing the silicon dioxide layer using a solution of HF:ethanol (1:1 by vol.) for 60 s at room temperature. Flat silicon electrodes were loaded in a three-electrodes electrochemical cell containing the HF-based electrolyte (details are provided in the **Supplementary Material**), and the current flowing through the etch-cell was monitored upon application of voltages varying from 2 to −1.5 V with a sweep rate of −0.1 V s^{-1}, under back-side illumination (halogen lamp, 250W) of silicon. Experimental current density-voltage (J-V) curves (**Figure S1, Supplementary Material**) highlight the presence of an electropolishing current density peak J_{peak} = 78 ± 3 mA cm^{-2}, occurring at a voltage V_{peak} = 1.2 V, in good agreement with the literature (Lehmann and Föll, 1990; Barillaro and Strambini, 2010).

Potentiostatic Etching of Regular Arrays of Pores at High Anodic Voltage in Aqueous HF-Based Electrolyte

Pre-patterned *n*-type silicon electrodes were achieved starting from square silicon slabs (2 × 2 cm^2) cut from the patterned silicon wafers. The pattern was transferred onto the silicon surface by KOH etching, which yielded an array of inverted pyramid-shaped pits. The KOH etching was performed at 50°C for 750 s with a 20 wt% solution of KOH in deionized water, using the patterned silicon dioxide as a masking material. 2-Propanol was added to the KOH solution to increase wetting capability and to improve, in turn, etching uniformity. The silicon dioxide layer

was then dissolved using a solution of HF:ethanol (1:1 by vol.) for 60 s at room temperature.

The pre-patterned silicon electrodes were loaded in a three-electrodes electrochemical cell (details are provided in **Supplementary Material**) containing a HF-based electrolyte (5 vol% HF:95 vol% H_2O, with 1000 ppm of SLS as wetting agent), and etched for 2,000 s at different anodic voltage values, under back-side illumination of silicon.

The photogenerated etching current density (J_{etch}) was set to a given initial value J_{etch0} and linearly decreased over time to maintain the pore diameter constant with depth. Three different J_{etch0} values were tested, namely 13.4, 16.8, and 20.2 mA cm^{-2}, which were linearly reduced over time with a rate (α) of -0.938, -1.219, and -1.453 μA s^{-1}cm^{-2}, respectively, by decreasing the back-side illumination intensity through a reduction of the lamp power (Bassu et al., 2012). The different J_{etch0} values correspond to different expected porosity (i.e., dissolved silicon to total silicon volumetric ratio) values P_e:

$$P_e = \frac{J_{etch0}}{J_{peak}} \tag{1}$$

namely, 17.2, 21.5, and 25.8%, and, in turn, to different expected pore diameters d_e:

$$d_e = \sqrt{P_e \frac{4A_C}{\pi}} \tag{2}$$

namely, 0.842, 0.942, and 1.032 μm (**Table S1**, **Supplementary Material**), being $A_C = 1.8 \times 1.8$ μm^2 the unit cell area. For each J_{etch0} value, six different anodization voltage values (V_{etch}) were investigated, namely 1.2, 15, 20, 25, 35, and 40 V. The anodization voltage value is kept constant throughout the whole etching time. For $V_{etch} = 40$ V a further current density value $J_{etch0} = 10.07$ mA cm^{-2} ($P_e = 12.8\%$, $d_e = 0.644$ μm) was investigated, with J_{etch0} linearly reduced over time with $\alpha = -0.710$ μAs^{-1}cm^{-2}. Each experiment was replicated at least 3 times for each given J_{etch0}–V_{etch} pair.

After etching, pre-patterned silicon slabs underwent an overnight static bath in a HF:ethanol (1:4 by vol.) solution to fully remove SLS. A static rinse in ethanol and pentane, respectively, for 300 s followed by drying at 100°C on a hot plate was eventually performed.

All the etched slabs were then diced to allow morphological investigation of the longitudinal cross-section of the pores in the array to be carried out.

Morphological Characterization of Regular Arrays of Pores by SEM Microscopy

The morphological characterization of regular arrays of pores resulting from the electrochemical etching of pre-patterned silicon electrodes, at different anodic voltages and current densities, was performed by scanning electron microscope (SEM) using a JEOL JSM-6390. Top-view and cross-section images at different magnifications were acquired at an acceleration voltage of 3 kV. Five different cross-section images were acquired per each slab at both 2,000 × and 5,000 × magnifications, from which pore depth and diameter were experimentally measured. The cross-section images were exploited to perform a statistical analysis using a home-made software routine implemented using Matlab (Mathworks, Inc.), so as to obtain average value and standard deviation of both depth (h_m) and diameter (d_m) of the etched pores.

Experimental porosity P_m values were obtained from h_m and d_m values through the use of Equation (3), as the ratio between pore cross-sectional area (i.e., A_{CS}) and the unit cell area A_C, assuming all pores featuring circular cross-section and constant diameter over depth:

$$P_m = \frac{A_{CS}}{A_C} = \frac{\pi \left(\frac{d_m}{2}\right)^2}{A_C} \tag{3}$$

Experimental data on pore geometrical features (i.e., h_m, d_m) were also used to analytically evaluate the total silicon volume dissolved during each etching experiment (M_m). In particular, experimental M_m values were evaluated through the use of Equation (4), as the number of pores involved during the etching ρ_P (i.e., ratio between the etching area E_A of ~0.64 cm^2 and the unit cell area A_C) times the average pore volume (M_P):

$$M_m = \rho_P M_P = \frac{E_A}{A_C} \pi \left(\frac{d_m}{2}\right)^2 h_m \tag{4}$$

The experimental values obtained for the main pore parameters, i.e., diameter (d_m), depth (h_m), porosity (P_m), and volume (M_m), resulting from the above described morphological analysis of the SEM images, were compared with the expected values, i.e., d_e, h_e, P_e, and M_e, respectively, obtained from the etching parameters, i.e., etching time (t_{etch}) and etching current density (J_{etch}), on the basis of the model proposed by Barillaro and Pieri (2005). In particular, expected diameter (d_e) and porosity (P_e) were already reported in section Potentiostatic Etching of Regular Arrays of Pores at High Anodic Voltage in Aqueous HF-Based Electrolyte (Equations 1, 2). The expected silicon volume M_e dissolved for any J_{etch0} value was evaluated through the use of Equation (5), as the ratio of the total charge Q supplied during the whole etching experiment ($Q = E_A \int_0^{t_{etch}} J_{etch} dt$) and the product of silicon dissolution valence $n_v = 2.66$ (i.e., number of charges needed to dissolve a single silicon atom) (Barillaro and Pieri, 2005), elementary charge e (i.e., $e = 1.602 \times 10^{-19}$ C), and atomic density of silicon N_{Si} (i.e., $N_{Si} = 5 \times 10^{22}$ cm^{-3}):

$$M_e = \frac{Q}{n_v e N_{Si}} = \frac{E_A \int_0^{t_{etch}} J_{etch} dt}{n_v e N_{Si}} \tag{5}$$

Eventually, the expected pore depth (h_e) was evaluated using M_e and d_e values according to Equation (6):

$$h_e = \frac{M_e}{P_e E_A} \tag{6}$$

RESULTS AND DISCUSSION

High Anodic-Voltage Controlled Etching of Regular Arrays of High-Density High-Aspect-Ratio Pores in *n*-Type Silicon With Diameter Down to the Sub-micrometric Scale

Figure 1a (left side) shows a typical top-view SEM image of an array of pores prepared by anodic etching under back-side illumination at $V_{etch} = 1.2$ V and $P_e = 17.2\%$ ($J_{etch0} = 13.4$ mA cm^{-2}) of low-doped *n*-type silicon pre-patterned with regular lattices of square holes with size of 1 μm and pitch of 1.8 μm. The etching results in randomly-organized pores with non-constant spacing and average diameter of about 2 μm, which are uncorrelated from the pre-patterned layout, as confirmed by SEM analysis of the cross-section of the pore array (**Figure S2a**). Increasing the expected porosity value to 21.5 and 25.8% (etching current density value J_{etch0} to 16.8 and 20.2 mA cm^{-2}, respectively), while keeping the V_{etch} value unchanged (1.2 V), does not significantly improve the etching outcome (**Figures S2b,c**). This agrees with the state-of-the-art literature on the BIEE of pores in low-doped silicon at low anodic voltage (Barillaro and Strambini, 2010), according to which both minimum diameter and spacing exist for the controlled dissolution of silicon in acidic electrolytes, which depend on silicon resistivity, below which the anodic etching of regular patterns of square holes cannot be controlled to achieve a regular array of pores. For instance, for *n*-type silicon electrodes with resistivity of a few Ω cm, typically used in microelectronics, minimum values for diameter and spacing of pores above which the anodic etching can be fully controlled are about 1 and 2 μm, respectively. Below these boundary values, competition for collection of holes, photogenerated on the silicon back-side, at the tips of adjacent pores is very high. In fact, after an initial nucleation phase, during which silicon dissolution proceeds with the formation of pits in correspondence of defect sites pre-patterned at the silicon surface, photogenerated hole collection is no longer uniform over time and space, so that some pits collect more holes than others within the array. The former keep growing and increase their diameter to reach a roughly constant steady-state value over depth; the latter stop growing after a given depth, which depends on the growth of neighbor pores (**Figures S2a–c**).

Intense electric-field establishing across the depletion region at the pore tips (defects, in the nucleation phase) is known to induce an effective hole-focusing at low V_{etch} values when diameter and spacing of pores (defects) is >2 μm. We argue that severe overlap of space charge regions of adjacent pores occurring when the pore spacing reduces below 2 μm leads to a defocusing of electric-field lines at the pore tips, which affects the collection of photogenerated holes and enhances surface non-homogeneities, giving rise to a non-uniform sharing of photogenerated holes and, in turn, to an uncontrolled etching/growth of the pores.

Experiments at higher anodic voltage values V_{etch}, namely from 15 to 40 V, using the same current density values above reported for 1.2 V, were carried out to investigate the effect of an increasing electric-field on the focusing at the pore tips of holes photogenerated on the silicon back-side. Experimental results on the electrochemical etching of pores at increased anodic voltages are reported in **Figures 1b,c** and **Figures S2d–t.** Increasing the V_{etch} value turned out to have a beneficial effect on the controlled anodic etching of pre-patterned lattices of square holes with spacing < 2 μm. In fact, the number of dying pores significantly reduces as the etching voltage increases from 1.2 to 15 and 20 V, for any given etching current density value, and the correlation between etched/growing pores and surface pattern greatly improves (**Figures S2d–i**). Remarkably, for a given anodic voltage value, the number of dying pores reduces as the etching current density increases, then becomes zero at 20 V and 20.2 mA cm^{-2} ($P_e = 25.8\%$), so enabling the fabrication of a regular array of pores with uniform depth and diameter and without missing pores (**Figure S2i**). A further increase of the V_{etch} value to 25, 35, and 40 V (**Figures S2l–t**) highlights that, as the anodic voltage increases the etching of pores can be fully controlled also at smaller J_{etch0} values, namely 13.4 ($P_{theo} = 17.2\%$) and 16.8 mA cm^{-2} ($P_{theo} = 21.5\%$). Notice that, at V_{etch} of 35 and 40 V, arrays of regular pores with no missing pores were successfully prepared with a submicrometric dimater of about about 860 nm at $J_{etch0} = 13.4$ mA cm^{-2} (**Figures 1b,c**).

Effect of High Anodic-Voltage on Geometrical Features of Regular Arrays of High-Density High-Aspect-Ratio Pores Etched in *n*-Type Silicon

A thorough morphological investigation of regular arrays of pores (with no missing pores) etched at different high anodic voltages/current densities was carried out to infer into the effect of etching parameters on pore diameter, porosity, and depth. **Figure 1d** shows experimental values (average value and standard deviation, sd) of pore diameter (d_m, left axis) and array porosity (P_m, right axis) vs. pore depth (h_m), achieved at anodic voltages of 25, 35, and 40 V and current densities of 13.4, 16.8, and 20.2 mA cm^{-2}. Coefficient of variation %CV (by definition, the ratio between standard deviation and mean values) values average 3.4 and 0.7% for diameter/porosity and depth, respectively, highlighting that the etched pores are uniform over the whole array both in the in-plane and out-of-plane directions. For a given anodic voltage, an increase of both pore diameter d_m and array porosity P_m occurs as the etching current density J_{etch0} increases. Remarkably, once etching current density and etching time are given, both diameter/porosity and depth of the pores strongly depend on the anodic voltage value. For instance, at $J_{etch0} = 13.4$ mA cm^{-2} ($t_{etch} = 2{,}000$ s) the anodic etching of the pre-patterned square hole lattice gives rise to a regular array of sub-micrometric pores with diameter of 870 nm (sd = 35 nm) and depth of 39.5 μm (sd = 131 nm) at 40 V, and diameter of 863 nm (sd = 27 nm) and depth of 38.3 μm (sd = 335 nm) at 35 V, whereas pores etched at 25 V feature a diameter of 1.14 μm (sd = 50 nm) and depth of 36.7 μm (sd = 331 nm).

This differs from what expected for pores prepared in silicon through electrochemical etching at anodic voltage values close to the electropolishing voltage peak (i.e., a few Volts). In this case, once both etching current density and etching time are

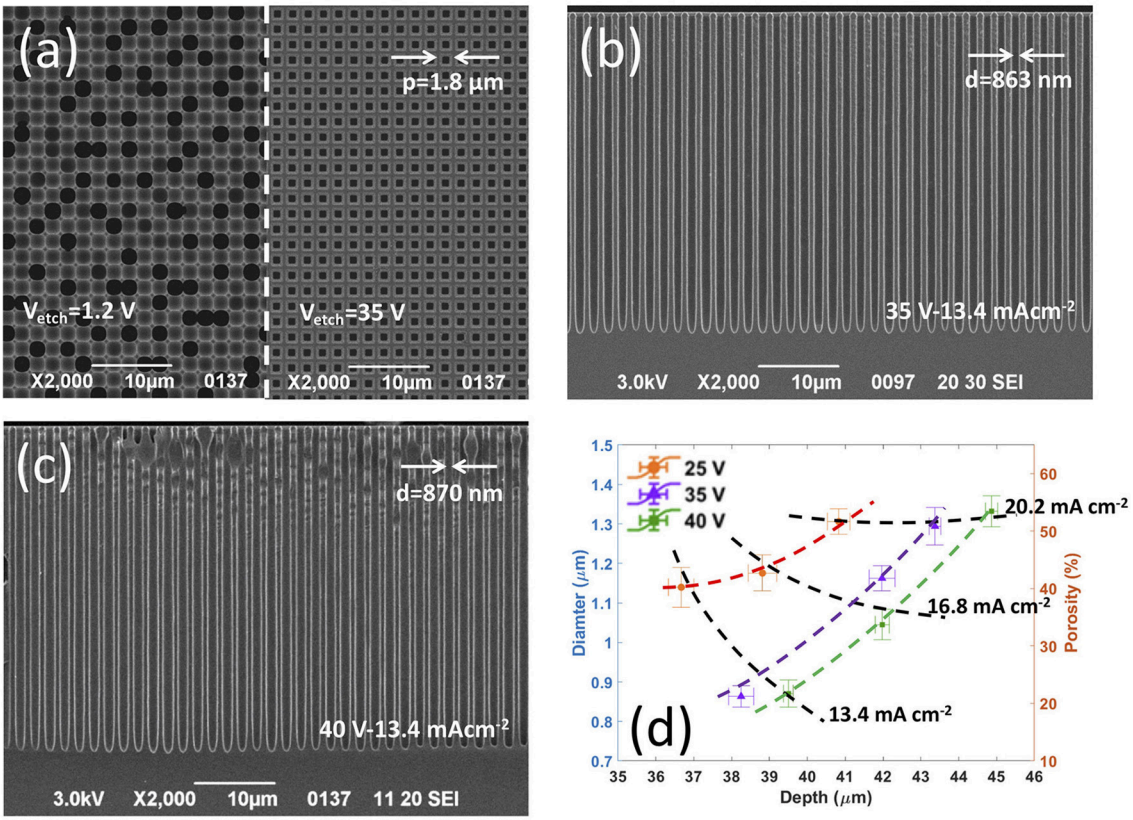

FIGURE 1 | Influence of etching voltage V_{etch} and etching current density J_{etch0} value on the controlled etching of pores with sub-micrometric diameter and spacing of 1.8 µm. **(a)** Top-view SEM images showing (left side) the uncontrolled etching resulting by performing the BIEE with $V_{etch} = 1.2$ V and $J_{etch0} = 13.4$ mAcm^{-2}, and (right side) a uniform array of sub-micrometric ordered pores featuring same diameter and depth, successfully achieved increasing the V_{etch} value to 35 V; **(b,c)** cross section SEM images showing uniform arrays of sub-micrometric ordered pores featuring same diameter and depth successfully obtained by BIEE performed with **(b)** $V_{etch} = 35$ V and $J_{etch0} = 13.4$ mAcm^{-2}, and **(c)** $V_{etch} = 40$ V and $J_{etch0} = 13.4$ mAcm^{-2}. **(d)** Morphological investigation of fully-uniform arrays of ordered pores etched at high anodic voltages, in terms of pore diameter, porosity, and depth: average values and standard deviations (error bars) of pore diameter (left axis) with corresponding experimental porosity (right axis) as a function of pore depth (average values and standard deviations) for each of the V_{etch} and J_{etch0} values investigated.

chosen, the electrochemical etching leads to pores with same diameter/porosity and depth, regardless of the anodic voltage value, if diameter and spacing of the etched pores are above 1 and 2 µm, respectively. **Figure S3a** shows expected values for diameter, porosity, and depth (calculated using Equations 1, 2, 6, respectively) of pores etched at current densities of 13.4, 16.8, and 20.2 mA cm^{-2}, regardless of the anodic voltage value. From the comparison between **Figure 1d** and **Figure S3a**, we can infer that, despite a properly controlled etching, a significant deviation of pore diameter and, in turn, array porosity from the expected values occurs at high anodic voltages for J_{etch0} values of 16.8 and 20.2 mA cm^{-2}, regardless of the V_{etch} value. On the contrary, the arrays etched at the lowest J_{etch0} value (i.e., 13.4 mA cm^{-2}) and highest V_{etch} values (i.e., 35 and 40 V) featured experimental diameter and porosity of about 870 nm and ∼20%, respectively, in good agreement with expected values (**Figure S3a**). Moreover, the comparison between **Figures 1d**, **S3a** also highlights a marked mismatch between measured and expected pore depths, thus pointing out that the growth rate depends on both J_{etch0} and V_{etch} values when the etching is performed at high anodic voltages.

Experimental results on pore depth, diameter, and porosity were further used to calculate the total amount of silicon dissolved (**Figure S3b**), for which a good agreement with expected values was obtained (dashed line in **Figure S3b**) when the electrochemical etching was performed at the highest J_{etch0} value (i.e., 20.2 mA cm^{-2}), regardless of the V_{etch} value. On the other hand, the mismatch between calculated and expected amount of silicon dissolved increased as the etching current density decreased, with a maximum mismatch obtained for fully uniform arrays of sub-micrometric pores etched at 13.4 mA cm^{-2} with 35 and 40 V. We argue that, such a mismatch can be ascribed to a variation of the silicon dissolution valence at high anodic voltages, when low etching current densities are employed.

Physics of High Anodic-Voltage Etching of High-Density Pores in *n*-Type Silicon Electrodes

The back-side illumination electrochemical etching of low-doped *n*-type silicon electrodes involves the flow of photogenerated holes through the depletion region establishing within the silicon

electrode, at the electrolyte/silicon interface. Therefore, a steady etching of pores within a silicon electrode pre-patterned with a regular lattice of defects requires that a steady flow of holes is established and sustained both in time and space through the space charge region at the pore tip. Both flow intensity and collection area of holes at the pore tip define, at a given etching time, the geometrical features of the resulting array of pores, namely diameter/porosity and length. Specifically, the flow intensity is mainly set by the electric-field establishing within the depletion region, while the collection area is mainly affected by the depletion region width establishing at the pore tip. Therefore, experimental results achieved on the electrochemical etching of high-density pores were tentatively interpreted in terms of the depletion region establishing at the pore tip at low and high anodic voltages.

The radius of curvature of the electrolyte/silicon interface is one of the key parameters affecting the depletion region developing within the silicon electrode, both in terms of width of the space charge region and intensity of the electric-field inside it. From SEM cross-sections of pores fabricated at low and high anodic voltages (**Figures S2a–t**), it is apparent that the pore tips become more elongated as the anodic voltage increases, so that the curvature radius at the apex of the pore tips is smaller at higher anodic voltage, with respect to that a low anodic voltage. This is sketched in **Figure 2a**, which shows as the curvature radius of the pore tip, and, in turn, of the electrolyte/silicon interface, increases monotonically moving from the tip apex, minimum value r_{min}, to the pore base, maximum value $r_{max} = d/2$, assuming for the pore a circular cross-section with a diameter d. A simplified theoretical model was implemented that takes variation of the curvature radius along the pore tip into account and allows the effect of anodic voltage on depletion region width and, in turn, electric-field intensity along the pore tip to be investigated. In the model, the tip surface is schematized with independent spherical surfaces/junctions with radius of curvature r_0 variable between r_{min} and the tip apex and r_{max} at the pore base (**Figure 2a**). One single pore/tip is analyzed, neglecting possible contributions of neighbor pores to depletion region and, in turn, electric-field at the pore tip. Also, the anodic voltage V_{etch} is assumed to fully drop across the space charge region formed in the silicon electrode, neglecting possible voltage drops across the space charge region established in the electrolyte and along the resistive paths between voltage source and electrolyte/silicon interface.

For a spherical electrolyte/silicon interface with curvature radius r_0 (**Figure 2b**), the following relations for electric-field $E(r)$ and electric potential $V(r)$ as a function of r_0 can be obtained by solving the Poisson equation in the silicon electrode (Muller and Kamins, 1977):

$$E(r) = \frac{qN_D}{3\varepsilon_s}\left[-r + \frac{(r_0 + w_d)^3}{r^2}\right] \quad (7)$$

$$V(r) = \frac{qN_D}{6\varepsilon_s}\left[r^2 + \frac{2(r_0 + w_d)^3}{r} - 3(r_0 + w_d)^2\right] \quad (8)$$

being r the distance from center of the spherical surface, ε the dielectric constant of silicon, N_D the ionized donor density, q the elementary electron charge, and w_d the width of the depletion region. **Figure 2b** shows a cross-section of a spherical electrolyte/silicon interface with curvature radius r_0, also highlighting the depletion region w_d established within the silicon electrode.

For a given voltage difference V_d applied between electrolyte and silicon, a relationship between depletion region width w_d and applied voltage V_d is obtained by assuming $V(r_0) = -V_d$ in Equation (8) (see **Supplementary Material**). This relationship was used to plot the depletion region width w_d in the silicon electrode as a function of the voltage V_d applied across the silicon/electrolyte interface and of the curvature radius r_0 of the silicon/electrolyte interface (**Figure 3a**). **Figure 3a** shows a contour plot of the depletion region width w_d in the silicon electrode, as a function of the anodic voltage V_d (between 0 and 50 V) applied across the silicon/electrolyte interface and of the curvature radius r_0 (between 100 and 1,000 nm) of the silicon/electrolyte interface. **Figure 3b** shows the relationship between depletion region width w_d and curvature radius r_0 for increasing values of V_d (corresponding to the dashed lines in **Figure 3a**).

By replacing w_d into Equation (7) with its expression derived above, a relationship between the maximum electric-field $E_{max} = E(r_0)$ establishing within the depletion region in the silicon electrode and the voltage V_d applied is obtained (see **Supplementary Material**). This was used to plot the maximum value of the electric-field $E_{max} = E(r_0)$ within the depletion region in the silicon electrode as a function of the anodic voltage V_d applied across the silicon/electrolyte interface and of the curvature radius r_0 of the silicon/electrolyte interface (**Figure 3c**). **Figure 3c** shows a contour plot of the maximum value of the electric-field $E_{max} = E(r_0)$ establishing within the depletion region in the silicon electrode, as a function of the anodic voltage V_d (between 0 and 50 V) applied across the silicon/electrolyte interface and of the curvature radius r_0 (between 100 and 1,000 nm) of the silicon/electrolyte interface. **Figure 3d** shows the relationship between maximum electric-field E_{max} and curvature radius r_0 for increasing values of the applied voltage V_d (corresponding to dashed lines in **Figure 3d**). As expected, an increase of both depletion region width w_d and electric-field intensity E_{max} at the pore tip occurs as the anodic voltage V_d is augmented, regardless of the curvature radius at the tip. However, the degree by which both depletion region width w_d and electric-field intensity E_{max} are augmented, depends on the curvature radius value. For instance, as the curvature radius at the tip reduces from 500 nm (i.e., pore base) to 100 nm (i.e., pore apex), the ratio between width of the depletion region at the pore base and tip apex increases from 3.1 to 3.4 (**Figure S4a**), and the ratio between maximum electric-field intensity at the tip apex and pore base increases from 27 to 42 (**Figure S4b**), as the anodic voltage is augmented from 2 to 40 V.

We argue that, for array of pores with spacing much larger than twice the depletion region, the pores of the array can be considered isolated from each other, so that low values (e.g., 2 V) of the anodic voltage V_{etch} are enough to sustain an effective hole focusing at the pore tip apex, where the curvature radius of the electrolyte/silicon interface is smaller than that at the pore base,

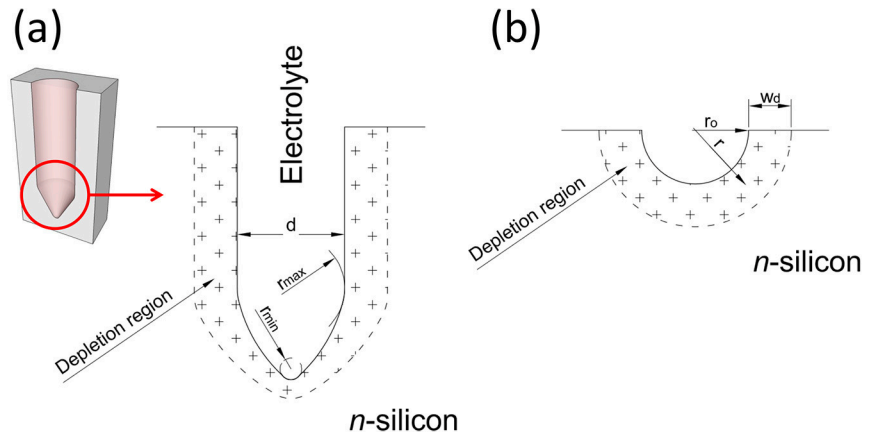

FIGURE 2 | Sketch of the electrolyte/silicon interface of a pore, with depletion region establishing into the silicon substrate highlighted. **(a)** Pore-shaped electrolyte/silicon interface; **(b)** hemispherical-shaped electrolyte-silicon interface. The radius of curvature of the electrolyte/silicon interface at the pore tip raises monotonically from the tip apex, minimum value r_{min}, to the pore radius, maximum value $r_{max} = d/2$, assuming for the pore a circular cross-section with a diameter d.

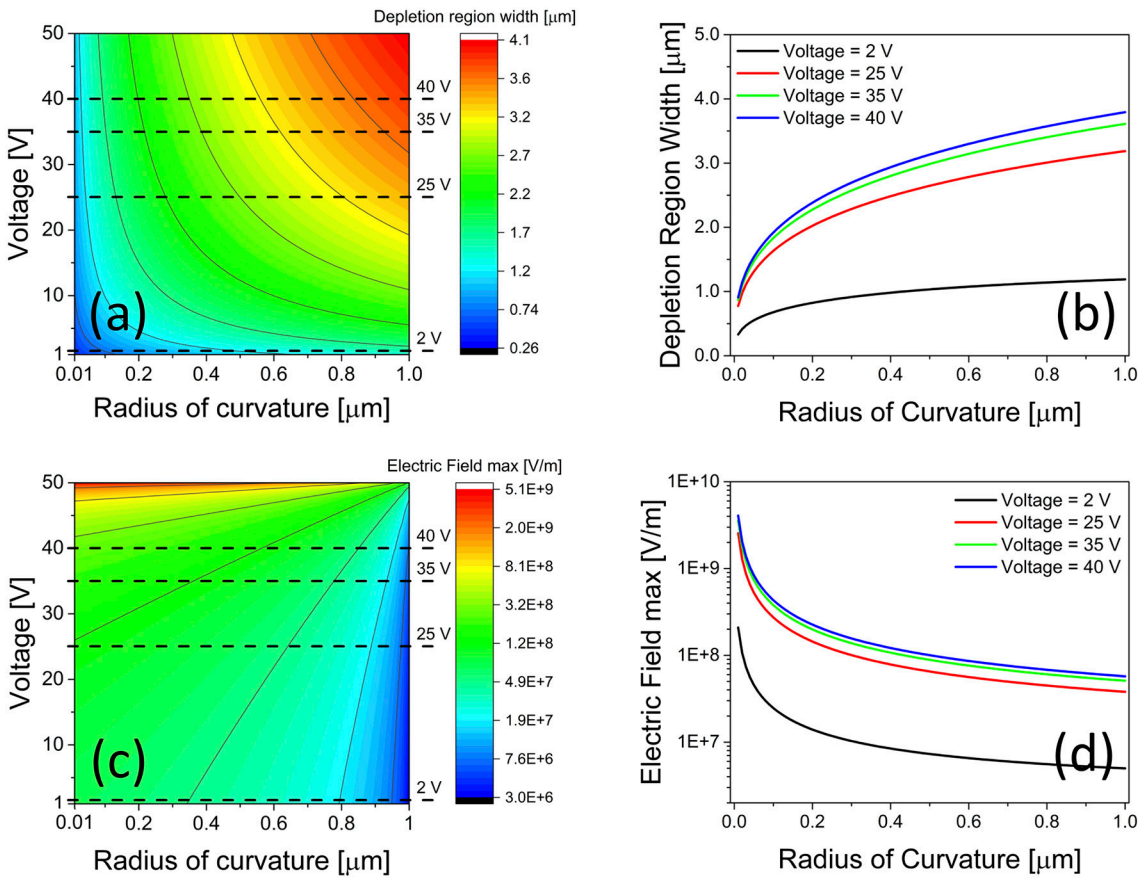

FIGURE 3 | Theoretical results on depletion region width and maximum electric-field intensity at the electrolyte/silicon interface of a pore, as a function of both anodic voltage and curvature radius values. **(a,c)** Contour plot of depletion region width w_d and maximum intensity of electric-field E_{max} in the silicon substrate as a function of electrolyte/silicon interface anodic voltage and curvature radius; **(b,d)** depletion region width w_d and maximum intensity of electric-field E_{max} in the silicon substrate as a function of electrolyte/silicon interface curvature radius, for different anodic voltage values, namely 2, 25, 35, and 40 V, corresponding to dashed lines in **(a,b)**.

thanks to the simultaneous lower value of w_d and higher value of E_{max} at the tip apex with respect to the pore base. This allows all pores of the arrays to develop and grow steadily. On the other hand, for array of pores with spacing of the same order of the depletion region or smaller (i.e., high-density array of pores), the pores in the array cannot be considered isolated anymore. In this case, the overlap of the depletion region between adjacent pores sensibly reduces the differences between curvature radius at the tip apex and pore base and, in turn, hole focusing efficiency at the tip apex. Tip apex and pore base now share photogenerated holes, thus producing morphologically-driven instabilities in the electrochemical etching of pores, for low anodic voltage values. Conversely, the use of high values (e.g., >20 V) for the anodic voltage V_{etch} allows the ratios between depletion region widths w_d at the tip apex and pore base (**Figure S4a**) and between maximum electric-field intensities E_{max} at the tip apex and pore base (**Figure S4b**) to be further enhanced with respect to those at low anodic voltage. This enables an efficient electric-field driven focusing of holes at the tip apex also for high-density array of pores with spacing smaller than the depletion region width, and, in turn, a stable pore growth/etching, in agreement with experimental results obtained at high anodic voltage in this work. Indeed, for a given etching current density value, whereas randomly-distributed pores were obtained from low-doped silicon substrates pre-patterned with a lattice of holes with spacing of 1.8 μm using a low anodic voltage (1.2 V), perfect arrays of pores were achieved at high anodic voltages (>20 V) using the same pre-patterned silicon substrates, thanks to the enhanced electric-field focusing of holes at the tip apex of the pores, with respect to the pore base, which allowed the etching of pore tips to be preferentially initiated and steadily sustained.

CONCLUSIONS

In conclusion, the controlled fabrication of high-density (∼30 × 10^6 cm^{-2}) regular arrays of pores featuring high-depth (up to ∼45 μm), high-aspect-ratio (from ∼35 to ∼45), and spacing of 1.8 μm was successfully achieved by back-side illumination electrochemical etching at high anodic voltage (from 20 to 40 V) of low-doped (resistivity 3–8 Ω cm) *n*-type silicon using low-HF-concentration etchants (5% by vol. in deionized water). Regular arrays of sub-micrometric pores featuring a diameter of 863 nm (sd = 27 nm) and 870 nm (sd = 35 nm), were successfully etched at 35 and 40 V, respectively, with J_{etch0} =13.4 mA cm^{-2}. A theoretical model was proposed, which allows experimental results to be interpreted in terms of an electric-field enhanced focusing of holes at the tip apex of the pores, with respect to the pore base, at high anodic voltages, which enables the etching of the pore tips to be preferentially initiated and steadily sustained over time and space.

The controlled anodic etching of submicrometer pores in low-doped *n*-type silicon envisages the possibility to scale the electrochemical micromachining (ECM) technology down to the mesoscale, through a better understanding of the silicon dissolution at high anodic biasing and by further optimization of the etching conditions, in terms of composition of the etching solution. This would open noteworthy applications in the fields of (though not limited to) nanomedicine, nanoelectromechanical systems (NEMS), and nanoelectronics.

AUTHOR CONTRIBUTIONS

CC and GP carried out the experiments. LS designed the theoretical model. GB conceived the idea and supervised the research. All authors analyzed and discussed the results and wrote the manuscript.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at: https://www.frontiersin.org/articles/10.3389/fchem.2018.00582/full#supplementary-material

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