APPLIED SCIENCES AND ENGINEERING

Sensing single domains and individual defects in scaled ferroelectrics

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Ultra-scaled ferroelectrics are desirable for high-density nonvolatile memories and neuromorphic computing; however, for advanced applications, single domain dynamics and defect behavior need to be understood at scaled geometries. Here, we demonstrate the integration of a ferroelectric gate stack on a heterostructure tunnel field-effect transistor (TFET) with subthermionic operation. On the basis of the ultrashort effective channel created by the band-to-band tunneling process, the localized potential variations induced by single domains and individual defects are sensed without physical gate-length scaling required for conventional transistors. We electrically measure abrupt threshold voltage shifts and quantify the appearance of new individual defects activated by the ferroelectric switching. Our results show that ferroelectric films can be integrated on heterostructure devices and indicate that the intrinsic electrostatic control within ferroelectric TFETs provides the opportunity for ultrasensitive scale-free detection of single domains and defects in ultra-scaled ferroelectrics. Our approach opens a previously unidentified path for investigating the ultimate scaling limits of ferroelectronics.

INTRODUCTION

On the basis of the reversible intrinsic polarization of the crystal lattice, ferroelectric materials have attracted enormous attention for nonvolatile memories (*1*–*3*), neuromorphic computing (*4*, *5*), and energy-efficient transistors (*6*, *7*). Regarding high-density cointegrated systems for future technology nodes, scalability plays an essential role among various ferroelectric materials, such as perovskites (*8*, *9*) and hafnium oxides (*10*, *11*). Much research has focused on the thickness scaling of ferroelectric films (*11*–*14*); however, from the perspective of high-density integration, especially for memory (*3*) and neuromorphic applications (*4*), area scaling is also crucial. The ultimately three-dimensionally scaled ferroelectric devices (*15*), including ferroelectric transistors, ferroelectric tunnel junctions, and ferroelectric random-access memories, will use only one domain, and, consequently, building a sensor for detection of ferroelectricity in a single nanoscale domain is required for understanding the fundamental limits and domain dynamics of ferroelectronics (*16*). Meanwhile, ferroelectric switching tends to generate new charge-trapping sites that influence the device performance (*17*, *18*). For a scaled ferroelectric device, the effect of an individual defect might be as strong as a single domain, and, thereby, it is critical to investigate the interplay of individual defects and ferroelectric switching at the ultra-scaled level.

The ferroelectric field-effect transistor (FeFET) is a device integrating a ferroelectric layer in the gate stack of a conventional metal oxide semiconductor field-effect transistor (MOSFET). The reversible remanent polarization of the ferroelectric is used for shifting the threshold voltage (V_T) of the transistor. By aggressively scaling the gate length (L_g) to about the size of a domain, FeFETs exhibit single domain–like switching with discrete V_T shifts (*1*, *19*, *20*). Scaled FETs were also demonstrated to detect individual defects in the gate oxide (*21*, *22*). However, when downscaling L_g in FeFETs to further explore the dimensional limit of ferroelectricity, the electrostatic control of the gate substantially degrades because of short-channel effects (*23*). Thus, despite the theoretical prediction of stable and robust remanent polarization existing even in unit-cell ferroelectrics (*15*), it is practically challenging to miniaturize L_g with maintained electrostatic control to investigate the material properties toward the ultimate scaling limits of ferroelectricity.

Using the quantum mechanical band-to-band tunneling (BTBT) in the staggered heterostructure of a tunnel field-effect transistor (TFET), we here instead demonstrate a fundamentally different method to sense the localized potential change induced by ferroelectric switching of single domains and charge trapping of individual defects in a nanoscale oxide without scaling the L_g. The BTBT does not depend on the physical L_g but on the highly confined electrostatic scaling length (λ) (fig. S1A), which determines the potential profile (band bending) across the tunnel junction (*24*, *25*). This means that the on-current (tunneling current) in the TFET is only sensitive to the local potential variation within λ rather than the rest of the channel. In this work, despite a physical L_g of 300 nm, we reduce λ to below 6 nm by appropriate geometry design, enabling the detection of single domain switching and individual defects in a 13-nm-thick ferroelectric gate oxide. The major advantage of this method is that λ automatically scales with the thickness of the ferroelectric film. That is, even smaller single domains down to sub–5 nm can be sensed by simply thinning the ferroelectric film, and by further structural modifications, single domains in ferroelectric films down toward subnanometer thickness can be sensed (fig. S1C). This unique property clearly differentiates from ultra-scaled FeFETs for single domain detection (*19*). Our TFET approach relies on the successful integration of vertical nanowire TFETs with a thin gate-all-around ferroelectric oxide, confirmed by the as-fabricated performance with a minimum subthreshold swing (SS) of 49 mV/dec (subthermionic) and the existence of negative differential resistance (NDR), in line with the state-of-the-art TFET (*26*). Benefiting from the high permittivity of ferroelectric gate-all-around stack, an effective oxide thickness reaches 1.4 nm, which is lower than most of

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the reported FeFETs (*27*). Many simulation investigations have shown performance improvement using the ferroelectric TFET (ferro-TFET) as a steep-slope device (*28*, *29*), nonvolatile memory (*30*), and a reconfigurable frequency multiplier (*31*) for low-power logic, storage, and high-frequency systems, respectively, but an experimental verification is lacking. Our ferro-TFET with SS < 60 mV/dec and a state-of-the-art memory window (MW) >2 V with ferroelectric switching therefore unlocks this promising device technology toward its potential applications.

RESULTS

TFETs for scale-free single domain sensing

To achieve high-performance TFET, heterostructures with staggered band alignment are typically used to prevent the tunneling in the off-state and simultaneously lower the tunneling barrier in the on state (*32*, *33*). Although many material systems, such as Si/SiGe (*34*), and two-dimensional materials (*35*) can be used for TFETs, III-V compound semiconductors enable high flexibility in the heterostructure design for TFETs. Moreover, a nanowire with gate-all-around geometry provides superior electrostatic control, thereby increasing the sensitivity toward potential variations in the channel. Hence, a nanowire ferro-TFET with an InAs/(In)GaAsSb/GaSb heterostructure is selected to be in line with state-of-the-art performance TFET structures (*33*, *36*). As shown in Fig. 1 (A and B), the 23-nm-thick nonintentionally doped (*nid*) InAs in the middle of the nanowire acts as the channel, while the n-type InAs and p-type (In)GaAsSb/GaSb are used for the drain and source, respectively. For the ferroelectric gate oxide, we chose 13-nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) mainly because of (i) its compatibility with Si complementary metal oxide semiconductor technology and easy synthesis via atomic-layer deposition (*37*); (ii) robust polarization at ~10-nm thickness (*38*, *39*); and (iii) this thickness being substantially thinner than the 300-nm L_g. The structural details of the HZO film on InAs such as crystallization verification and their interface quality have been shown in our previous work (*38*). Our TFET approach is not limited by the choice of ferroelectric material when comparing with other FeFET implementations. As shown in the band diagram of Fig. 1C, in the on state, the conduction energy band (E_C) of the channel is sufficiently lower than the Fermi level of the source ($E_{F,s}$) so that BTBT occurs across the InAs/(In)GaAsSb heterojunction (*25*). One of the imperative factors affecting the tunneling current is the transmission probability of BTBT at the heterojunction, which is mainly determined by the energy window between channel E_C and $E_{F,s}$. In the off state, the

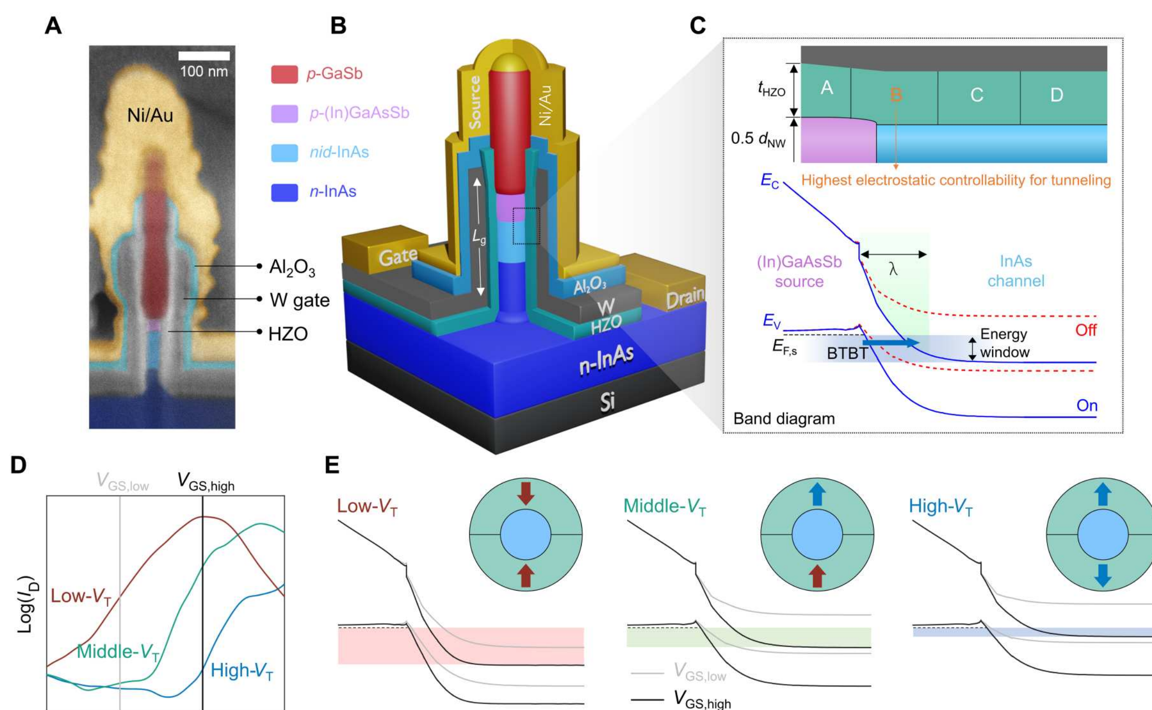

Fig. 1. Device structure of the vertical nanowire ferro-TFET and the mechanism of single domain detection. (**A**) False-colored SEM image of a single nanowire ferro-TFET in a vertical cross-sectional view. (**B**) The schematic of a nanowire ferro-TFET device with an InAs/(In)GaAsSb/GaSb structure. The color indication applies to both (A) and (B). (**C**) Zoom-in of the gate stack and the corresponding band diagram in the tunnel junction region. The black dashed line denotes the Fermi level at the source ($E_{F,s}$). E_C, conduction band; E_V, valence band; λ, the electrostatic scaling length, ~6 nm; d_{NW}, the channel diameter, 23 nm; t_{HZO}, the HZO thickness, 13 nm. Along the nanowire (the same as the tunneling direction), domain B (closest to the heterojunction) in HZO has the highest electrostatic controllability for tunneling. That is, the tunneling current of the ferro-TFET is only sensitive to the polarization of domain B rather than the other domains. (**D**) Presentative transfer characteristics of a ferro-TFET with three different polarization states: low-V_T, middle-V_T, and high-V_T. (**E**) Schematic band diagrams at two different gate voltages V_{GS} ($V_{GS,low}$ and $V_{GS,high}$) indicated in (D) and the polarization state of domains at the tunnel junction in a horizontal cross section for the low-V_T, middle-V_T, and high-V_T state, respectively. For a ferro-TFET with three states, we assume that there are two domains around the tunnel junction affecting the tunneling probability. The energy window at $V_{GS,high}$ in different cases is shown by the red, green, and blue rectangles, respectively.

energy window closes as the channel E_C is above $E_{F,s}$, and carriers cannot tunnel.

Generally, λ in a gate-all-around nanowire transistor is strongly influenced by the channel diameter (d_{NW}), the oxide thickness (t_{HZO}), and their corresponding permittivity (*40*, *41*). For our gate-all-around ferro-TFETs, λ is estimated as ~6 nm (*42*) (see text S1), which is considerably shorter than the diameter of a single grain (13 nm) in our HZO film (text S3). In a situation where several ferroelectric domains are positioned along the nanowire, the ferroelectric polarization state in the domain (domain B in Fig. 1C) closest to the (In)GaAsSb/InAs interface (overlapping with the λ region) will have the highest impact on the tunneling current. The polarization switching of rest domains around the channel, such as domains C and D, will only cause slight current variation due to the negligible resistance of the InAs channel as compared to that of the tunneling junction. In other words, V_T only significantly shifts in the ferro-TFET when domain B is switched and negligibly by other domains along the channel. Since the domains most likely are smaller than the width of the 23-nm channel (nanowire circumference), there could be multiple domains around the tunnel junction, leading to multiple V_T states. In the case as shown in Fig. 1D, three different V_T states are measured corresponding to two domains around the tunnel junction in addition to the respective band diagrams, as illustrated in Fig. 1E.

When keeping the same channel material and diameter, λ simultaneously scales with the thickness of the HZO gate oxide, leading to a minimum ferroelectric thickness for single domain detection below 5 nm using the current TFET structure (fig. S1C). This unique feature enables ferro-TFETs to sense a single domain in ultrathin ferroelectric films without aggressive L_g scaling using sophisticated lithography techniques. With further scaling of λ by thinning down the channel diameter, for instance, using atomic layer etching (*43*), we find that ferro-TFETs with a 5-nm-thick channel have the potential to probe single domains even in subnanometer-thick ferroelectric films according to the λ scaling modeling (fig. S1C) (*44*), which is of great importance for understanding the compatibility of ferroelectrics with future technology nodes.

Super-steep switching in DC characterization

We start the electrical characterization with the pristine transfer (Fig. 2B) and output characteristics (Fig. 2C) of a ferro-TFET (device A) based on the scheme marked in black in Fig. 2A. For TFETs, SS is not limited by the thermal Maxwell-Boltzmann tail of carriers, thus being able to reach below 60 mV/dec (*24*, *25*). Here, the transfer characteristics show a minimum SS of 49 mV/dec with negligible hysteresis (Fig. 2B and fig. S5A). Notably, the drain current (I_D) slightly reduces at high gate voltages (V_{GS}) in the transfer curve, which can be understood as the source depletion (*26*) due to gate overlapping with the source segment in the device structure (Fig. 1A). This phenomenon is also observed in other reported heterostructure TFETs (*26*, *45*). The output characteristic in Fig. 2C shows a trend of I_D saturation with increasing the drain-source voltage (V_{DS}), and the inset shows a manifest NDR with a peak-to-valley current ratio of ~1.5 at the reverse V_{DS} bias, confirming the presence of a high-quality tunnel junction within the transistor. The overall pristine performance verifies the integration feasibility of ferroelectrics onto gate-all-around TFETs.

Next, we examine the reconfigurability (V_T regulation) of the ferro-TFET (device A) by applying a voltage pulse (V_{pulse}) at the gate (the red scheme in Fig. 2A) before the transfer characterization (DC *I-V* sweep). As shown in Fig. 2D, two separated transfer characteristics (low-V_T and high-V_T states) can be set by pulsing the gate at +4 /−4 V for 250 ns, respectively. Compared with the pristine case (Fig. 2B), a degradation of average SS and higher off current in both states are observed after ferroelectric switching in Fig. 2D, which is attributed to more charge trapping being involved. An increased on current after ferroelectric switching is achieved, which is similar to the literature (*46*). By comparing two V_T states in Fig. 2D, a state-of-the-art MW of >2 V is obtained, close to the theoretical limit using this HZO thickness (*47*). The key metrics of our ferro-TFETs, including an endurance of >10^5 and a retention time >10 years (fig. S5, C and D), are summarized in text S4 and table S2. Moreover, an average MW reaches about 1.5 V with a device-to-device variation of the same sample as indicated in fig. S6. When backward sweeping (arrows in Fig. 2D) V_{GS} in the low-V_T state, two distinct steep steps, labeled ① and ②, appear with a very low SS of 38 and 4.6 mV/dec (Fig. 2, E and F), respectively, which is interpreted as the polarization switching of a single domain (*48*). Notably, the first step in the low-V_T state leads to a reduced MW of 1.9 V (Fig. 2D), indicating one domain being switched. Because of the polycrystalline nature of the HZO film in addition to the variation in grain orientation, the domain position with respect to the tunneling interface and the coupling effect from neighboring domains along the channel, the coercive voltage can differ among single domains around the heterojunction. Therefore, more than one steep step due to ferroelectric switching may be observed. Since the ferroelectric switching occurs faster than DC sweeping rate, an abrupt transition from one current level to another is expected. To evaluate this, we reduce the V_{GS} sweep steps gradually down to 1 mV in the DC measurement and obtain the lowest SS due to switching of 2.1 mV/dec, as shown in Fig. 2G (transfer characteristics in fig. S5B). This super-steep switching is commonly observed in other devices (Fig. 2, H and I, device B; fig. S5E, device F; and fig. S6) with the switching voltage ranging from −2.5 to −1.5 V in the low-V_T state (fig. S6).

To reveal the evolution of single domain switching, we design a set of measurements with backward sweeping of V_{GS} on the representative device B with two super-steep steps. First, we set the device to the low-V_T state by sending a +V_{pulse} (+4 V/250 ns). We measure the transfer characteristics and stop sweeping when the first steep switching appears (first sweep in Fig. 2H). Then, we repeat using an identical sweep directly after the first sweep and find a positive V_T shift (second sweep in Fig. 2H). To confirm that this positive V_T shift results from the ferroelectric switching of a single domain instead of traps, a third sweep is executed, and its transfer characteristic almost overlaps with the second sweep (Fig. 2H). Another validation to approve this method is the hysteresis measurements (fig. S7), which can separate the ferroelectric switching from traps (*49*). Next, we redo the measurement but instead stop the first sweep when the second steep switching occurs (Fig. 2I). As expected, a wider V_T shift is observed (Fig. 2I) between two transfer curves, indicating that two domains are switched. Last, we read the transfer characteristic of the high-V_T state after a −V_{pulse} (−4 V/250 ns). This is necessary to confirm whether there are other domains existing around the heterojunction. If the V_T in the high-V_T state overlaps with the V_T in the second sweep in Fig. 2I (light blue curve), there are only two single domains; otherwise, other single domains should be involved. Thus, four different transfer characteristics plotted together in Fig. 2J suggest four accessible states with three

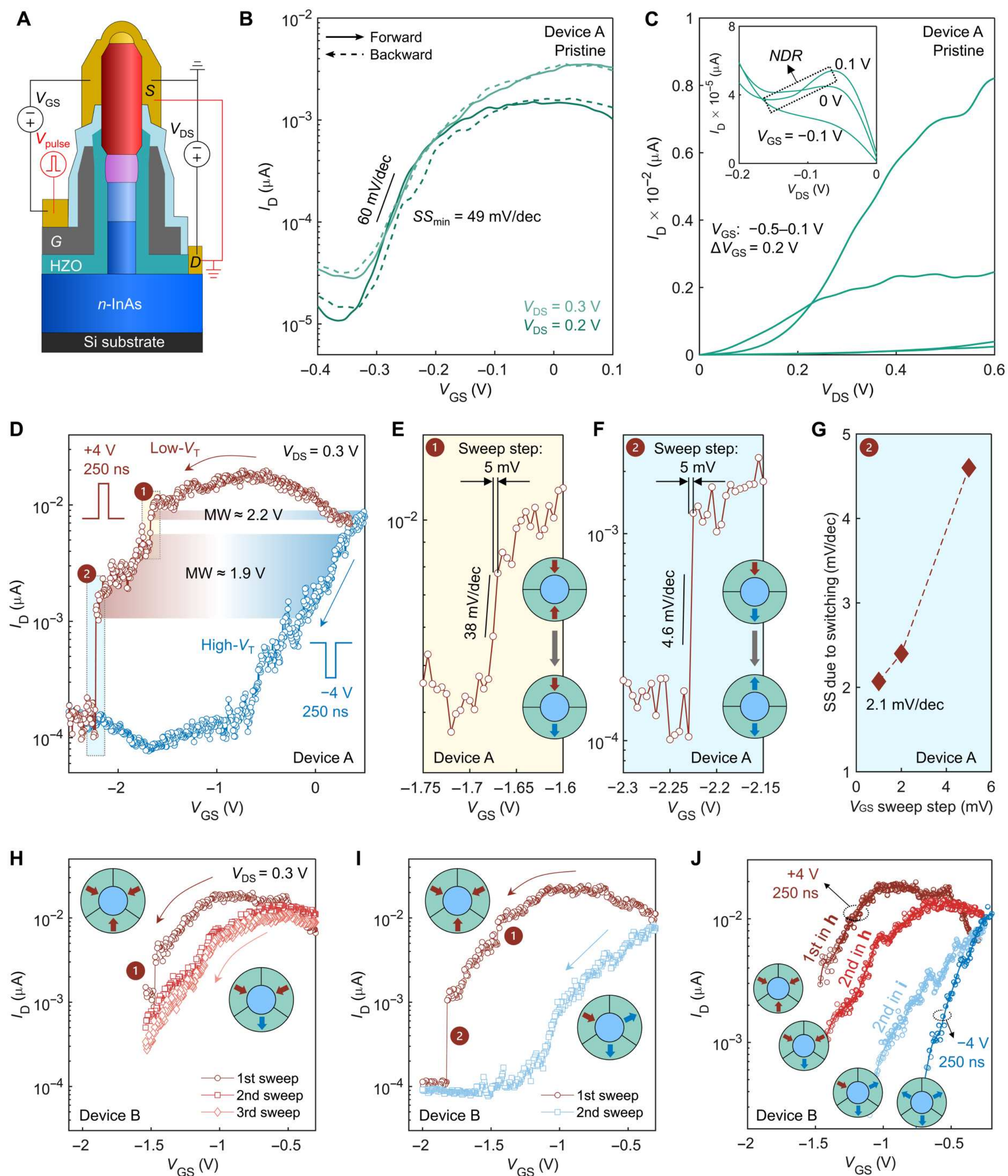

Fig. 2. DC characterizations of ferro-TFETs. (**A**) The electrical measurement scheme for the ferro-TFETs. Connections and components marked in red show the voltage pulse (V_{pulse}) for ferroelectric polarization, while the scheme of DC *I-V* characterization is illustrated in black. S, G, and D denote source, gate, and drain, respectively. The color indication of the device is identical to that in Fig. 1B. (**B**) Pristine transfer characteristic of a sub–60 mV/dec ferro-TFET device. "Forward" and "Backward" denote V_{GS} sweep direction indicated by the corresponding arrows. (**C**) Pristine output characteristics of the same device. The inset shows NDR at reverse V_{DS} bias. (**D**) Reconfigurable ferro-TFET with the low-V_T (red) and high-V_T (blue) states controlled by pulsing the gate at ±4 V for 250 ns, respectively. The arrows indicate the sweep direction. An MW is defined by the voltage difference between two states at the same current level. The steep slope results from the single domain switch as marked in ① and ②. (**E** and **F**) Magnified figures of the steep-slope region ① (E) and ② (F). (**G**) Subthreshold swing (SS) due to ferroelectric switching of the steep step ② as a function of V_{GS} sweep steps. (**H**) One-domain switching reveal. First, pulsing the gate with +4 V/250 ns; sweeping V_{GS} until the super-steep switching ① appears (first sweep); repeating sweeping V_{GS} directly after the previous sweep without pulsing the gate (second and third sweep). (**I**) Two-domain switching reveal. First, pulsing the gate with +4 V/250 ns; sweeping V_{GS} until the super-steep switching ① and ② appear (first sweep); sweeping V_{GS} directly after first sweep without pulsing the gate (second sweep). (**J**) All four discrete states (dashed circles indicate the *I-V* measured after the gate pulse correspondingly) can be detected, suggesting three domains around the tunnel junction in the ferro-TFET, as the insets show in (H), (I), and (J).

domains around the tunnel junction (insets of Fig. 2, H to J). The reason that no third steep step is observed in the DC sweeps is that the device reaches the off state before it reaches the required V_{GS} to switch the polarization. It is also noticeable that the data in Fig. 2 (D and H to J) exhibit some noise, which can be understood as a result of the quick DC sweep used to mitigate the defect response during the measurements. Nevertheless, our findings related to single domain switching is unambiguous.

Single domain switching in pulsed *I-V* measurements

To validate that all four states relate to three domains in device B, we implement a conventional pulse scheme by gradually increasing the amplitude of V_{pulse}, while a pulsed *I-V* measurement, typically used for FeFETs (*19*, *48*), is used to measure I_D-V_{GS} for each V_{pulse}. The transfer characteristic of pulsed *I-V* is identical to the DC *I-V* in the on state, whereas the off state is overestimated because of the noise floor of the pulsed measurement setup (fig. S8A). Therefore, it is reasonable to here define V_T as V_{GS} at I_D = 5 nA (Fig. 3A), which is in the on-state region.

When gradually increasing V_{pulse} (t_{pulse} = 1 μs), three abrupt V_T transitions in the transfer characteristics are found in Fig. 3A, corresponding to four distinct V_T states in Fig. 3B. The transfer curve in any state resembles each other well except for a V_T shift, which is seemingly a different behavior compared to ultra-scaled planar FeFET (*19*). By instead varying $-V_{pulse}$, almost identical V_T states are observed (Fig. 3C), overlapping well with positive pulse schemes (Fig. 3D). This result confirms the presence of three single domains around the tunnel junction, in agreement with the result of DC measurement. The discrete V_T shift with gradually tuning V_{pulse} differs from the analog switching behavior in InAs nanowire FeFETs with similar dimensions (*50*) and long-channel Si FeFETs (*51*), verifying that our ferro-TFET behaves as an ultra-scaled FeFET with single domain–like V_T shifts (*20*). Notably, V_T shifts slightly toward the opposite direction after state transition at high $-V_{pulse}$ (Fig. 3C), which is probably caused by hole trapping

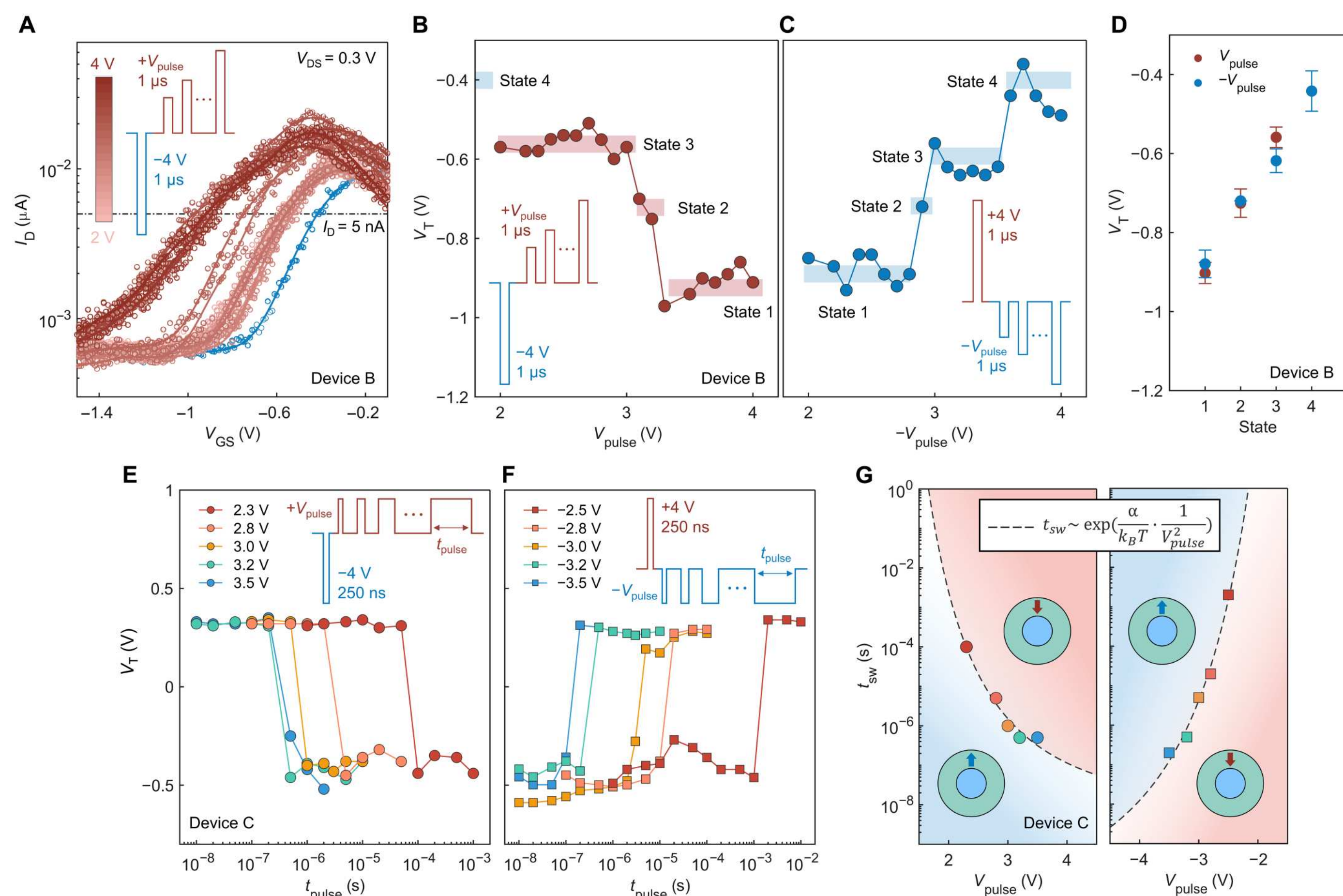

Fig. 3. Pulsed *I-V* measurements of ferro-TFETs. (**A**) Pulsed I_D-V_{GS} curves of device B measured after each pulse shown in the inset. The color bar indicates the value of V_{pulse}. (**B**) V_T (defined as V_{GS} at I_D = 5 nA) for all curves in (A) are extracted as a function of V_{pulse}. (**C**) V_T obtained by varying $-V_{pulse}$ with the pulsing scheme in the inset. Multiple states (red and blue rectangles guide the eye for different states) with digital transition in (B) and (C) are observed. (**D**) Extracted average V_T from each state in (B) and (C). The error bar shows the SD of the data points in the same state. (**E** and **F**) V_T extracted from pulsed I_D-V_{GS} measurements with varying t_{pulse} in the pulse scheme (inset) for a ferro-TFET with only a single major domain affecting the tunneling. Two stable states can be found at various V_{pulse}. Thus, this device is ideal to investigate the switching dynamics of the single domain. (**G**) Required switching time t_{sw} extracted from (E) and (F) as a function of V_{pulse}, fitting well with the nucleation-dominated switching model (inset), which separates two polarized states indicated by different colors. In the expression, α, k_B, and T denote the exponential coefficient associated with the material properties, Boltzmann constant, and temperature, respectively.

(*52*). In addition, the entire MW is compressed compared to the DC measurements in Fig. 2, which we attribute to endurance degradation during the DC measurements (fig. S8B).

Subsequently, we explore the ferroelectric switching dynamics in our ferro-TFETs. Because of the polycrystal HZO film in the ferro-TFETs, the number of ferroelectric domains in different devices can vary. For simplicity, a device (device C) with only one domain switching is investigated. By progressively varying t_{pulse}, a binary V_T shift takes place at a certain pulse width, as shown in Fig. 3 (E and F). Repeating the same procedure at various V_{pulse}, the minimum required switching time (t_{sw}) at each V_{pulse} is achieved in Fig. 3G. Because of the small grain size existing in our HZO film, the domain wall migration is limited (*37*). Therefore, the ferroelectric polarization reversal is considered as a nucleation-dominated process described in (*19*), with a nucleation-limited switching model (*53*, *54*) typically used for polycrystalline fluorite–structured ferroelectrics (*37*). In this case, an exponential dependence between t_{sw} and $1/V^2_{pulse}$ is expected as the inset indicates, differing from the simple power-law relationship described in the Kolmogorov-Avrami-Ishibashi model typically used for bulk and epitaxial ferroelectric films (*55*). Although t_{sw} may vary every repeating time at a certain V_{pulse}, as reported previously (*19*), the trend of the t_{sw}-V_{pulse} relationship will not change, thus defining the operational regime to achieve the desired polarization state (Fig. 3G, inset).

Individual defect detection in the ferroelectric gate oxide

Last, we examine the detectability of individual defects in the gate oxide. A typical impact of individual oxide defects on the transfer characteristic is I_D fluctuation when sweeping V_{GS}, which was observed in ultra-scaled MOSFETs (*21*) and TFETs (*33*, *56*). This phenomenon is visible in our ferro-TFETs both before (green) and after (blue) ferroelectric switching (Fig. 4A). To clearly demonstrate the effect from the individual defects, the most notable current peaks with the largest current fluctuation are studied in both cases. If a localized individual defect is positively charged in the off state, the charged defect can capture an electron when increasing the gate bias (forward sweeping) to a certain value. Consequently, I_D drops sharply when the charge is neutralized, provoking a peak in the transfer characteristic due to a V_T shift (~19 mV of peak A; Fig. 4A).

This current fluctuation due to individual defects in the gate oxide can be measured by random telegraph signal (RTS) noise (see Materials and Methods). We assume an acceptor-like defect located within the oxide, which causes the current reduction with the capture of an electron while increasing the current with the emission of an electron. In the pristine characteristic, a two–current level RTS noise at fixed bias is observed (Fig. 4B). The time constants for the capture (τ_c; fig. S9B) and emission (τ_e; Fig. 4C) of an electron are determined by fitting an exponential distribution of capture/emission time (t_c/t_e indicated in Fig. 4B). A series of time constants are obtained as a function of V_{GS} (Fig. 4F) by implementing an identical measurement at different V_{GS} near peak A. When the channel E_F probes the defect trap 1, $\tau_c = \tau_e$, that is, an electron has equal probability to enter or leave trap 1 by the tunneling process (Fig. 4G).

However, a three–current level RTS noise is observed after ferroelectric switching (Fig. 4D), indicating two traps. Within the selected RTS measurement duration, the two higher current levels (trap 2) have more transitions and counts (fig. S9C), and, thus, we mainly analyze trap 2 and determine its τ_c (fig. S9D) and τ_e (Fig. 4E). A set of τ_c and τ_e are also obtained for V_{GS} near peak B (Fig. 4H), and E_F aligns with trap 2 (Fig. 4I) at equilibrium. Since the defect trap with a lower energy level is more likely to capture the electron (shorter t_c in Fig. 4D), we attribute peak B and peak C to trap 2 and trap 3, respectively (Fig. 4A). Since I_D fluctuations occur at similar current levels before and after the ferroelectric switching, it is highly likely that trap 1 is the same defect as either trap 2 or trap 3.

Moreover, the depth of the defect (z) from the channel into the oxide can be estimated (see Materials and Methods) by the time constant at equilibrium (*57*). The almost identical time constant (0.55 versus 0.67 s) obtained before and after switching suggests that the probed individual defect is located in the gate oxide with the same depth, $z \approx 4$ nm, assuming elastic tunneling of electrons from the oxide to the channel (calculations in Materials and Methods). With simplified electrostatic modeling of a point charge at the same depth, the potential energy change of the channel owing to one defect can be estimated to ~3 meV, which is slightly smaller than the surface potential change (~8 meV) determined from ΔV_{GS} (peak width) in Fig. 4A (calculations in text S5). This underestimation may originate from several aspects, such as uncertainty of selected parameters, a very simple electrostatic model, and a very ideal trapping process using an elastic tunneling model without including activation energy (discussed in text S5). Although the model may be improved with the above considerations, the calculated result is still comparable to the experimental one within the same order of magnitude. Thus, the RTS noise with a corresponding ~19-mV V_T shift in the transfer curve originates from one individual defect trap in the oxide at $z \approx 4$ nm. It also fits well with the situation after ferroelectric switching where the summed ΔV_{GS} of peaks B and C is doubled (~40 mV in Fig. 4A) and also consistent with the three–current level RTS result (Fig. 4D). We also find in another device that more than one new defect due to ferroelectric switching is activated, although one original defect was present before any switching (fig. S10). Identical ΔV_{GS} is obtained at a similar current level in that device, and the ΔV_{GS} maintains an integer multiple of ~19 mV after ferroelectric switching (fig. S10). All the above confirm that our ferro-TFETs probe individual defects that are responsible for the small V_T shift by trapping/detrapping an electron. Combining with the capability of single domain detection in ferro-TFETs, one can use this device to quantify the number of traps in the gate oxide introduced by a single polarized domain.

DISCUSSION

We have reported the integration of TFETs with a thin ferroelectric HZO gate stack, achieving a pristine SS < 60 mV/dec and an MW >2 V induced by ferroelectric switching in the device. Because of the BTBT transport mechanism in the ferro-TFET, the effective channel length, λ, is scaled below 6 nm. Using this ultrashort effective channel length, we have demonstrated abrupt V_T shifts in both DC and pulsed *I-V* measurements in the ferro-TFET, verifying the detection of single domains in nanoscale ferroelectric HZO. We also probe the same individual defect before and after ferroelectric switching and find newly activated defects that have a similar energy level after ferroelectric switching by measuring their RTS noise. The scaling theory indicates that λ can be extremely scaled down toward the subnanometer level (fig. S1C) by current technologies (*14*, *43*)

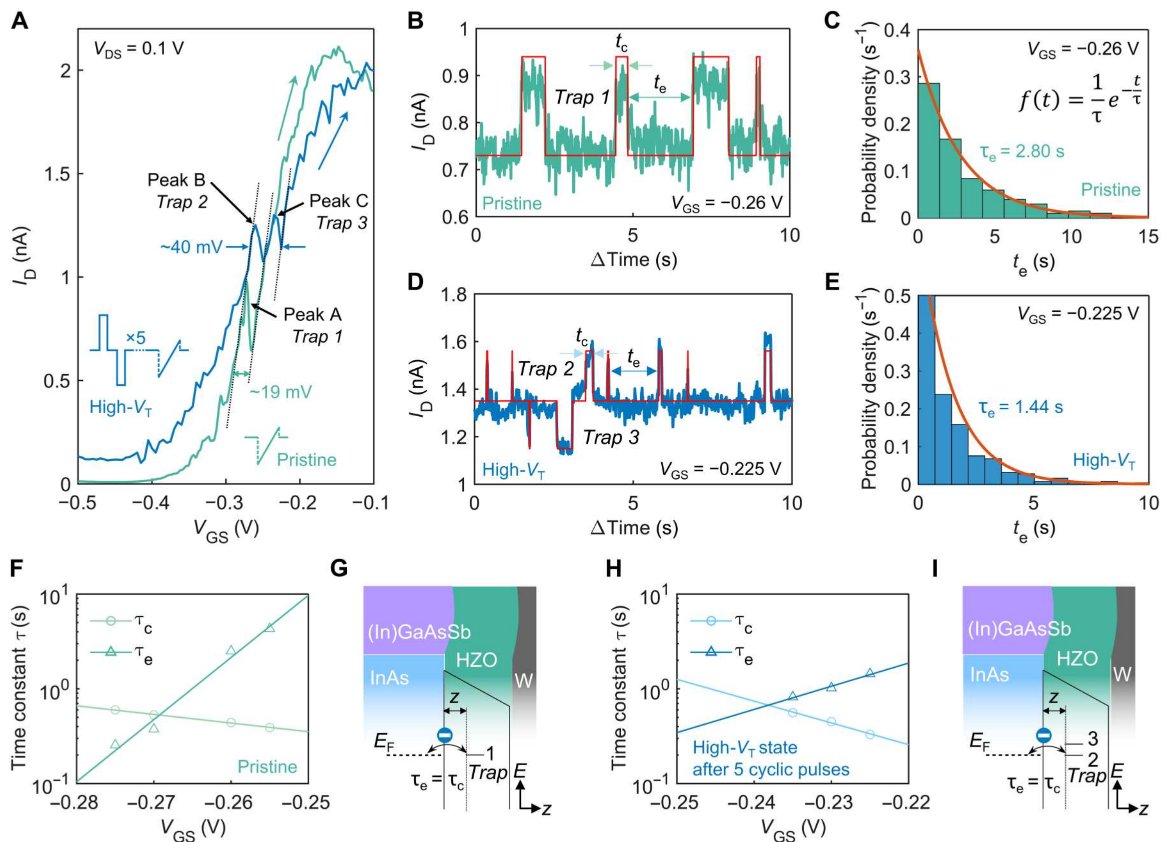

Fig. 4. Detection of individual defects in the HZO gate oxide. (**A**) Transfer characteristics of a ferro-TFET before and after ferroelectric switching. The arrows denote the forward sweeping direction. The corresponding measurement scheme is indicated with the same color in the inset. Green, pristine; blue, after five-cycle switching (±4 V/250 ns) in the high-V_T state. (**B**) Excerpt of an RTS measurement showing two current levels (green, measured data; red, abrupt transition steps obtained from the peak values of the current distribution; see fig. S9A). (**C**) Probability density distribution of t_e extracted from the entire RTS measurement at fixed bias. The exponential distributions $f(t)$ fitted to obtain the time constant τ are indicated by the red curves. (**D** and **E**) Excerpt of an RTS measurement (D) and corresponding probability density distribution of t_e (E) after ferroelectric switching in the high-V_T state, respectively. Three current levels in (D) correspond to three Gaussian fittings in the entire current distribution (fig. S9C). (**F**) Extracted capture (τ_c; see fig. S9B) and emission (τ_e) time constant at different V_{GS} before ferroelectric switching (pristine). (**G**) Illustration of band diagram in the situation that the channel E_F probes defect trap 1 in the oxide when $\tau_c = \tau_e$. E_F, the channel Fermi level; E_{FM}, the gate metal Fermi level; z, the depth of the individual defect in the oxide. (**H** and **I**) The case of the same device after ferroelectric switching. When $\tau_c = \tau_e$ (τ_c determined in fig. S9D), the channel Fermi level probes trap 2 (I), which we studied for the time constant (H). An extra defect (trap 3) with a higher energy level is also activated after ferroelectric switching, leading to three–current level RTS noise in (D), where trap 2 results in the higher two current levels, while trap 3 causes the lower two current levels.

while retaining a long physical channel without short-channel effects. Our ferro-TFET structure thus provides a simple approach for demanding investigations of ultra-scaled ferroelectric dynamics and the interplay with defects at the subnanoscale level, which will enable the fundamental material understanding necessary for future scaled ferroelectric devices. In addition, this ferro-TFET device may find more functionalities in low-power systems due to its subthermionic and reconfigurable operations.

MATERIALS AND METHODS

Device fabrication

The sample started with the nanowire growth. First, a short Sn-doped InAs was grown on a prepatterned Si substrate with a 260-nm highly doped InAs buffer layer by metal organic vapor–phase epitaxy via a Au-assisted vapor-liquid-solid process. Next, an *nid*-InAs was grown as the channel for the TFET. After that, a quaternary segment (In)GaAsSb with Zn incorporated as the dopant was grown for p-type source. The compositions of the (In)GaAsSb quaternary segment are identical to sample D in (*36*), which were confirmed by the energy-dispersive x-ray spectroscopy using transmission electron microscopy. During the (In)GaAsSb growth, In was not supplied but remained in the nanowire due to its high solubility in Au catalyst (*58*), thus being incorporated in the quaternary segment. The nanowire growth was finalized by a Zn-doped GaSb segment with a larger diameter, which increases the top contact area. The entire nanowire after growth is illustrated in fig. S2A.

Figure S2 shows the main process flow of ferro-TFETs. First, three cycles of digital etch (DE) were performed by repeating the ozone exposure and wet etching in citric acid to the sample, which improves the gate electrostatics by reducing the channel diameter and suppressing the oxide states at the channel interface (*59*, *60*). This DE etch process tends to be selective between InAs and GaSb, resulting in diameter reduction only in the InAs channel instead of the top GaSb (*61*). After the last cycle of DE, the

sample was immediately transferred into the atomic layer deposition chamber for HZO growth at 200°C. The HZO thickness (13 nm) was confirmed by ellipsometer measurement on the planar part of the sample. By measuring the total diameter of the nanowire with 13-nm HZO ferroelectric oxides, we can estimate that the InAs channel diameter is ~23 nm (fig. S1B). Next, the gate is defined using a 60-nm sputtered W aligned via an S1813 (photoresist) back-etch mask followed by dry etching (SF6:Ar), which sets the L_g (see fig. S2B). The top HZO was then removed by wet etching in hydrofluoric acid (HF) 1:400 to expose the source contact region. Rapid thermal annealing was thereafter used to crystalize the HZO ferroelectric film at 450°C for 30 s in a nitrogen ambient (fig. S2C). The device was finalized by the metallization for contacts (sputtered 10-nm Ni/200-nm Au), and 10-nm Al_2O_3 was used as the top spacer to isolate the gate and source (fig. S2D). The ferroelectricity in the planar HZO film of the same nanowire sample was verified by a conventional polarization-voltage hysteresis measurement (see text S2).

Electrical characterization

All the *I-V* electrical characterization was performed in an MPI TS2000-SE probe station using a Keysight B1500A parameter analyzer. To enable pulsed measurements, a B1530A waveform generator module was used for pulsed *I-V* measurements as well as for fast voltage pulses to stimulate the ferroelectric switching at the HZO gate. For DC *I-V* measurements, high-resolution source measure units (SMUs) coupled with E5288A Auto-sense units were used. Capacitance-voltage measurements were performed in a Lake Shore CRX-4K cryogenic probe station using an Agilent 4294A impedance analyzer.

RTS noise measurements and analysis

RTS noise was measured in the MPI TS2000-SE probe station using the high-resolution SMUs coupled with E5288A Auto-sense units in the Keysight B1500A parameter analyzer as well. All the data were acquired with a time resolution of 10 ms at various fixed V_{GS} and constant V_{DS} (0.1 V). Sufficient time is required to obtain at least a hundred transitions. The capture/emission time constants ($\tau_{c/e}$) were obtained from the measured data fitting the exponential distribution (inset in Fig. 4C) to the histogram of the time spent in the capture (t_c in high current level) and emission process (t_e in low current level), as shown in Fig. 4B. The time constant extracted from the condition $\tau_c = \tau_e$ can be determined by the depth of the defect in the oxide with simplification that elastic tunneling drives the capture and emission process. Thus, the time constant decays exponentially as

$$\tau_{c/e} = \tau_0 \exp(z/l_{tl})$$

where τ_0 is a constant in terms of capture into a defect at the channel/oxide interface, z is the depth of the defect in the oxide from the interface, and l_{tl} is the tunneling attenuation length, which is defined as $l_{tl} = \left[\frac{4\pi}{h}\sqrt{2m^*_{ox}\Phi_B}\right]^{-1}$ according to Wentzel-Kramers-Brillouin theory (*57*), with the Planck constant h, the oxide effective mass m^*_{ox}, and the energy barrier height of the InAs channel to the HZO gate Φ_B. Here, we simply chose Φ_B = 2.3 eV from the barrier height of InAs/HfO_2 (*33*) owing to negligible difference in the affinity between HfO_2 and ZrO_2 (*62*). In addition, m^*_{ox} = 0.12 m_0 (electron rest mass m_0) is selected from (*63*), ignoring the difference in m^*_{ox} before and after ferroelectric switching. Therefore, l_{tl} can approximate to 0.18 nm. Although many different values for τ_0 ranging from 6.6×10^{-14} s (*64*) to 10^{-10} s (*65*) can be found in literature, the depth z, however, only varies from 4 to 5 nm by taking the up and down limits, which will not change the physics interpretation of the results. For simplicity, we here take $\tau_0 = 10^{-10}$ s for the estimation. Thus, the similar time constant (0.55 and 0.67 s) obtained in Fig. 4 gives the same location of the defects in the oxide with the depth $z \approx 4$ nm.

Supplementary Materials

This PDF file includes:
Supplementary Text
Figs. S1 to S10
Tables S1 and S2
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Acknowledgments: We would like to thank E. Lind from Lund University for discussions of TFET-related physics and point charge modeling. We would also like to thank R. Athle from Lund University for his contribution to the focused ion beam processing of the sample. **Funding:** This work was supported in part by the Swedish Research Council under grant 2016-06186 Electronics beyond kT/q and in part by the European Research Council under grant 101019147 Dynamic Properties of Ferroelectric III-V MOSFETs. **Author contributions:** Conceptualization: Z.Z., A.E.O.P., and L.-E.W. Methodology: Z.Z. and A.E.O.P. Investigation: Z.Z. and A.E.O.P. Visualization: Z.Z. Supervision: L.-E.W. Writing—original draft: Z.Z. Writing—review and editing: Z.Z., A.E.O.P., and L.-E.W. All the authors discussed and revised the final manuscript. **Competing interests:** The authors declare that they have no competing interests. **Data and materials availability:** All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials.

Submitted 2 September 2022
Accepted 4 January 2023
Published 3 February 2023
10.1126/sciadv.ade7098