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A 1-nS 1-V Sub-1-μW Linear CMOS OTA with Rail-to-Rail Input for Hz-Band Sensory Interfaces

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Abstract: The paper presents an operational transconductance amplifier (OTA) with low transconductance (0.62–6.28 nS) and low power consumption (28–270 nW) for the low-frequency analog front-ends in biomedical sensor interfaces. The proposed OTA implements an innovative, highly linear voltage-to-current converter based on the channel-length-modulation effect, which can be rail-to-rail driven. At 1-V supply and 1-V_{pp} asymmetrical input driving, the linearity error in the current-voltage characteristics is 1.5%, while the total harmonic distortion (THD) of the output current is 0.8%. For a symmetrical 2-V_{pp} input drive, the linearity error is 0.3%, whereas THD reaches 0.2%. The linearity is robust for the mismatch and the process-voltage-and-temperature (PVT) variations. The temperature drift of transconductance is 10 pS/°C. The prototype circuit was fabricated in 180-nanometer CMOS technology.

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1. Introduction

Operational transconductance amplifiers (OTAs) with a very low conversion ratio of 10^{-11} to 10^{-7} A/V (hereinafter referred to as low-transconductance amplifiers, LTA) are used in analog pre-processing of very-low-frequency biomedical signals. Before digitalization, the analog biomedical signal is amplified and pre-filtered as illustrated in Figure 1 [1–5]. First, the signal is amplified by a low noise amplifier (LNA). Then, the signal amplitude is corrected by a variable gain amplifier (VGA) in order to make it suitable for the input of an analog-to-digital converter (ADC). The analog filter reduces the bandwidth to minimize signal distortion that results from the aliasing effect. LNA, VGA and the filter constitute an analog front-end. It should be noted that the filter does not have to be implemented as an individual block. Instead, the filtering component can be embedded into LNA and VGA through the limitation of their bandwidth [1,6].

The amplitude of biomedical signal ranges from a few μV to several tens of mV, and its frequency is from 0.01 Hz to 3 kHz [6]. To achieve optimal processing dynamics, the front-end is integrated with ADC in a single chip. However, the integration of low-frequency circuits is a challenge. The corner frequency is associated with the RC-time-constant, i.e., $f \approx 1/(2\pi RC)$. In a typical CMOS process, resistors can be made of polysilicon with a resistivity of 10^3 Ω/square, and capacitors made of polysilicon-insulator-polysilicon or metal-insulator-metal layers with a unit capacitance of 10^{-15} F/μm². Due to large area requirements, the practical values of the resistances and capacitances in integrated circuits are $R < 100$ kΩ and $C < 100$ pF, whereas the corresponding corner frequency is $f > 15$ kHz. For further reduction of frequency, the RC-time-constant can be increased using active techniques

such as the capacitance multiplication and resistance emulation. Examples of using the capacitance (Miller's) multiplication in front-ends can be found in [1,7]. However, the majority of the available literature focuses on LTA-based emulation of large resistances [2,3,8–18]. LTAs emulate resistors as large as 10^7–10^{11} Ω while occupying a reasonable area of 0.01 mm^2 to 0.1 mm^2 [2,3,8–18]. However, when compared to passive components, the performance figures of active resistors such as linearity, temperature stability and noise are worse. Improvement of these parameters is one of the main goals of contemporary research studies [12].
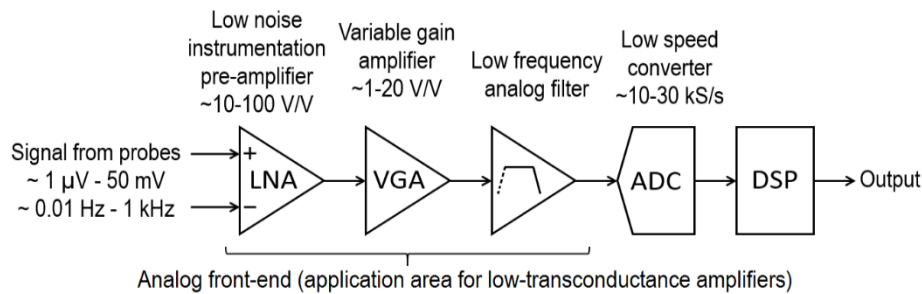

Figure 1. The main components of a microelectronic system processing low-frequency signals.

This work presents an innovative LTA that is developed and manufactured in a 0.18-μm CMOS technology at the Taiwan Semiconductor Manufacturing Company (TSMC). LTA uses the so-called Early effect (channel-length-modulation effect) in a field effect transistor (FET) to directly emulate high resistance. The relationship between the output current and the input voltage of LTA is linear from the ground to the supply voltage. The circuit design is relatively simple and does not require special optimization. Owing to the use of sub-microwatt power consumption and 1-V supply, it is suitable for use in low-power low-voltage biomedical interfaces. The following chapters present the operating principle, circuit details, theoretical analysis and prototype measurement results.

2. Voltage-to-Current Conversion Using Channel-Length-Modulation Effect

2.1. Operation Principles

The proposed voltage-to-low-current converter is shown in Figure 2a. The conversion mechanism is the same as in [18]; however, the proposed converter circuit is improved so as to support operation with low-supply voltage. Furthermore, the structure can be rail-to-rail driven.

(**a**)   (**b**)
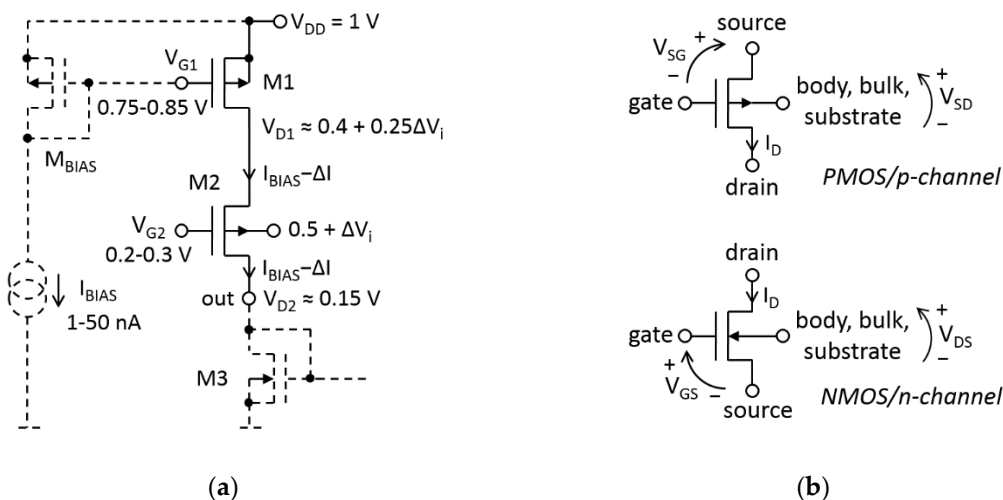
Figure 2. A voltage-to-low-current conversion utilizing the channel-length-modulation effect in MOSFET: (**a**) the realization in CMOS technology; (**b**) MOSFET's notation.

The input signal is ΔV_i and the output signal is ΔI. Here, saturation of all transistors is assumed. The transistor M_1 is a DC current source that is generating the bias current I_{BIAS}. M_2 is a bulk-driven voltage follower. It transfers ΔV_i from the bulk of M_2 to the drain of M_1 with a factor of about 0.25 V/V. The deviation in the drain current of M_1 caused by the channel-length-modulation can be expressed as follows:

$$I_{D1} - \Delta I_{D1} = I_{BIAS} - \Delta I = I_{BIAS}(1 + \lambda_p \Delta V_{SD1}) = I_{BIAS}(1 + \lambda_p(\Delta V_{DD} - \Delta V_{D1})) \tag{1}$$

where λ_p is the channel-length-modulation factor in a p-channel device for given channel length. The deviation of current can also be calculated using an alternative formula.

$$I_{D1} - \Delta I_{D1} = I_{BIAS} - \Delta I = I_{BIAS}(1 + \Delta V_{SD1}/(V_{Ep}L_1)) = I_{BIAS}(1 + (\Delta V_{DD} - \Delta V_{D1})/(V_{Ep}L_1)) \tag{2}$$

where V_{Ep} is the p-channel devices Early voltage per unit-channel-length [19], and L_1 is the length of the M_1 channel.

Assuming $\Delta V_{D1} \approx 0.25\Delta V_i$ and $\Delta V_{DD} = 0$, the I-V conversion factor, defined as transconductance $G_m = \Delta I/\Delta V_i$, can be simply calculated from Equation (1) or (2):

$$G_m = \Delta I/\Delta V_i \approx 0.25 \cdot I_{BIAS} \cdot \lambda_p \tag{3}$$

$$G_m = \Delta I/\Delta V_i \approx 0.25 \cdot I_{BIAS}/(V_{Ep} \cdot L_1). \tag{4}$$

When M_1 and M_2 are saturated, Equations (1)–(4) are valid regardless of the inversion levels in M_1 and M_2. However, to achieve G_m of the order of 10^{-9} A/V, the inversion levels of M_1 and M_2 should be weak or at most moderate. The selected operating points, shown in Figure 2a, ensure the proper transistor operating range for the standard 180-nm CMOS process. For example, transistors with $L_1 = 200$ nm, $V_{Ep} = 8.8$ V/μm and $I_{BIAS} = 10$ nA will give $G_m \approx 1.4$ nA/V (1.4 nS).

The resistance seen from the M_2 source is much smaller than the output resistance of M_1; thus, ΔI is entirely transferred from the M_1 drain to the converter's output (out). Next, ΔI is reflected in a current mirror, part of which is the diode-connected transistor M_3.

2.2. Robustness to Unfavorable Factors

As long as FET remains saturated, the channel-length-modulation effect in FET is linear over a wide range of operating points [20]. Therefore, the impact of undesirable effects, such as transistor mismatch, tolerances of the manufacturing process or temperature variations on the linearity of the converter, are limited. Notwithstanding, the mentioned factors affect the G_m through changes of I_{BIAS}, λ_p (or $V_{Ep}L_1$) and the follower's gain (factor 0.25). However, measurements of the prototype converter show that the real value of G_m differs from a predicted value by about only 10%.

Another aspect that requires detailed analysis involves the demonstration of the effect of temperature on G_m. The increase of the current in M_1 (ΔI) is equal to the product of the drain voltage increase (ΔV_{D1}) and the drain-source conductance (g_{DS1}), i.e., $\Delta I = \Delta V_{D1} \cdot g_{DS1}$. The conductance $g_{DS1} = I_{BIAS}/(V_{Ep}L_1)$ results from the effect of channel length modulation. Hence, G_m can be expressed by the formula that is more accurate than Equation (4), i.e.,

$$G_m = \frac{\Delta I}{\Delta V_i} = \frac{\Delta V_{D1}}{\Delta V_i} \cdot g_{DS1} = \frac{\Delta V_{D1}}{\Delta V_i} \cdot \frac{I_{BIAS}}{V_{Ep}L_1} \tag{5}$$

Here, V_{Ep} and L_1 do not depend on the temperature, whereas I_{BIAS} can be stabilized. The only temperature dependent factor in Equation (5) is $\Delta V_{D1}/\Delta V_i$, i.e., the gain of the M_2 follower. It can be determined as

$$\frac{\Delta V_{D1}}{\Delta V_i} = \frac{g_{mb2}}{g_{mb2} + g_{m2} + g_{DS2} + g_{DS1} + \frac{g_{DS1}g_{DS2}}{g_{m3}+g_{DS3}}} \cong \frac{1}{\frac{g_{m2}}{g_{mb2}} + 1} \approx 0.25 \tag{6}$$

where g_{m2} and g_{mb2} are the gate and bulk transconductances of M_2, respectively.

Using the detailed formulas of [20], one can show that the dependence of the g_{m2}/g_{mb2} ratio on temperature is relatively weak. This implies that for stable I_{BIAS} in the M1-M2-M3 branch, G_m does not depend on temperature.

3. Low-G_m OTA (LTA)

Based on the two converters from Figure 2a, an amplifier with differential input was developed (cf. Figure 3). The currents ΔI_+ and ΔI_- from the two converters flow to the amplifier's output (out) through two independent tracks. In other words, ΔI_+ flows in the non-inverting path containing one mirror composed of the transistors M_{3+} to M_{6+}. The ΔI_- flows through the inverting path containing two mirrors formed by transistors M_{3-} to M_{11-}. All mirrors have a 1:1 ratio.
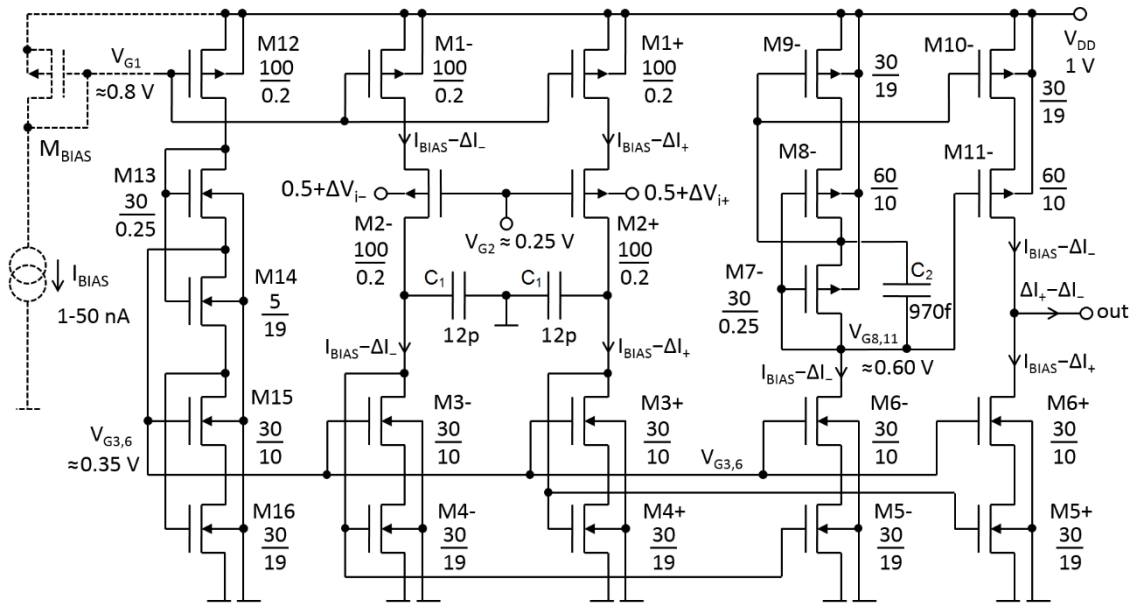

Figure 3. Complete electrical diagram of the low-G_m OTA (LTA) prototype. The dashed lines represent an in-chip generator of V_{G1}.

The amplifier's transconductance for differential input ($G_{m,diff}$) is exactly equal to G_m, i.e.,

$$G_{m,diff} = \frac{\Delta I_{out}}{\Delta V_{i,diff}} = \frac{\Delta I_+ - \Delta I_-}{\Delta V_{i+} - \Delta V_{i-}} = \frac{G_m \Delta V_{i+} - G_m \Delta V_-}{\Delta V_{i+} - \Delta V_{i-}} = G_m. \tag{7}$$

The output conductance of the amplifier (G_{out}) should be much smaller than G_m, i.e., $G_{out} << 1$ nS. This was achieved by using long-channel transistors and cascodes. The cascodes consisting of n-channel transistors are biased by $V_{G3,6}$. The latter is generated by the $M_{12}-M_{16}$ branch. The "p-channel" cascodes are biased by the $V_{G8,11}$ generated by M_{7-}. All transistors in Figure 3 are standard 1.8-V thin-oxide with nominal-threshold-voltages of 0.42 V and -0.5 V for n-channel and p-channel transistors, respectively. Transistors' dimensions (width/length expressed in μm/μm) are given in the schematic, whereas the rationale behind selecting specific dimensions is explained in Section 4.2. The schematic also shows the DC bias voltages at V_{DD} of 1 V. Two capacitors of C_1 attenuate a possible overshoot in the step transient response of the source followers M_{2+} and M_{2-} [21]. A real pole (p) due to the parallel combination of C_1 and g_{m4} (i.e., $p \cong g_{m4}/C_1$) cancels a zero (z) due to C_{sb2} and g_{mb2} (i.e., $z \cong g_{mb2}/C_{sb2}$) in M_{2+} and M_{2-}. A capacitor of C_2 is a "by-pass" for an AC current flowing through the bias transistor M_{7-}. It should be emphasized that these capacitors are not critical elements and have been added to the prototype circuit for research purposes only.

Figure 4 shows a selected fragment of a prototype microchip that embeds LTAs. The size of a single LTA (marked using a white rectangle) is 174 µm × 156 µm. The capacitors, located close to the microstructure surface, are clearly visible. There are two 12-picofarad capacitors, each of which is composed of 10 smaller capacitors (two arrays of capacitors, each of which contains 10 components), and one 970-femtofarad capacitor (small array consisting of 2 capacitors).
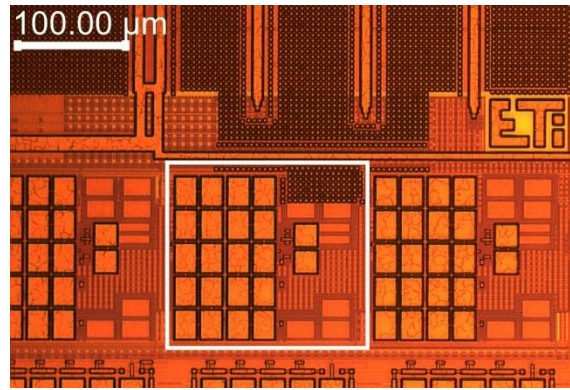
Figure 4. Micro photography of the prototype integrated circuit. A single piece of LTA is marked using a white rectangle.

4. Performances of the Prototype

4.1. Linearity of Current-Voltage Characteristics

The linearity of current-voltage characteristics was measured for unfavorable asymmetrical excitation when the input V_{i+} was fixed at a constant potential of 0.5 V, and while the V_{i-} was swept from 0 V to V_{DD} = 1 V. The measured DC characteristics I_{out} vs. V_{i-} for several values of the I_{BIAS} source ranging from 5 nA to 50 nA are plotted in Figure 5a. The characteristics obtained from the pre-production simulation (dashed lines) are also shown.

To calculate a linearity error of the measured I_{out} vs. V_{i-}, the ideal responses were first obtained using the linear regression and the least squares method. Next, the linearity error was calculated as the difference between the measured I_{out} and the corresponding ideal I_{out} divided by a full range of I_{out} values, i.e., $(I_{out,meas} - I_{out,ideal})/I_{out,full-range}$. The calculated results (expressed in percent) were plotted in Figure 5c. The obtained error values are relatively low and range from −1% to +1.5% max. The curvature of the I_{out} vs. the V_{i-} plots is better visualized using derivatives dI_{out}/dV_{i-}, as shown in Figure 5b.

The value of dI_{out}/dV_{i-} at 0.5 V is equal to the nominal transconductance of the amplifier, i.e., $G_m = dI_{out}/dV_{i-}|_{Vi- = 0.5}$. The nominal G_m can be tuned from 0.62 nA/V to 6.28 nA/V by changing the source I_{BIAS} from 5 nA to 50 nA. The percentage difference between dI_{out}/dV_{i-} and the target G_m (i.e., the G_m-deviation error) is at most ±12% over an entire (rail-to-rail) input range. Detailed plots of the G_m deviation error are in Figure 5d.

The amplifier was also tested for harmonic distortion. The results of measuring the harmonic content in I_{out} for 1-kHz sinusoidal excitation are shown in Figure 6. The THD reaches 0.8% for the maximal V_{i-} of 1 V_{pp}.

(**a**)

(**b**)

(**c**)

(**d**)
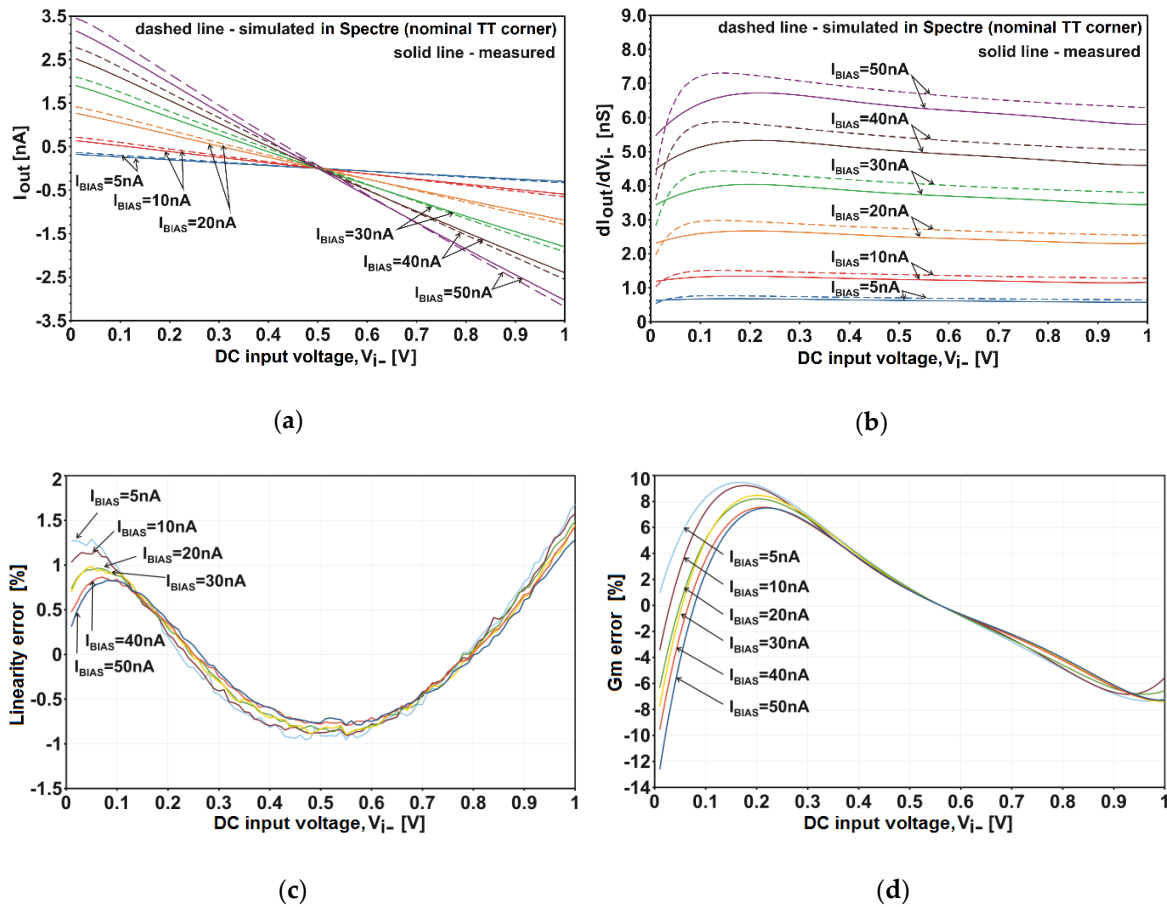
Figure 5. DC characteristics of the amplifier from Figure 3 at asymmetrical drive: (**a**) I_{out} vs. V_{i-}; (**b**) derivatives dI_{out}/dV_{i-}; (**c**) linearity error of the measured I_{out} vs. V_{i-} plots; (**d**) deviation error of the measured dI_{out}/dV_{i-} plots (i.e., deviation error of G_m). The V_{i+} is fixed at 0.5 V, V_{DD} is 1 V and temperature is 27 °C.
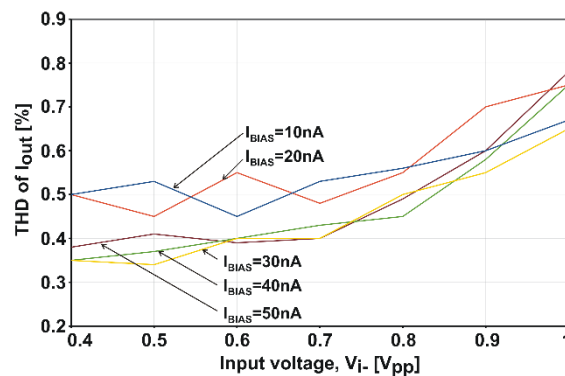
Figure 6. Measured THD (total harmonic distortion) of I_{out} at an asymmetrical input driving. V_{DD} is 1 V and T is 27 °C.

Clearly, nonlinearities are smaller when both inputs of the amplifier are driven symmetrically, as such a configuration ensures the highest suppression of even harmonics. It should be emphasized that in practice, an input differential signal, ($V_{i+}-V_{i-}$), is never balanced in amplifier applications with a non-differential output. However, it is worth providing results for a symmetrical excitation, because the circuit in Figure 3 can be easily equipped with a second output and adapted to "fully-balanced" applications. With symmetrical excitation with a maximum value of $V_{i+} - V_{i-} = 2$ V$_{pp}$, THD reaches

only 0.18%. The $G_{m,diff}$ deviation is ±1.5% over the 2-V_{pp} input range. Detailed plots of the derivative $dI_{out}/(dV_{i+} - dV_{i-})$ are in Figure 7a, and the corresponding plots of the $G_{m,diff}$ deviation error are in Figure 7b.


(**a**) (**b**)
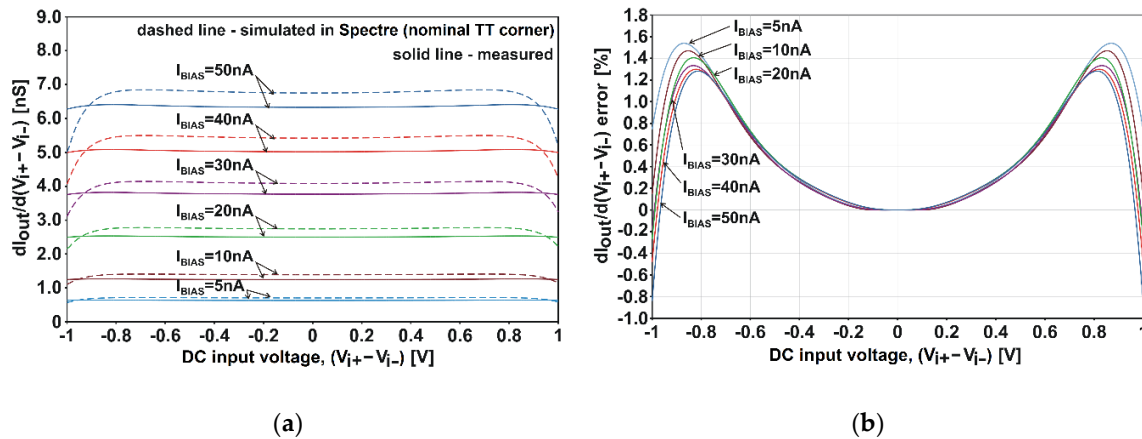
Figure 7. DC characteristics of the amplifier of Figure 3 at the symmetrical input drive: (**a**) derivatives $dI_{out}/d(V_{i+} - V_{i-})$; (**b**) deviation error of the measured $dI_{out}/d(V_{i+} - V_{i-})$ plots (i.e., deviation error of $G_{m,diff}$). V_{DD} is 1 V and T is 27 °C.

It should be emphasized that the prototype amplifier features better linearity than predicted by the simulations. This is clearly visible in Figure 5b in the area for $V_{i-} < 0.2$ V (see also Figures A1 and A2 in Appendix A). The bulk-effect (body-effect) in FET is not accurately modelled for the low potentials of bulk.

4.2. Frequency and Noise Characteristics

A small-signal transconductance was measured in the range of 1 Hz–200 kHz. Measurements were performed separately for each of the inputs. Figure 8a shows the results only for the V_{i-} input, because this is the worst case in terms of frequency properties (because the inverting track is longer than the non-inverting track). The values of G_m for the considered frequencies are consistent with the values of dI_{out}/dV_{i-} at $V_{i-} = 0.5$ V obtained from the DC measurements shown in Figure 5b. The measured −3-dB frequency is lower than the one predicted in simulations by about 90–200 kHz. This is because the values of correcting capacitors used in the prototype amplifier are too large. The boost of the G_m characteristic for $I_{BIAS} = 5$ nA is caused by undercompensation of the measuring path.

Noise characteristics obtained from the simulation are plotted in Figure 8b. In the range below 1 Hz, the 1/f noise reaches over 200 $\mu V/(Hz)^{1/2}$. Above 100 Hz, the thermal noise is about 50 $\mu V/(Hz)^{1/2}$. The current mirrors, particularly the transistors M_{4-}, M_{4+}, M_{5-}, M_{5+}, M_{9-} and M_{10-}, are the greatest contributors to the total noise. This can be explained using the electrical diagram depicted in Figure 9. The schematic contains only the transistors that significantly contribute to the total output noise. The cascode transistors (and their biasings) are removed because their contributions to the noise are minor. Also, the noise of M_2+ and M_2- is omitted, as those devices acts as cascodes for M_1+ and M_1-.

(a) (b)
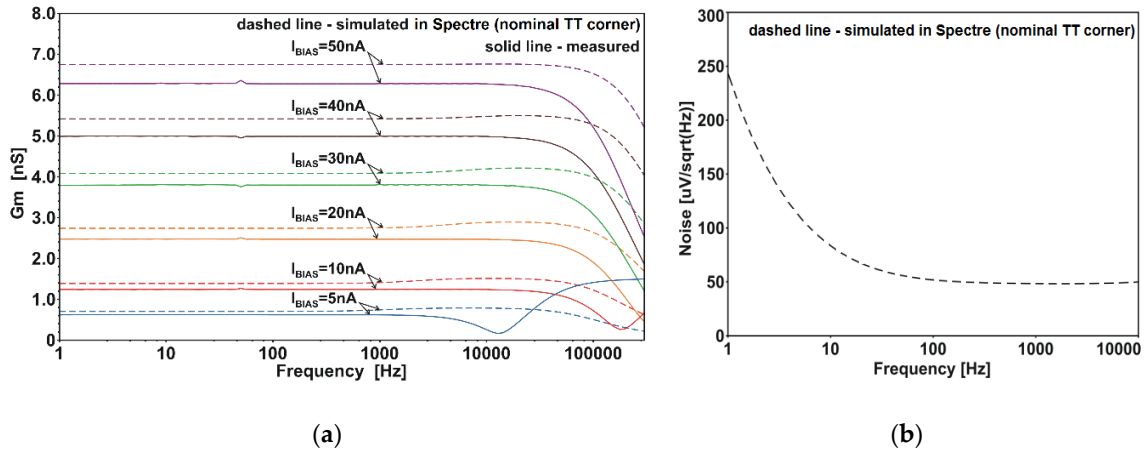
Figure 8. Small-signal characteristics: (**a**) of the transconductance; (**b**) of the input-referred noise. AC signal is applied to the inverting input V_{i-}. DC levels on inputs are $V_{i-} = V_{i+} = 0.5$ V. The V_{DD} is 1 V.
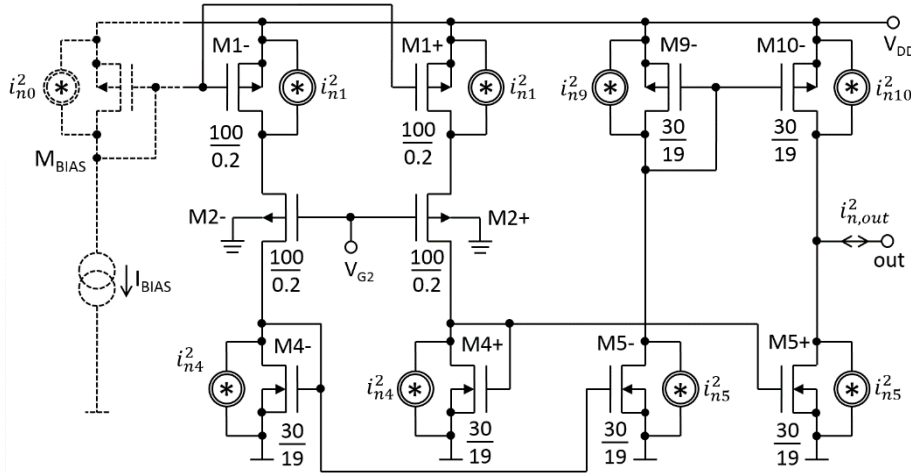
Figure 9. The simplified electrical diagram of the LTA for the noise calculation.

In Figure 9, the all noise currents propagate through the current mirrors with a gain of 1, so the total mean-square output noise can be expressed as the sum of the particular noise currents:

$$i^2_{n,out} = 2i^2_{n1} + 2i^2_{n4} + 2i^2_{n5} + i^2_{n9} + i^2_{n10} = 2i^2_{n1} + 4i^2_{n4,5} + 2i^2_{n9,10}. \tag{8}$$

The noise current source (thermal + flicker) of MOSFET can be modelled as follows [22]:

$$i^2_n = 4kT\gamma g_m + \frac{K_F g^2_m}{f C_{OX} WL} \left[\text{A}^2/\text{Hz} \right] \tag{9}$$

where k is Boltzmann's constant, T is temperature, γ is a constant coefficient ($\gamma \approx 2/3$), K_F is the technological flicker-noise parameter and f is the frequency. Furthermore, C_{OX} denotes gate-capacitance-per-unit-area, whereas W and L represent the width and length of MOSFET, respectively.

For weak-inversion, a MOSFET transconductance (g_m) is mainly determined by a biasing current and almost does not depend on W and L. Consequently, the parameter g_m is almost the same for all the devices shown in Figure 9, i.e.,

$$g_{m1} \cong g_{m4,5} \cong g_{m9,10} = g_m \cong I_{BIAS} q/kT \tag{10}$$

where q is the electron charge.

It should be noted that contribution of all the transistors in Figure 9 to the thermal noise—the first component of Equation (9)—is equal. Similarly, their contribution to the flicker noise—the second component of Equation (9)—is nearly equal. Notwithstanding, flicker noise can be reduced by large values of W and L.

Based on Equations (7)–(10) and Figure 2b, the input-referred noise of the LTA in Figure 3 is given as:

$$e_{n,in}^2 = \frac{i_{n,out}^2}{G_{m,diff}^2} = 32qV_{Ep}^2L_1^2\left[\frac{16\gamma}{I_{BIAS}} + \frac{q}{k^2T^2fC_{OX}}\left(\frac{K_{FP}}{W_1L_1} + \frac{K_{FP}}{W_{9,10}L_{9,10}} + \frac{2K_{FN}}{W_{4,5}L_{4,5}}\right)\right] [V^2/Hz] \quad (11)$$

where K_{FP} and K_{FN} denote the K_F for the p-channel and n-channel transistors, respectively.

As can be seen from Equation (11), the low value of the total noise of LTA for the given I_{BIAS} can be maintained using current mirrors characterized by large $W_{4,5,9,10}$ and large $L_{4,5,9,10}$, as well as M_{1+} and M_{1-} with large W_1 and small L_1. The parameter L_1 was set to 0.20 μm, which is close to the technological minimum of 0.18 μm, but still sufficient to achieve a G_m of the order of nS (cf. Section 2.1). It is worth noting that parameters L_2 and W_2 do not affect the noise. They have been set to $L_2 = 0.20$ μm and $W_2 = 100$ μm in order to minimize the gate-source voltage of M_2. Similarly, parameters $L_{3,6,8,11}$ and $W_{3,6,8,11}$ do not affect the noise, but they have been set to over 10 μm for better matching.

4.3. PSRR and CMRR

Owing to p-channel-based implementation, the amplifier's input stage features small flicker noise ($K_{FP} < K_{FN}$) and supports rail-to-rail bulk driving [23]. However, for proper operation, the biasing voltage V_{G2} must be generated so that the difference $V_{DD} - V_{G2}$ is constant. Otherwise, the unwanted AC signal on the V_{DD} line will be visible in ΔI, resulting in a reduced power-supply-rejection-ratio (PSRR). The V_{G2} can be generated in a relatively simple way, as shown in Figure 10.
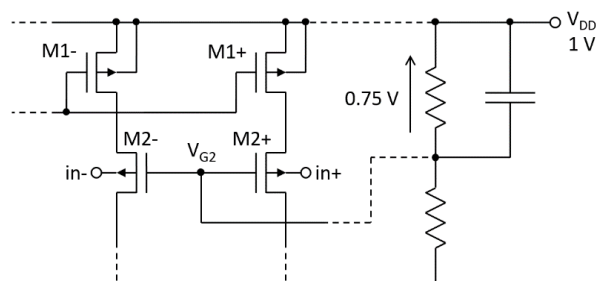
Figure 10. The off-chip generator of V_{G2} used for tests of the prototype LTA of Figure 3.

The input stage does not attenuate the common component of the input differential signal. Hence, it is pseudo-differential. The common component is suppressed at the amplifier's output node by subtracting the currents. However, mismatch of the transistors causes the inverting and non-inverting tracks to not be perfectly matched and for the currents to not be perfectly subtracted. As a consequence, the rejection of the common component is not complete. The same mechanism resulting from the mismatch also weakens the amplifier's resistance to interferences from the V_{DD} line. The mismatch phenomenon is random. Out of the 12 fabricated amplifier prototypes, the worst one had a CMRR (common-mode rejection ratio) of 57 dB and a PSRR of 48 dB.

4.4. Temperature

As already explained in Section 2.2, for stable I_{BIAS}, the effect of temperature changes on G_m is negligible. However, for the circuit of Figure 3, the temperature affects the copy of I_{BIAS} in the non-cascoded mirrors M_{BIAS}-M_{1+} and M_{BIAS}-M_{1-}. As indicated by the simulations, increase of the

temperature from 0 °C to 70 °C, affects the increase of the G_m by 15%. To put that into perspective, drift of the G_m is 2.1 pS/°C and 9.7 pS/°C for $I_{BIAS} = 5$ nA and $I_{BIAS} = 50$ nA, respectively. The simulations were carried out under the assumption that the drift of the I_{BIAS} source is at the level of a typical band-gap source (100 ppm/°C [24]).

4.5. Summary of the Performance Properties

The performance properties of the prototype are summarized in Table 1.

Table 1. Parameters of the prototype LTA at $V_{DD} = 1$ V and 27 °C.

Parameter	Simulated	Measured
Technology/Vendor	Standard 180 nm CMOS 1P6M/TSMC	
Physical dimensions [1]	174 μm × 156 μm	
Supply voltage V_{DD}	1 V (min. 0.8 V, max. 1.8 V)	
Average current consumption [1]	32–290 nA	28–270 nA
G_m tuning range (I_{BIAS} range 5–50 nA)	0.7–6.75 nS	0.62–6.28 nS
G_m temperature drift [2]	2.1 pS/°C @ $I_{BIAS} = 5$ nA 9.7 pS/°C @ $I_{BIAS} = 50$ nA	- -
Input common-mode range	0.1–1 V	0–1 V (rail-to-rail)
THD of I_{out} non-symmetrical driving symmetrical driving	2.4% @ 1 V_{pp}, 1% @ 0.64 V_{pp} 0.47% @ 2.0 V_{pp}	0.8% @ 1 V_{pp} 0.18% @ 2 V_{pp}
Gm deviation (linearity) error non-symmetrical driving symmetrical driving	±22% @ 1 V_{pp} ±12% @ 2 V_{pp}	±12% @ 1 V_{pp} ±1.5% @ 2 V_{pp}
Input-reffered noise	760 μV_{RMS} (integrated over 1–100 Hz)	-
Signal to noise ratio (SNR) non-symmetrical driving symmetrical driving	49.5 dB @ THD = 1% 59.3 dB @ THD = 0.47%	- -
CMRR, PSRR	min. 56 dB, 47 dB [3]	min. 57 dB, 48 dB [4]
Input offset voltage (V_{OS})	max. ± 25 mV [3]	25–50 mV [4]
Mismatch-induced deviation of Gm	max. ± 4.5% [3]	-

[1] Without the circuits drawn with dashed lines in Figure 3. [2] G_m deviation is 15% max when temperature varies from 0 to 70 °C. [3] 200 Monte Carlo runs. [4] For 12 fabricated amplifier samples.

5. Application Example (Simulation Results)

The LTA performance properties have been be validated using the popular application scenario, i.e., the low-pass anti-aliasing G_m-C filter for the EEG/ECG band (0.05~100 Hz). For the system shown in Figure 1, the filter may have a smooth attenuation characteristic, i.e., its order may be low (from 2 to 4) [25–28]. Furthermore, approximation can be realized using Butterworth [28,29] or Bessel functions. Advanced, "sharp" filtration is performed in a digital signal processor (DSP). The advantage of smooth filters is that they do not have significant requirements with respect to the performance of transconductance amplifiers. On the other hand, such filters are often insufficient for performing thorough tests of amplifier circuits. Therefore, in this example, a more demanding 6th order Chebyshev filter is used (cf. Figure 11).
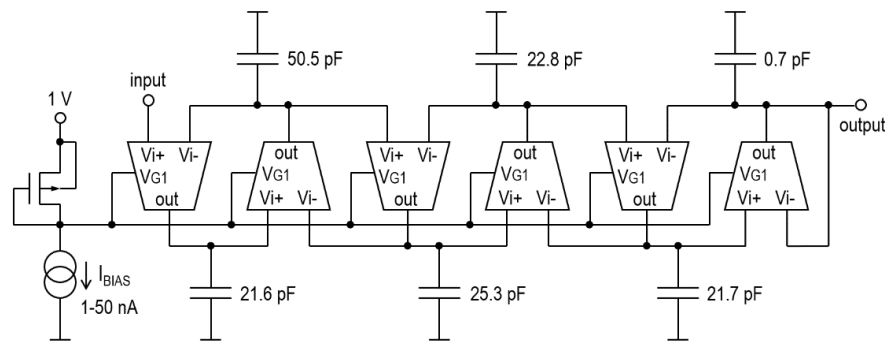
Figure 11. The 6th-order low-pass G_m-C (transconductor-C) filter with Chebyshev approximation.

Under the assumption that transconductors are ideal, the frequency parameters of the filter in Figure 11 are as follows: the gain in the pass-band is 1 *v/v* (0 dB), the amplitude slope is −120 dB/dec and the attenuation in the stop-band is infinite. In reality, however, non-ideal parameters of transconductors that include finite output resistance, as well as parasitic zeros and transmittance poles, contribute to a more gradual slope of the characteristic and limited stop-band attenuation. Figure 12 shows a comparison of an ideal filter (dashed lines) with the one that implements the transconductors shown in Figure 3 (solid lines). The corner frequency of the filter can be tuned from 14.6 Hz to 144.8 Hz by changing the I_{BIAS} between 5 nA and 50 nA. As can be seen, the considered transconductors accurately reproduce characteristics of the filter down to −90 dB, which is a very good result when it comes to analog G_m-C filters. When it comes to the large-signal properties, the output THD is below 1% (−40 dB) for sinusoidal excitation with a V_{pp} amplitude of 0.6 and frequency ten-fold lower than the corner one. When the excitation frequency is close to the corner one, i.e., near the end of the pass-band, the output distortions HD_2 = −36 dB and HD_3 = −55 dB, respectively.
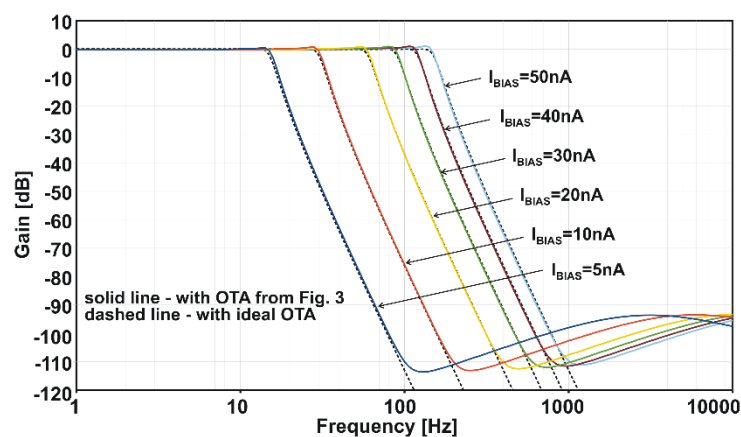
Figure 12. Simulated amplitude responses of the filter from Figure 8.

6. Discussion and Conclusions

Linear LTAs are realized using various techniques such as current division (current splitting), current cancellation, bulk driving, source degeneration or floating gates. The examples can be found in many literature references, e.g., [2,3,8–10,12–17,30,31]. To the best of authors' knowledge, to date, the channel-length-modulation effect for LTA realization has been reported only in [18]. The prototype amplifier solution in [18] is interesting, but it operates with a relatively high supply voltage of 5 V.

The proposed solution has been compared against state-of-the-art circuits from the literature comprising the linear transconductors with possibly close G_m values. The results are collected in Table 2. Most of the solutions are characterized by differential input/output and are only symmetrically driven. In such conditions, the proposed transconductor is the only one that maintains linearity when driven

by a signal (2 V_{pp}) greater than the supply voltage (1 V). However, in the proposed solution, the noise is relatively high and, despite maintaining linearity in a wide range, it does not feature improved SNR as compared other solutions. On the other hand, the proposed circuit features improved performance in terms of low power consumption (0.3 μW) and low supply voltage (1 V). Temperature parameters cannot be compared because this parameter is not reported in majority of the available literature.

Table 2. Comparison of linear LTAs (linear low-G_m OTAs).

Parameter	This Work	[12] (BD+CD Case)	[16] (Simulated)	[17]	[18]
Type of input/output	diff./single	diff./single	diff./diff.	diff./single	diff./diff.
G_m	0.62–6.28 nS	9.4 nS	39.5–367.2 nS	0.46–82 nS	30 pS–25 μS
Supply voltage	1 V	2.7 V (±1.35 V)	5 V (±2.5 V)	1.5 V	5 V (±2.5 V)
Power consumption	<0.3 μW (28–270 nW)	4.05 μW (sim.)	160 μW	<1 μW	<300 μW
Input comm.-mode range	rail-to-rail	-	-	rail-to-rail	-
Linear range for symmetrical input	2 V_{pp} @ 0.18% THD	0.9 V_{pp} @ 1% HD_3	2 V_{pp} @ 0.13% THD	1.2 V_{pp} @ 1% THD	2.6 V_{pp} @ 1% THD
Input-referred noise	760 μV_{RMS} (sim.) (1–100 Hz)	104.7 μV_{RMS} (0.01–10 Hz)	332 μV_{RMS} (10–30 kHz)	110 μV_{RMS} (1–100 Hz)	635 μV_{RMS} (1 Hz–2 MHz)
SNR	59.3 dB (sim.) @ 0.47% THD	69.6 dB @ 1% HD_3	~66.5 dB @ 0.13% THD	70 dB @ 1% THD	62 dB @ 1% THD
CMRR/PSRR	56 dB/47 dB	-	>44.8 dB/n.a.	-	>80 dB/>80 dB
CMOS process	0.18 μm	1.2 μm	0.35 μm	0.8 μm	0.35 μm
Layout area	0.027 mm^2	0.22 mm^2	0.006 mm^2	0.04 mm^2	0.046 mm^2

The presented transconductor solution is dedicated to working in a system where high gain is provided by the input LNA. From this perspective, the noise of an antialiasing transconductor-C filter is not of primary concern. Nevertheless, the noise in the proposed transconductor can be reduced through implementation in a single stage topology. It should be worth noting, however, that the single-stage topology is characterized by a narrower driving range. Therefore, choice between the single- and multi-stage topologies is a compromise between maintaining a low-noise and high-driving amplitude. The use of low-noise analog-dedicated CMOS technology (with lower technological parameters K_{FN} and K_{FP} in Equation (11) can also be considered to address the mentioned challenges.
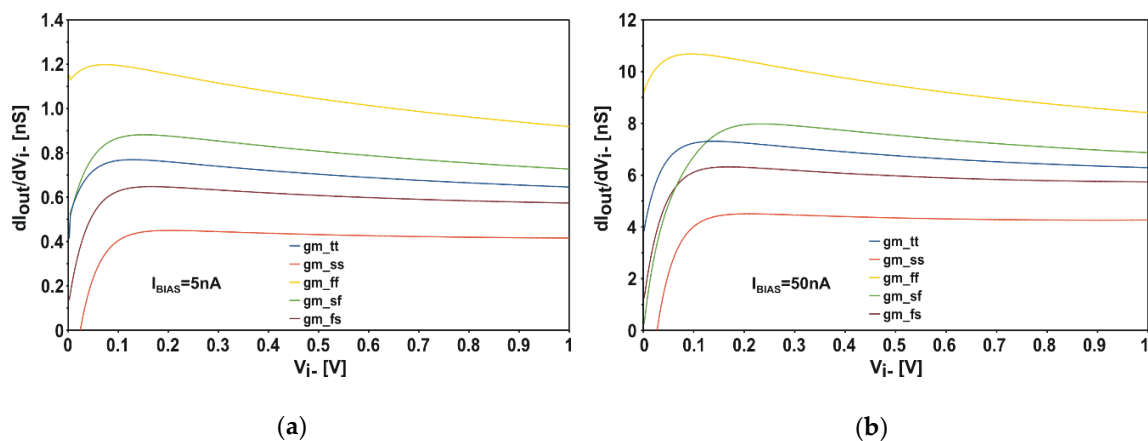
Appendix A

Figures A1 and A2 present simulation results obtained for all corners (worst case analysis). The responses represent supplementary data to the characteristics of Figures 5b and 7b.

(**a**)　　　　　　　　　　　　　　　　　　　　　　　　(**b**)

Figure A1. Corner simulations of the amplifier of Figure 3 at the asymmetrical input drive: (**a**) for 5-nA I_{BIAS}; (**b**) for 50-nA I_{BIAS}. V_{DD} is 1 V.

(**a**)　　　　　　　　　　　　　　　　　　　　　　　　(**b**)
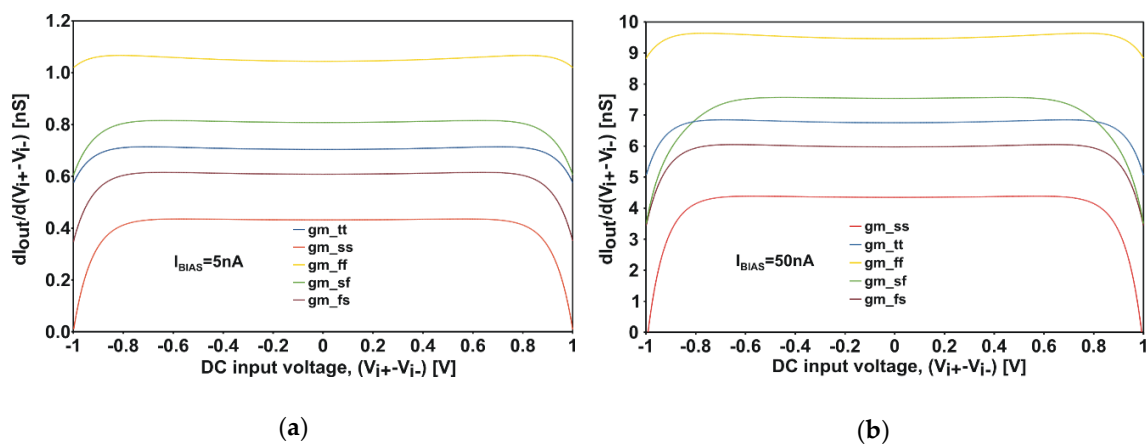
Figure A2. Corner simulations of the amplifier of Figure 3 at the symmetrical input drive: (**a**) for 5-nA I_{BIAS}; (**b**) for 50-nA I_{BIAS}. V_{DD} is 1 V.

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