

## Supporting information

### Ultralow-power in-memory computing based on ferroelectric memcapacitor network

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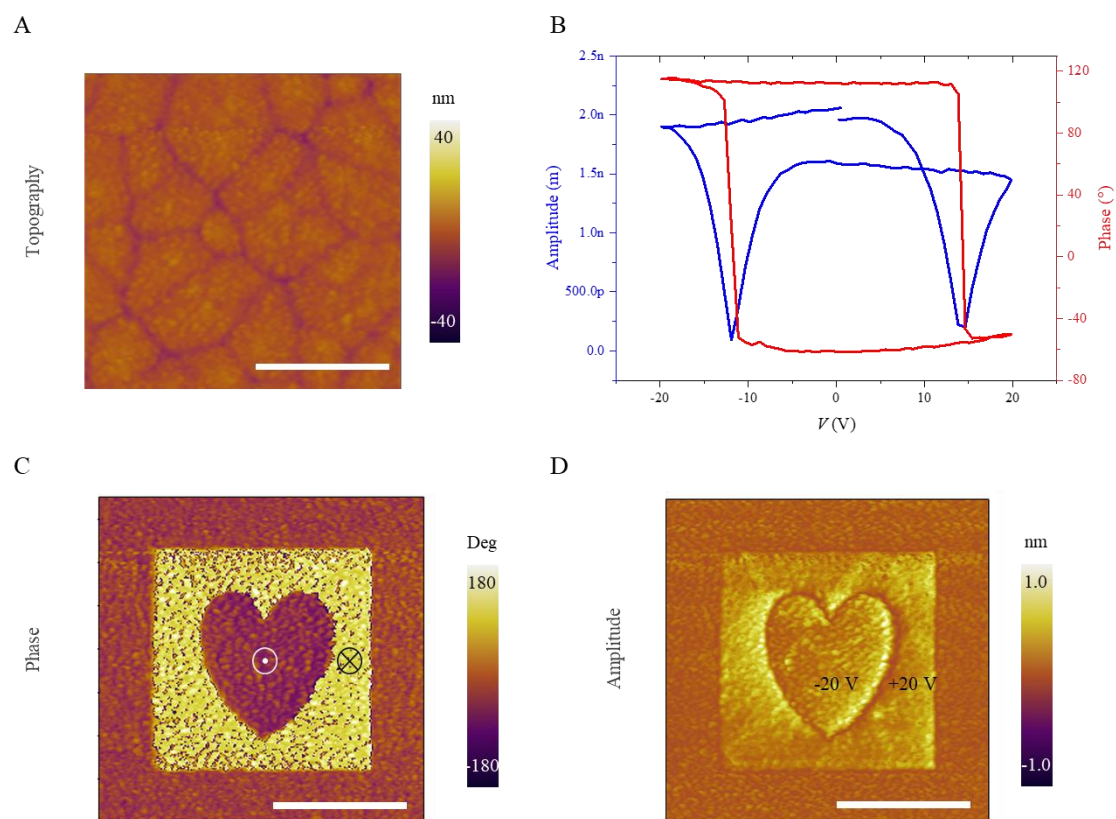
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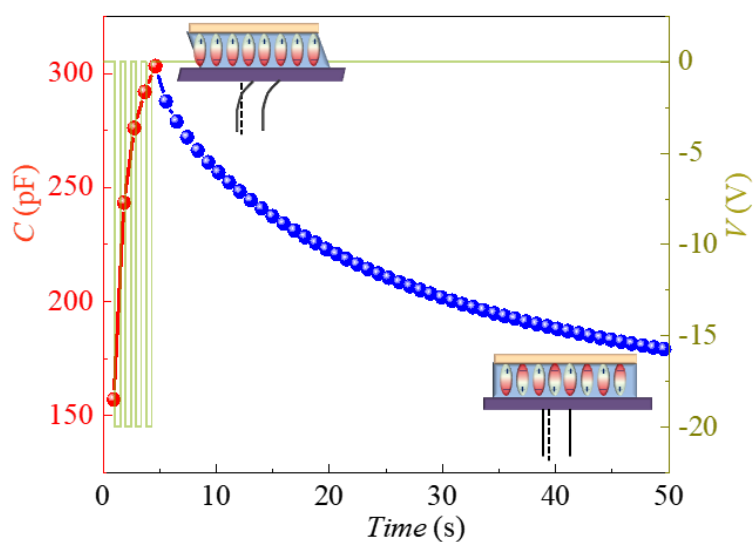
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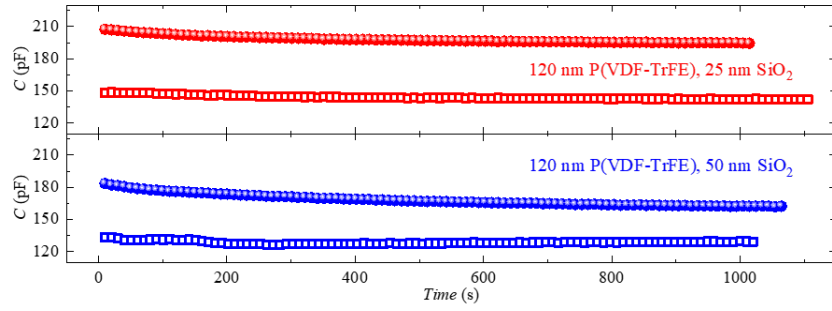
## FIGURES



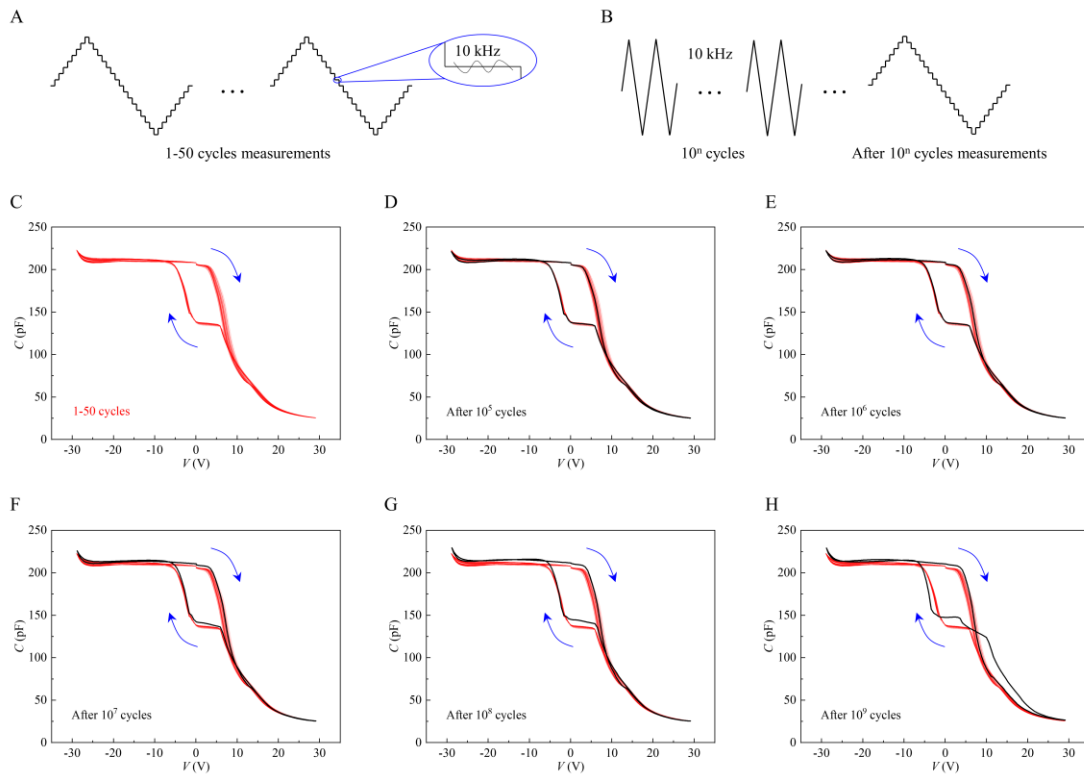
**FIGURE S1** A) AFM topography image of P(VDF-TrFE) thin films. B) PFM Piezoelectric hysteresis loops of P(VDF-TrFE) thin films: phase (red) and amplitude (blue). C) PFM phase and D) amplitude image of P(VDF-TrFE) films after writing a square area on film surface with a positive voltage (+20 V) followed by a smaller “heart” with a negative voltage (-20 V) by a biased conductive tip. The scale bar is 6  $\mu$ m.



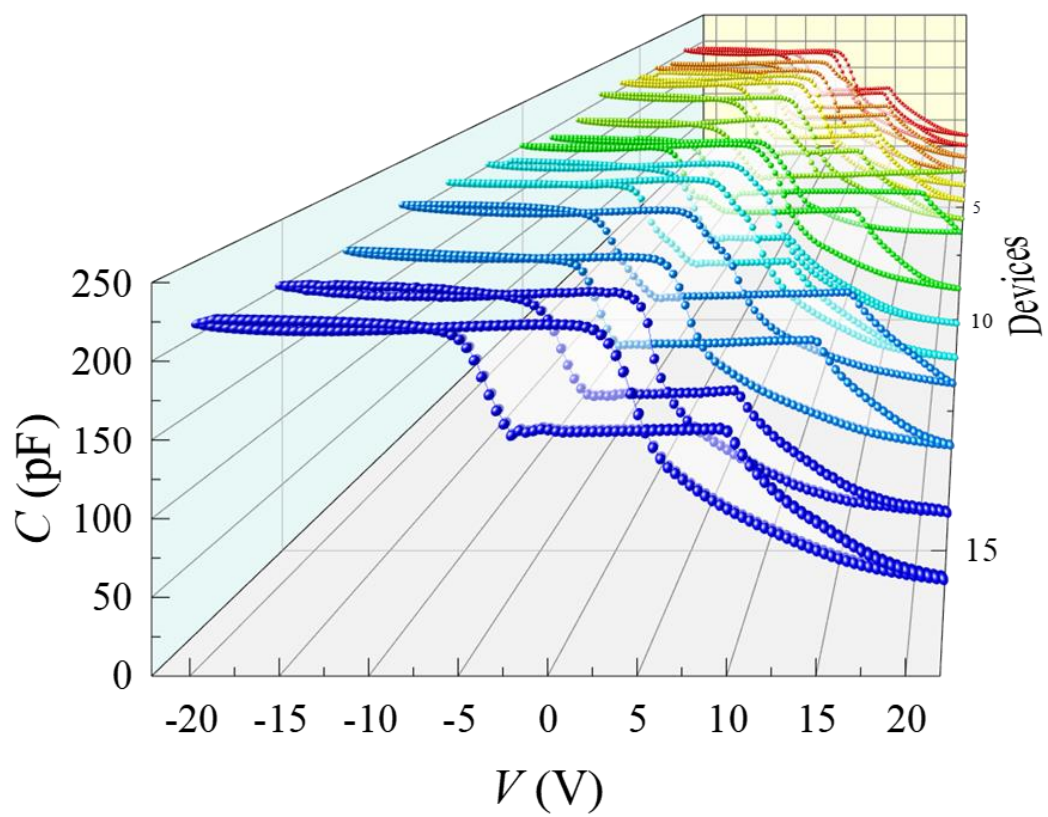
**FIGURE S2** Retention of the programmed high capacitance state in the MFIS memcapacitor with 60 nm-thick P(VDF-TrFE) and 25 nm-thick SiO<sub>2</sub>.



**FIGURE S3** Retention of the highest capacitance state and the lowest capacitance state in a MFMIS memcapacitor with 120 nm-thick P(VDF-TrFE) and 25 nm-thick (red) or 50 nm-thick (blue) SiO<sub>2</sub>.



**FIGURE S4** Evolution of  $C$ - $V$  hysteresis loops under endurance cycles in a MFMIS memcapacitor with 120 nm-thick P(VDF-TrFE) and 25 nm-thick SiO<sub>2</sub>. The amplitude of triangular wave cycles in (D-H) is 30 V, which is larger than the coercive voltage in the MFMIS memcapacitor.



**FIGURE S5**  $C$ - $V$  hysteresis loops for 16 different MFMIS memcapacitors with 120 nm-thick P(VDF-TrFE) and 25 nm-thick SiO<sub>2</sub>.