

Cite this: *RSC Adv.*, 2019, 9, 36293

# Interface tailoring through the supply of optimized oxygen and hydrogen to semiconductors for highly stable top-gate-structured high-mobility oxide thin-film transistors†

Jong Beom Ko, <sup>a</sup> Seung-Hee Lee,<sup>a</sup> Kyung Woo Park <sup>b</sup> and Sang-Hee Ko Park<sup>\*a</sup>

Self-aligned structured oxide thin-film transistors (TFTs) are appropriate candidates for use in the backplanes of high-end displays. Although SiN<sub>x</sub> is an appropriate candidate for use in the gate insulators (GIs) of high-performance driving TFTs, direct deposition of SiN<sub>x</sub> on top of high-mobility oxide semiconductors is impossible due to significant hydrogen (H) incorporation. In this study, we used AlO<sub>x</sub> deposited by thermal atomic layer deposition (T-ALD) as the first GI, as it has good H barrier characteristics. During the T-ALD, however, a small amount of H from H<sub>2</sub>O can also be incorporated into the adjacent active layer. In here, we performed O<sub>2</sub> or N<sub>2</sub>O plasma treatment just prior to the T-ALD process to control the carrier density, and utilized H to passivate the defects rather than generate free carriers. While the TFT fabricated without plasma treatment exhibited conductive characteristics, both O<sub>2</sub> and N<sub>2</sub>O plasma-treated TFTs exhibited good transfer characteristics, with a V<sub>th</sub> of 2 V and high mobility (~30 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>). Although the TFT with a plasma-enhanced atomic layer deposited (PE-ALD) GI exhibited reasonable on/off characteristics, even without any plasma treatment, it exhibited poor stability. In contrast, the O<sub>2</sub> plasma-treated TFT with T-ALD GI exhibited outstanding stability, *i.e.*, a V<sub>th</sub> shift of 0.23 V under positive-bias temperature stress for 10 ks and a current decay of 1.2% under current stress for 3 ks. Therefore, the T-ALD process for GI deposition can be adopted to yield high-mobility, high-stability top-gate-structured oxide TFTs under O<sub>2</sub> or N<sub>2</sub>O plasma treatment.

Received 2nd September 2019  
Accepted 2nd November 2019

DOI: 10.1039/c9ra06960g

rsc.li/rsc-advances

## Introduction

Amorphous oxide semiconductors (AOSs) are appropriate candidates for the active layers of thin-film transistors (TFTs) due to their numerous advantages, such as high electron mobility, good electrical stability, uniformity over a large area, and easy fabrication.<sup>1–4</sup> Therefore, oxide TFTs are considered the best candidates for use in the backplanes of large-area flat-panel displays (FPDs). Among the various FPDs, those based on active-matrix organic light-emitting diodes (AMOLEDs) and micro-light-emitting diodes (micro-LEDs) have attracted much attention due to their unique advantages, such as vivid color,

high efficiency, and fast response times.<sup>5,6</sup> In particular, they have excellent contrast, and their thinness and lightness make them suitable for use in wall and window displays. Therefore, they are promising candidates for next-generation AM displays with large sizes, high resolutions, and foldability. However, there are many important issues in terms of backplane that should be addressed before AMOLEDs and active matrix micro-LEDs can be used for higher resolution, larger-sized displays. The high mobility of TFTs is essential for fully charging capacitors in a short time. Hence, there is much current research on oxide TFTs with various types of high-mobility materials, such as indium zinc oxide (IZO),<sup>7</sup> indium oxide (InO),<sup>8</sup> zinc oxynitride (ZnON)<sup>9</sup> and Al-doped ITZO (Al:ITZO).<sup>10</sup> Furthermore, among low resistivity metal materials, copper (Cu) should generally be used for electrodes to reduce resistive-capacitive (RC) delay in the pixel arrays of large-sized, high-resolution displays.<sup>11,12</sup>

Among the various TFTs, self-aligned (SA) TFTs are the most suitable for driving large-sized, high-resolution displays, due to their small parasitic capacitance.<sup>13</sup> Therefore, we can increase the capacitance of gate insulators (GIs) in SA TFTs to realize large driving currents. In other words, we can obtain high transconductance values, which vary in proportion to the capacitance

<sup>a</sup>Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea. E-mail: shkp@kaist.ac.kr

<sup>b</sup>Samsung Display, Co. Ltd., 1 Samsung-ro, Yongin-si, Gyeonggi-do 17113, Republic of Korea

† Electronic supplementary information (ESI) available: The overlapped transfer curve of 6 points of each samples after thermal annealing (Fig. S1), bar graph and error bar of the electrical parameters of the each TFTs (Fig. S2), output curves of the devices (Fig. S3), N 1s peaks of XPS of the active surfaces in each treatment conditions (Fig. S4) and the change of V<sub>th</sub> during the PBTS (Fig. S5). See DOI: 10.1039/c9ra06960g



of the GI. High- $k$  dielectric materials, such as  $\text{HfO}_2$ ,<sup>14</sup>  $\text{Y}_2\text{O}_3$ ,<sup>15</sup>  $\text{Si}_3\text{N}_4$ , and  $\text{Al}_2\text{O}_3$  (ref. 16) are good candidates for GIs.<sup>17</sup> Among these,  $\text{SiN}_x$  deposited by plasma-enhanced chemical vapor deposition (PE-CVD) is a suitable candidate for GIs of SA TFTs using Cu electrodes for display applications, because it has both high capacitance and good Cu diffusion barrier characteristics.<sup>18,19</sup> Unfortunately, it is difficult to use  $\text{SiN}_x$  as a GI for SA oxide TFTs, because hydrogen (H) is readily incorporated into the channel during GI deposition, thus increasing the carrier density and shifting turn-on voltage ( $V_{\text{on}}$ ) in the negative direction.<sup>18</sup> As a solution, an H barrier layer can be introduced as a first GI between the active layer and the main  $\text{SiN}_x$  GI to prevent the negative  $V_{\text{on}}$  shift. As  $\text{AlO}_x$  formed by means of atomic layer deposition (ALD) has benefits, such as being an H barrier<sup>18,20</sup> with low leakage current and high breakdown voltage due to a large bandgap,<sup>21</sup> thin  $\text{AlO}_x$  is suitable as the first GI of the double-layered high- $k$  GI for an SA TFT.

It is also essential to ensure stability of high-mobility TFTs under current and bias stress. To obtain highly stable, high-mobility oxide TFTs, both the material and deposition method of the GI should be carefully chosen and designed, especially in the top-gate structure. It is well known that the generation of charge trapping centers at the interface between the channel and GI induces a  $V_{\text{th}}$  shift. In general, GI deposition using plasma sources yields defects in the top-gate TFT. Among the various deposition methods, ALD is known to yield high-quality GIs.<sup>22,23</sup> Many studies on top-gate oxide TFTs with  $\text{AlO}_x$  GIs, achieved by means of thermal-ALD (T-ALD) using  $\text{H}_2\text{O}$  as an oxygen source, have been reported, wherein highly stable oxide TFTs could be fabricated owing to the mitigation of plasma damage.<sup>23</sup> Unfortunately, the T-ALD process of  $\text{AlO}_x$  also induces H incorporation into the active layer from  $\text{H}_2\text{O}$  reactants over very few ALD reaction cycles, resulting in a negative  $V_{\text{on}}$  shift. Thus, T-ALD-processed  $\text{AlO}_x$  GI layers can be adopted by only low-mobility TFTs, and high-mobility oxide TFTs fabricated with a T-ALD  $\text{AlO}_x$  process using  $\text{H}_2\text{O}$  become conductive. Therefore, this may serve as a key method for tailoring interfaces without creating charge trapping centers, and maintaining an appropriate carrier concentration of high-mobility oxide TFTs.

Here, we report a highly stable, high-mobility top-gate bottom-contact-structured oxide TFT that mimics a SA-structured TFT. The first GI, *i.e.*, an  $\text{AlO}_x$  thin layer, is deposited by T-ALD using an  $\text{H}_2\text{O}$  oxygen source, and the second GI, of  $\text{SiN}_x$ , is deposited by PE-CVD. During the T-ALD process, H from the  $\text{H}_2\text{O}$  reactant acts as a shallow donor and increases the carrier density. However, H at the interfaces between the active layer and the GI also acts as a passivator for the defects, thus improving stability.<sup>24–29</sup> Therefore, to realize a high-mobility oxide TFT with good stability, it is important to finely regulate the amount of H so that it behaves as a defect passivator rather than a shallow donor in the high mobility channel region. We applied the  $\text{O}_2$  or  $\text{N}_2\text{O}$  plasma treatment just before the T-ALD process so that the H from the  $\text{H}_2\text{O}$  would act as a passivator for the charge trapping defects generated by the subsequent processes, including plasma treatment.

To verify the plasma treatment effect, oxide TFTs not subject to  $\text{O}_2$  or  $\text{N}_2\text{O}$  plasma treatment before GI deposition were fabricated as references. The transfer and stability characteristics of each TFT, under different plasma treatment and GI deposition conditions, were compared and analyzed. The causes of the differences in performance among the TFTs were scrutinized by analyzing the stacked films using X-ray photoelectron spectroscopy (XPS), secondary-ion mass spectroscopy (SIMS) and Hall measurements. We confirmed that a highly stable, high-mobility oxide TFT with a top-gate structure could be realized by optimizing the H amount and charge trapping centers at the interface, which originated from oxygen-related defects occurring during plasma treatment.

## Experimental

The top-gate bottom-contact TFTs were fabricated under different GI deposition process conditions. As shown in Fig. 1(a), the top-gate bottom-contact TFTs have the same stacking sequences of active layers and GI as SA TFTs. Therefore, our samples are suitable for investigating the effects of GI and plasma treatment on mobility and stability characteristics. First, ITO was patterned as a source and drain. Then, 20 nm of high-mobility Al-doped ITZO<sup>10</sup> was deposited by sputtering, followed by patterning as an active layer. Before the deposition of GI,  $\text{O}_2$  and  $\text{N}_2\text{O}$  plasma treatments were carried out separately, under 200 W of power for 9 minutes at 200 °C, in the ALD reaction chamber. For the GI, a stack of 20 nm  $\text{AlO}_x$ /180 nm  $\text{SiN}_x$  was used. The  $\text{AlO}_x$  layer was deposited by T-ALD using  $\text{H}_2\text{O}$  as an oxygen source directly after the plasma treatment, without breaking the vacuum. To investigate the effect of the plasma treatment, reference TFTs were prepared, with the first GI deposited directly on top of the active layer by T-ALD or PE-ALD, using  $\text{H}_2\text{O}$  and  $\text{O}_2$  plasma as oxygen sources, respectively, without any further plasma treatment. The  $\text{AlO}_x$  was deposited with a trimethylaluminum (TMA) precursor as an Al source at 200 °C. As the second GI, a thick layer of  $\text{SiN}_x$  was deposited by PECVD. Silane ( $\text{SiH}_4$ ), ammonia ( $\text{NH}_3$ ) and hydrogen gas were

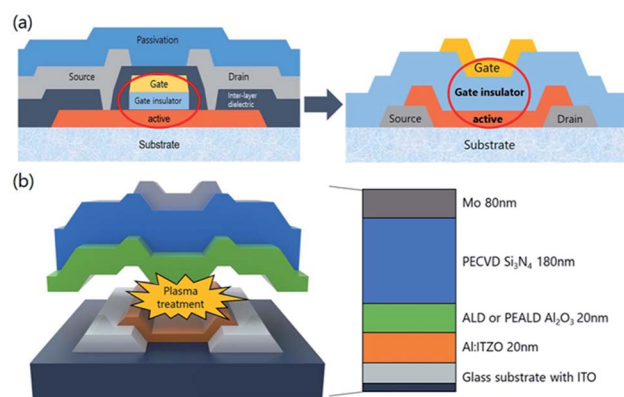


Fig. 1 (a) Schematic diagram of self-aligned structured TFT and top-gate bottom-contact structured TFT which have same stack sequence of active/GI/gate and (b) structure of high mobility TFT with the different condition of GI deposition process.

used as reaction elements for the  $\text{SiN}_x$  deposition. Finally, molybdenum was deposited as the gate electrode. A schematic diagram of the fabricated oxide TFT is shown in Fig. 1(b). The fabricated TFTs were annealed at 300 °C under vacuum conditions. The transfer and output characteristics of the TFTs were measured in an ambient environment. To investigate the origin of the differences between the TFTs, we analyzed them using SIMS and XPS.

## Results and discussions

The transfer characteristics of the top-gate bottom-contact TFTs with various types of GI deposition were investigated. Fig. 2(a) and (b) show the transfer characteristics of each TFT before and after thermal annealing under vacuum conditions, respectively (the overlapped transfer curves of six points for each sample, after thermal annealing, are shown in Fig. S1 in the ESI†). The applied  $V_d$  was 0.1 V and the TFTs were 40 and 20  $\mu\text{m}$  in width and length, respectively. Before the annealing process, the TFTs with GIs processed using thermal or PE-ALD, without any plasma treatment, exhibited conductive characteristics. However, on/off characteristics were exhibited when the GI was processed using ALD with  $\text{O}_2$  or  $\text{N}_2\text{O}$  plasma treatment. Both  $\text{O}_2$  and  $\text{N}_2\text{O}$  plasma-treated TFTs exhibited hysteresis, and the  $\text{O}_2$  plasma-treated sample exhibited a larger hysteresis value, of 14.5 V. Thermal annealing dramatically changed the characteristics of some of the TFTs. The TFT with GI processed by T-ALD without plasma treatment exhibited increased conductivity, whereas desirable TFT characteristics were obtained from the rest of the TFTs, as shown in Fig. 2(b). Furthermore, hysteresis was completely removed after thermal annealing, in the case of the TFT in which the first GI of  $\text{AlO}_x$  was deposited by T-ALD with plasma treatment. Direct deposition of a second GI, of  $\text{SiN}_x$ , on top of the high mobility oxide semiconductor would induce major incorporation of H into the adjacent active layer during post-thermal annealing according to several published

paper.<sup>30,31</sup> The deposition process would also increase the number of carriers in the oxide semiconductor and degrade the threshold voltage ( $V_{\text{th}}$ ). However, the ALD-processed thin  $\text{AlO}_x$ , as the first GI, acts as a good H barrier, resulting in devices with reasonable  $V_{\text{th}}$  characteristics even in the high mobility TFT.

The electrical characteristics, such as field-effect mobility ( $\mu_{\text{FE}}$ ), subthreshold swing (S.S) and  $V_{\text{th}}$ , were evaluated and are listed in Table 1 (a bar graph [with error bars] of the parameters is shown in Fig. S2 in the ESI†). The value of  $\mu_{\text{FE}}$  was calculated using the following equation:

$$\mu_{\text{FE}} = \frac{g_m}{\frac{W}{L} \times C_i \times V_d} \left( \text{where } g_m \equiv \frac{\partial I_d}{\partial V_g} \right)$$

where,  $W$  and  $L$  are the width and length of the channel, respectively.  $C_i$  is the capacitance of the GI; the measured value of the double-layered GI was approximately 3.1  $\text{pF m}^{-2}$ . As shown in the table, except for the device in which the GI was deposited with T-ALD without plasma treatment, all of the devices exhibited high mobility characteristics ( $>25 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ). In particular, the  $\text{N}_2\text{O}$  plasma-treated device exhibited degraded mobility characteristics. When the nitrogen from the  $\text{N}_2\text{O}$  plasma was incorporated into the active layer, it acted as a p-type dopant and reduced the n-type conductivity.<sup>32,33</sup> The drain current *versus*  $V_d$  characteristics of the devices were also investigated, and are illustrated in Fig. S3 of the ESI†. All of the devices exhibited typical output characteristics, with reasonable saturation behavior under various  $V_g$  conditions.

To investigate the origins of each of the TFT characteristics, we used the Hall measurement method to determine the carrier density of the active layers covered by each GI, which were processed as they would be in the devices. Fig. 3 shows the carrier concentration before and after thermal annealing. Notably, the carrier density of the active layer increased dramatically after thermal annealing when  $\text{AlO}_x$  was deposited using T-ALD without plasma treatment, up to  $1.6 \times 10^{20} \text{ cm}^{-3}$ ;

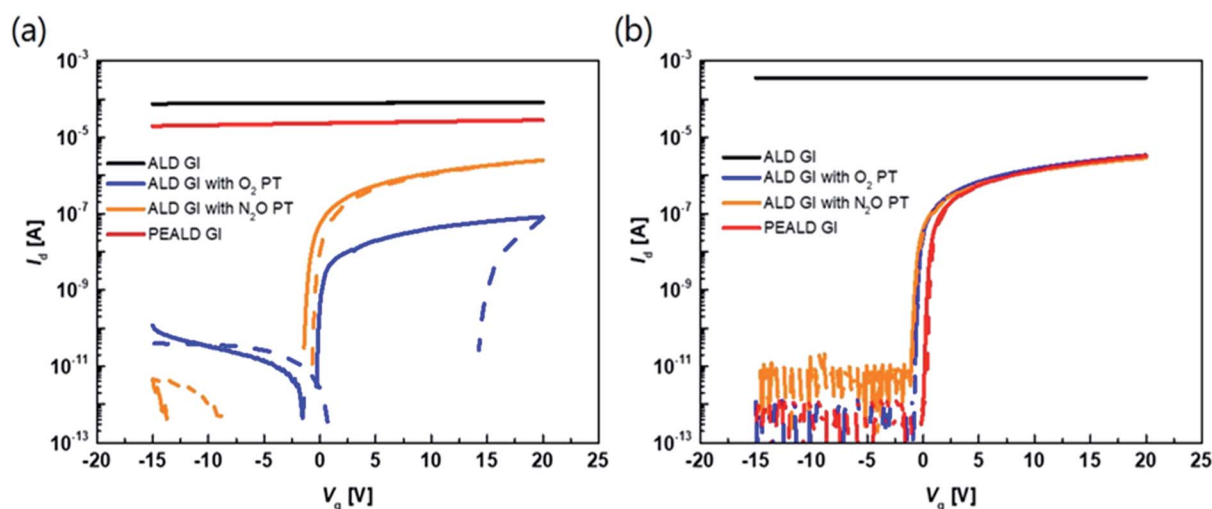
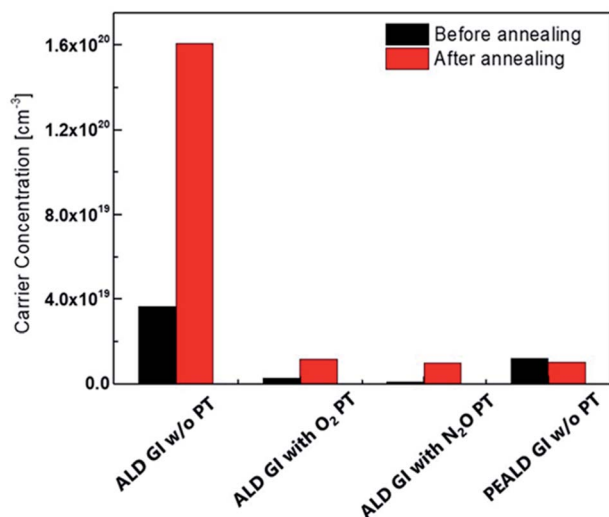


Fig. 2 Transfer curve of the TFT with different kinds of GI process with 0.1 V of drain voltage (a) before annealing and (b) after annealing at 300 °C under vacuum.

**Table 1** Electrical characteristics parameters of each device after thermal-annealing at 300 °C under vacuum

GI process condition	Field-effect mobility (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	Subthreshold-swing (V dec <sup>-1</sup> )	Threshold voltage (V)
ALD GI without PT	NA	NA	NA
PEALD GI without PT	33.2	0.10	3.06
ALD GI with O <sub>2</sub> PT	35.3	0.12	2.08
ALD GI with N <sub>2</sub> O PT	26.8	0.19	2.34



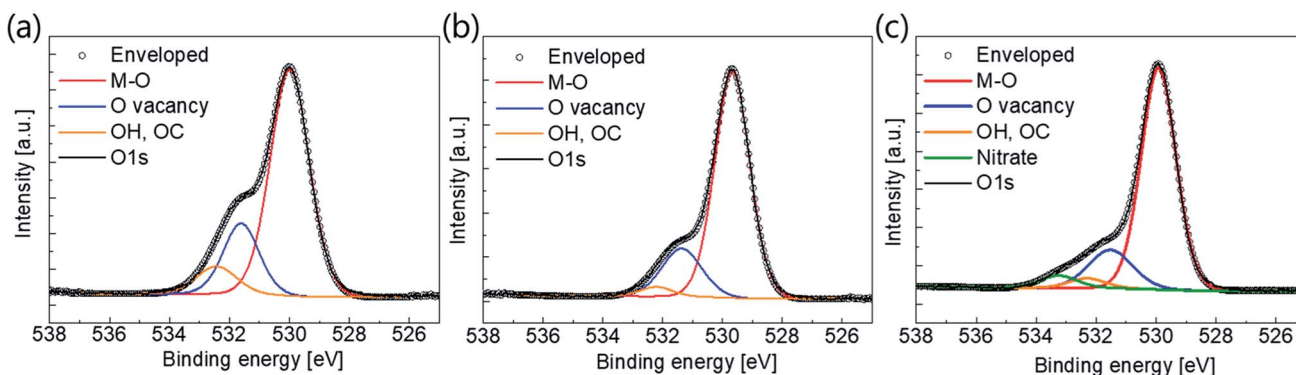
**Fig. 3** The carrier concentration of the active layer with each GI before and after thermal-annealing.

this value is too high to exhibit on/off characteristics. It is well known that a certain amount of H in the channel region acts as a donor by ionizing the H or bonding with oxygen and forming -OH.<sup>31,34,35</sup> Therefore, the increase in carrier density after thermal-annealing is caused by H diffusion from the AlO<sub>x</sub> to the active layer. However, a significant increase in the carrier density of the high-mobility oxide semiconductor was not observed when the plasma treatment was carried out directly

before the deposition of AlO<sub>x</sub> by T-ALD. After the annealing, these samples had similar carrier density, of  $1.0 \times 10^{19} \text{ cm}^{-3}$ , to that of the active layer covered by PE-ALD processed AlO<sub>x</sub>. According to Park *et al.*, while the degree of the negative shift in  $V_{th}$  caused by donor incorporation, for example H and O vacancy, may be mild in the case of TFTs with oxide semiconductors of low to moderate carrier density, such as InGaZnO, the doping effect becomes significant when the intrinsic carrier density of the oxide semiconductor is high.<sup>36</sup> As shown in Fig. 3, relatively low carrier concentrations were observed when the plasma treatment was performed prior to GI deposition; we observed a mild increase in carrier concentration due to the additional H doping effect. Therefore, TFTs with GIs deposited by T-ALD on active layers treated by O<sub>2</sub> and N<sub>2</sub>O plasma can exhibit reasonable on/off characteristics.

XPS analysis was carried out to investigate the effects of plasma treatment on the active surface composition and bonding states. We scrutinized the O 1s peaks because the electrical characteristics of oxide semiconductors are strongly related to their oxygen bonding states. The O 1s peaks near 530 eV were measured and de-convoluted with M-O, O vacancies and -OC or -OH bonding, as shown in Fig. 4. It is well known that the binding energies of O vacancies, and -OC and -OH bonds, are relatively large compared to M-O bonds.<sup>37-39</sup> From the graph, we can easily see that the amounts of O vacancies, and -OC and -OH bond, decreased dramatically after the plasma treatment. The atomic ratios of the bonding states are summarized in Table 2. The atomic ratio of M-O bonding was approximately 70% before the plasma treatment, increasing to 80% thereafter.

Furthermore, the atomic ratio of O vacancy decreased from 21.6% to 16.8 or 13.4%, depending on the plasma source. The degree of -OC and -OH bonding also decreased. It is well known that O vacancy acts as shallow donors. Therefore, oxygen-containing plasma treatment results in suppression of the intrinsic carrier density. These results are in good agreement with the previously described carrier concentration results. Furthermore, a nitrate peak with a binding energy of 533.2 eV was also detected in the active sample with N<sub>2</sub>O plasma treatment<sup>40</sup> (N 1s XPS peaks are also shown in Fig. S4 in the ESI†). Nitrogen incorporation can occur during N<sub>2</sub>O plasma

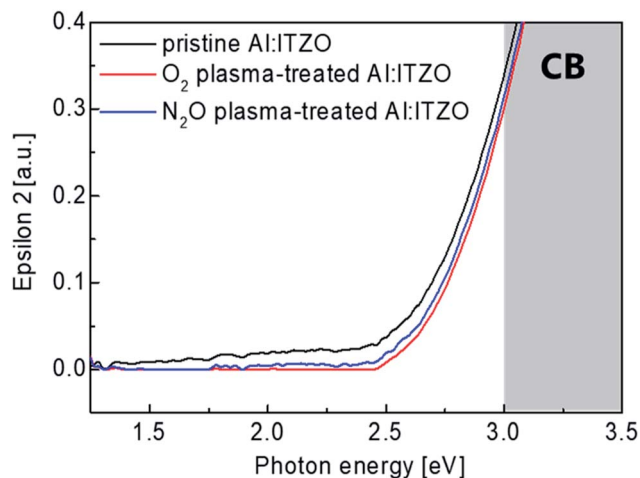


**Fig. 4** O 1s peaks and de-convoluted peaks from XPS results of (a) pristine active layer, (b) O<sub>2</sub> plasma-treated active, and (c) N<sub>2</sub>O plasma treated active.



**Table 2** The quantitative value of the atomic percent oxygen bonding state in the active layer before and after plasma treatment

Active state	O–M (at%)	V <sub>o</sub> (at%)	OH, OC (at%)	Nitrate (at%)
Pristine active	70.0	21.6	8.4	—
O <sub>2</sub> plasma treated	80.0	16.8	3.2	—
N <sub>2</sub> O plasma treated	78.7	13.4	3.2	4.7

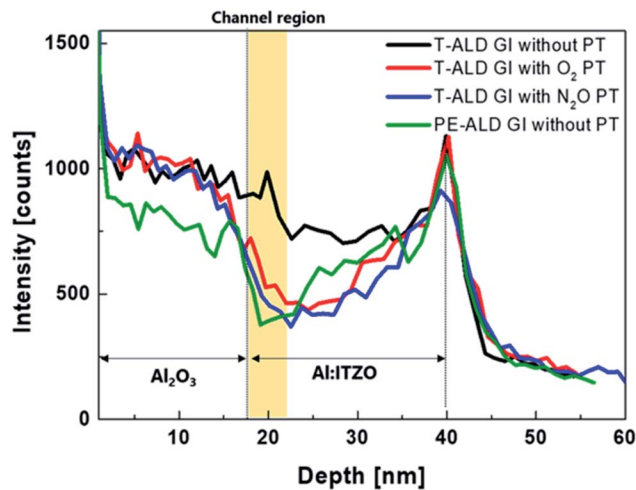


**Fig. 5** Imaginary dielectric function ( $\epsilon_2$ ) spectra of the Al doped ITZO films with and without O<sub>2</sub> or N<sub>2</sub>O plasma treatment.

treatment; this causes a reduction in the n-type conductivity,<sup>32,33</sup> resulting in mobility degradation of the TFT.

The effect of O<sub>2</sub> or N<sub>2</sub>O plasma treatment on the electronic structure of the active films was analyzed using a spectroscopic ellipsometer (SE). The imaginary dielectric-function ( $\epsilon_2$ ) versus photon energy spectra of the Al doped ITZO films with and without O<sub>2</sub> or N<sub>2</sub>O plasma treatment was shown in Fig. 5. These spectra were extracted from a two-phase model, which is composed of a Si substrate and Al doped ITZO layer. The  $\epsilon_2$  values near the conduction band minimum (CBM) correlated with the electrical characteristics of the devices.<sup>41,42</sup> As shown in the graph, it can be easily noticed that the sub-gap state near CBM was reduced in the Al doped ITZO films by O<sub>2</sub> and N<sub>2</sub>O plasma treatment. Therefore, it can be inferred that the O<sub>2</sub> and N<sub>2</sub>O plasma treatment effectively reduced charge trap sites especially oxygen vacancies.<sup>43</sup> This result is well matched with the XPS analysis results. Also, the  $\epsilon_2$  just below the CBM is related to the carrier concentration.<sup>44</sup> Therefore, decreased  $\epsilon_2$  near the CBM after O<sub>2</sub> and N<sub>2</sub>O plasma treatment indicates the reduction of the free carrier concentration of the Al doped ITZO film after O<sub>2</sub> and N<sub>2</sub>O plasma treatment which is correlated with Hall measurement results in Fig. 3. From the SE results, it can be referred that O<sub>2</sub> and N<sub>2</sub>O plasma treatment reduce the oxygen vacancies in the oxide semiconductor effectively to yield improved transfer characteristics as shown in Fig. 2.

The depth profile of the H of a film with the same stack sequence as a fabricated top-gate bottom-contact device was



**Fig. 6** Depth profile of hydrogen element in stacked films with different kinds of GI process after thermal-annealing.

investigated using SIMS measurements. Fig. 6 shows the depth profiles of H after thermal annealing. The H composition varied significantly between the samples. As expected, the larger amount of H was detected in GI with T-ALD than PE-ALD due to H<sub>2</sub>O reactant. H inside oxide semiconductors acts as a shallow donor to increase the carrier concentration.<sup>31,34,35</sup> The film stack sample deposited using T-ALD without plasma treatment contained the largest amount of H in channel region, which explains why the device exhibited conductive characteristics. In contrast, when the plasma treatment was performed prior to the T-ALD process, we observed a reduced amount of H in the channel region. This difference of H amount in channel region can be explained with XPS results which shown in Fig. 4. Many studies have reported that H can introduce to O vacancy sites and act as donor.<sup>45,46</sup> As shown in Fig. 4(a), a large amount of O vacancy was observed in the oxide semiconductor without plasma treatment, and a large amount of H can incorporate to the O vacancy sites. On the other hand, in oxide semiconductors with O<sub>2</sub> or N<sub>2</sub>O plasma treatment, the O vacancy decrease significantly, and even oxygen interstitial (O<sub>i</sub>) may generated, which plays the role of a charge trap center.<sup>47</sup> The hysteresis characteristics of the TFTs before annealing and the reduced carrier concentrations of the active layers covered by ALD GI, with O<sub>2</sub> and N<sub>2</sub>O plasma treatment, support this possibility (see Fig. 2(a) and 3). Therefore, it can be said that the plasma treatment effectively reduces the O vacancy sites where H can induce, so that a smaller amount of H is detected in the SIMS results. When the GI was deposited by PE-ALD without plasma treatment, a moderate amount of H is distributed because, O<sub>2</sub> plasma is used as the oxygen source, not H<sub>2</sub>O during PE-ALD process. Therefore, the TFT exhibited good transfer characteristics, similar to the TFTs with GIs deposited by T-ALD directly after plasma treatment. This resulted in also a moderate carrier concentration in the oxide semiconductor covered by PE-ALD processed AlO<sub>x</sub>.

The biggest difference among devices was observed in terms of electrical stability. The transfer curves shown in Fig. 6 were

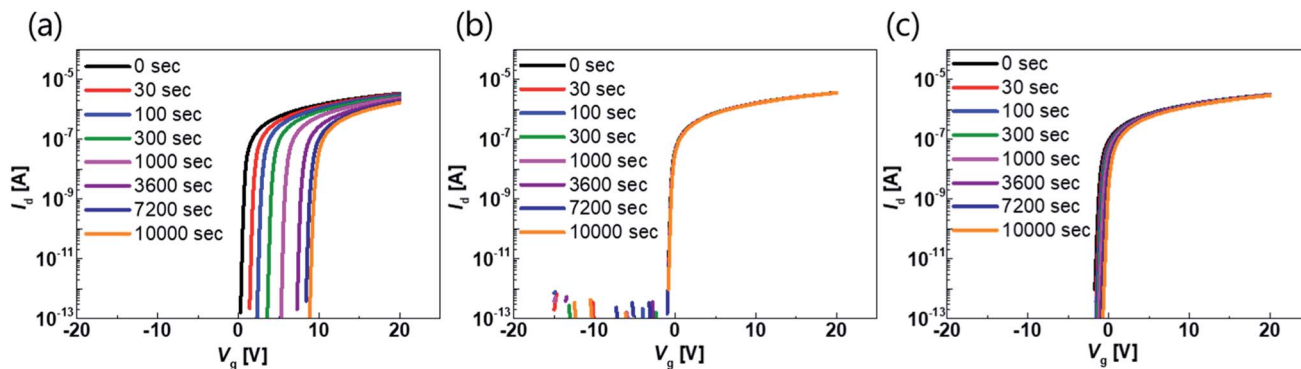


Fig. 7 Transfer curve during the PBTs environment of TFT of which alumina first GI was deposited by (a) PEALD without plasma treatment, (b)  $O_2$  plasma treatment followed by the thermal-ALD, and (c) with  $N_2O$  plasma treatment followed by thermal-ALD.

obtained under positive-bias temperature stress (PBTs) conditions. The gate bias and temperature were 20 V ( $1 \text{ MV cm}^{-1}$ ) and  $60^\circ\text{C}$ , respectively. The transfer curve shifted significantly in the positive direction when the GI of a given device was deposited using PE-ALD without plasma treatment, as shown in Fig. 7(a). However, when the GI was deposited using T-ALD with plasma treatment, the stability of the device improved significantly. In particular, the device with  $O_2$  plasma treatment exhibited outstanding PBTs stability characteristics, shifting by only 0.23 V after 10 000 s. The transfer curves of the devices with GIs deposited by PE-ALD without plasma treatment, and of GIs deposited by T-ALD with  $N_2O$  plasma treatment, shifted by 7.49 and 1.23 V, respectively. The variation in  $V_{th}$  during the PBTs is shown in Fig. S5 in the ESI.† The transfer curve of the TFT with GIs processed by PE-ALD shifted significantly during PBTs, without any degradation in the S.S value and no hump generation. This indicates that negative charges are either trapped at the GI and active interface or injected into the GI.<sup>24</sup> All of the devices experienced plasma damage during the GI deposition or plasma treatment, and only the plasma-treated devices with GI deposited by T-ALD exhibited high reliability. This was due to defect passivation by H during the T-ALD process and post-thermal annealing. Excessive H renders the oxide TFT conductive, but a moderate amount is beneficial for passivating trap sites at the active and GI interface.<sup>24–29</sup> Several cycles of the initial T-ALD  $AlO_x$  process using a  $H_2O$  source provide H to passivate the defects generated during  $O_2$  or  $N_2O$  plasma treatment. However, successive incorporation of H can be suppressed by the H barrier constituted by ALD- $AlO_x$  itself. The optimized plasma treatment time and T-ALD process temperature can match the degree of defect generation and passivation, which provides excellent electrical performance by minimizing the density of defects at the interface. When PE-ALD is used for GI deposition, the amount of H is insufficient to passivate the defects at the interface,<sup>48</sup> so it is difficult to ensure reliability of the device.

We also investigated the decay in drain current during the on-state bias, where current decay during operation leads to variation in the brightness of current-driven displays, such as OLEDs and LEDs. The normalized change in the amount of

drain current was measured under a bias of  $V_d = 5.5 \text{ V}$  and  $V_g = 5 \text{ V}$ , which corresponds to a saturation region. As shown in Fig. 7, the drain current decreases under on-bias due to screening of the gate bias by trapped charges. The on-current decay curves can be fitted with a stretched exponential equation:

$$\frac{I_D(t)}{I_D(0)} = \exp\left[-\left(\frac{t}{\tau}\right)^\beta\right]$$

where  $I_D(0)$  indicates the initial state of the drain current ( $t = 0$ ).  $\beta$  is the dispersion parameter, which is related to the trap distribution, and  $\tau$  is the characteristic time for trapping of the carriers.<sup>45–48</sup> The red lines in Fig. 8 indicate the fitting results obtained using the above equation; they agreed well with our experimental results. The  $\tau$  and  $\beta$  parameters were extracted from the fitted curve and are summarized in Table 3. The  $\tau$  value for the TFTs with GI deposited by T-ALD ( $3.9 \times 10^{12} \text{ s}$  for  $O_2$  and  $2.7 \times 10^7 \text{ s}$  for  $N_2O$  plasma treatment) were several orders larger than the value for the TFT in which a GI was deposited by PE-ALD without plasma treatment ( $1.6 \times 10^5 \text{ s}$ ). Therefore, we can infer that the TFT with plasma treatment and GI deposited by T-ALD contains far fewer trap sites.<sup>49–52</sup>

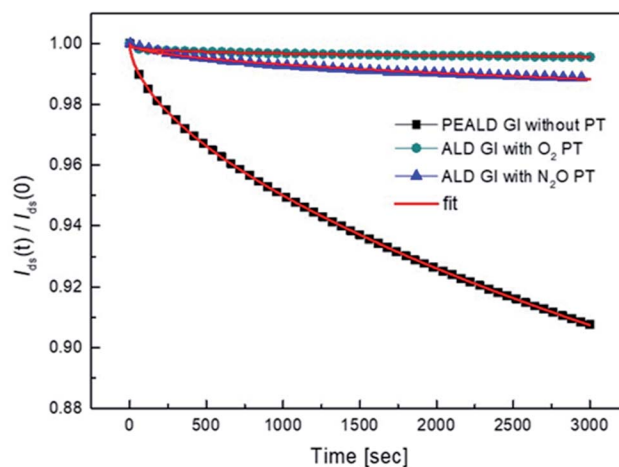
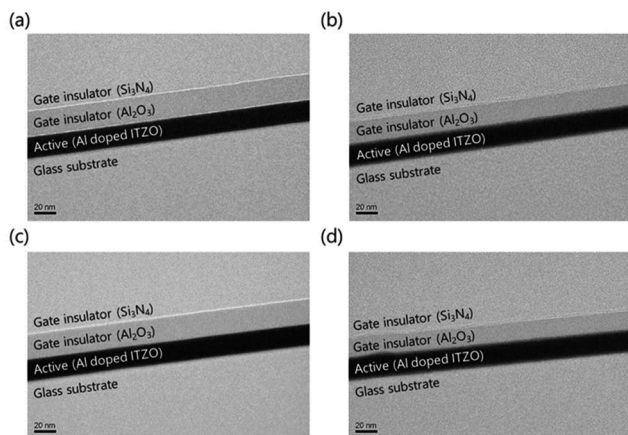


Fig. 8 The decay of the normalized drain current during the bias stress and fitted curve with stretched exponential equation.

**Table 3** The time for trapping of the carriers and dispersion parameters values of the TFTs with different kinds of GI processes

GI process condition	$\tau$ (s)	$\beta$
PEALD GI without PT	$1.6 \times 10^5$	0.58
ALD GI with O <sub>2</sub> PT	$3.9 \times 10^{12}$	0.26
ALD GI with N <sub>2</sub> O PT	$2.7 \times 10^7$	0.49



**Fig. 9** HRTEM images of a cross-section of the channel region in TFT that GI deposited by means of thermal-ALD (a) without plasma treatment, (b) with O<sub>2</sub> plasma treatment and (c) N<sub>2</sub>O plasma-treatment. (d) Is cross-section of the TFT that GI deposited by using PE-ALD without plasma treatment.

High-resolution transmission electron microscopy (HRTEM) images of the cross-sections of the active layer/GI stacks in TFTs indicate that the O<sub>2</sub> and N<sub>2</sub>O plasma treatments did not affect the surfaces of the active layers. Fig. 9(a) and (d) show cross-sectional HRTEM images of the channel regions of TFTs with GIs deposited by T-ALD, and by PE-ALD without plasma treatment, respectively. The HRTEM images of the O<sub>2</sub> and N<sub>2</sub>O plasma-treated TFTs are shown in Fig. 9(b) and (c), respectively. There were no significant differences in HRTEM results among the samples. In particular, on scrutinizing the interfaces between the active layers and GIs, the plasma-treated samples contained no crystallized regions, similar to the samples without plasma treatment. It is well known that polycrystalline oxide semiconductors show degraded electrical characteristics, such as low mobility and instability due to grain boundaries.<sup>53</sup> The plasma treatment did not provide sufficient energy to allow the active surfaces to crystallize, and there was no change in the phase. Therefore, plasma-treated TFTs maintain their outstanding electrical characteristics.

## Conclusions

High-mobility oxide TFTs with Cu electrodes are promising devices for realizing high-end, large-area displays, such as AMOLEDs and AMLEDs, due to their low RC delay characteristics. SiN<sub>x</sub> is a suitable candidate for GIs due to its good Cu diffusion barrier and high-*k* characteristics. To enable use of SiN<sub>x</sub> as the main GI, we applied a thin AlO<sub>x</sub> layer as the first GI,

which prevents incorporation of H during the SiN<sub>x</sub> deposition process, as well as the diffusion of H into the active layer during post-thermal annealing. To obtain good stability characteristics, T-ALD was used to deposit AlO<sub>x</sub> as the first GI. This process does not generate a reactive oxygen plasma source, thus suppressing the generation of charge trapping centers at the interface. To tailor the amounts of shallow H donors and ‘carrier-killer defects’ of interstitial oxygen in the active layer and/or interface, we used O<sub>2</sub> or N<sub>2</sub>O plasma treatment to yield TFTs with improved on/off characteristics. The TFTs subjected to O<sub>2</sub> and N<sub>2</sub>O plasma treatment had  $V_{th}$  values of 2.08 and 2.34 V, respectively. According to our XPS and SIMS results, both O<sub>2</sub> and N<sub>2</sub>O plasma treatment increased the amount of M–O bonding, and reduced the amount of donor elements caused by incorporation of H. The TFT with PE-ALD GIs also exhibited good on/off characteristics, even without any plasma treatment. The  $V_{th}$  of the TFT was approximately 3.06 V. The O<sub>2</sub> plasma-treated TFTs with T-ALD GIs exhibited high  $\mu_{FE}$  ( $>35.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ). Furthermore, the TFTs with T-ALD GIs treated by O-containing plasma exhibited improved bias stability compared to the TFT in which AlO<sub>x</sub>, the first GI, was deposited using PE-ALD. Therefore, we conclude that the T-ALD process for thin GI deposition can be applied to fabricate high-mobility top-gate structured oxide TFTs using O<sub>2</sub> or N<sub>2</sub>O plasma treatment. The AlO<sub>x</sub> deposited by T-ALD contains appropriate amounts of H, varying by the deposition temperature, and can passivate the extra trap sites generated during oxygen supply for the carrier control process of high-mobility oxide TFTs. Thus, high-mobility, high-stability TFTs can be obtained.

## Conflicts of interest

There are no conflicts to declare.

## Acknowledgements

This work was supported by Samsung Display Corporation through KAIST Samsung Display Research Center Program. Also, this work was supported by Wearable Platform Materials Technology Center (WMC) funded by the National Research Foundation of Korea (KRF) Grant by the Korean Government (MSIT) (No. 2016R1A5A1009926).

## References

- 1 J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee and J. M. Kim, *IEEE Electron Device Lett.*, 2008, **29**, 9–302.
- 2 T. Kamiya, K. Nomura and H. Hosono, *Sci. Technol. Adv. Mater.*, 2010, **11**, 044305.
- 3 J.-Y. Kwon, D.-J. Lee and K.-B. Kim, *Electron. Mater. Lett.*, 2011, **7**, 1–11.
- 4 J. S. Park, W.-J. Maeng, H.-S. Kim and J.-S. Park, *Thin Solid Films*, 2012, **520**, 1679–1693.
- 5 H.-H. Hsieh, H.-H. Lu, H. C. Ting, C.-S. Chuang, C.-Y. Chen and Y. Lin, *J. Inf. Disp.*, 2010, **11**, 160–164.

- 6 T. Wu, C.-W. Sher, Y. Lin, C.-F. Lee, S. Liang, Y. Lu, S.-W. H. Chen, W. Guo, H.-C. Kuo and Z. Chen, *Appl. Sci.*, 2018, **8**, 1–17.
- 7 J. B. Ko, H. I. Yeom and S.-H. K. Park, *IEEE Electron Device Lett.*, 2016, **37**, 39–42.
- 8 H.-I. Yeom, J. B. Ko, G. Mun and S.-H. K. Park, *J. Mater. Chem. C*, 2016, **4**, 6873–6880.
- 9 E. Lee, A. Benayad, T. Shin, H. Lee, D.-S. Ko, T. S. Kim, K. S. Son, M. Ryu, S. Jeon and G.-S. Park, *Sci. Rep.*, 2014, **4**, 4948.
- 10 S. H. Cho, J. B. Ko, M. K. Ryu, J.-H. Yang, H.-I. Yeom, S. K. Lim, C.-S. Hwang and S.-H. K. Park, *IEEE Trans. Electron Devices*, 2015, **62**, 3653–3657.
- 11 S. Hu, Z. Fang, H. Ning, R. Tao, X. Liu, Y. Zeng, R. Yao, F. Huang, Z. Li, M. Xu, L. Wang, L. Lan and J. Peng, *Materials*, 2016, **9**, 1–5.
- 12 S. H. Lee, D. J. Oh, A. Y. Hwang, D. S. Han, S. Kim, J. K. Jeong and J. W. Park, *IEEE Electron Device Lett.*, 2015, **36**, 802–804.
- 13 M. J. Powell, C. Glasse, P. W. Green, I. D. French and I. J. Stemp, *IEEE Electron Device Lett.*, 2000, **21**, 104–106.
- 14 K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, *Science*, 2003, **300**, 1269–1272.
- 15 H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, *Appl. Phys. Lett.*, 2006, **89**, 112123.
- 16 S.-H. K. Park, C.-S. Hwang, H. Y. Jeong, H. Y. Chu and K. I. Cho, *Electrochem. Solid-State Lett.*, 2008, **11**, H10–H14.
- 17 J.-S. Park, J. K. Jeong, Y.-G. Mo and S. Kim, *Appl. Phys. Lett.*, 2009, **94**, 042105.
- 18 Y. Kim, K.-H. Lee, G. Mun, K. Park and S.-H. K. Park, *Phys. Status Solidi A*, 2017, 1700183.
- 19 H. Miyazaki, H. Kojima and K. Hinode, *J. Appl. Phys.*, 1997, **12**, 7746–7750.
- 20 G. Dingemans, F. Einsele, W. Beyer, M. C. M. van de Sanden and W. M. M. Kessels, *Materials*, 2012, **111**, 093713.
- 21 L.-L. Zheng, S.-B. Qian, Y.-H. Wang and W.-J. Liu, *IEEE J. Electron Devices Soc.*, 2016, **4**, 347–352.
- 22 J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, X.-H. Zhang and B. Kippelen, *Appl. Phys. Lett.*, 2009, **94**, 142107.
- 23 M. S. Oh, K. Lee, J. H. Song, B. H. Lee, M. M. Sung, D. K. Hwang and S. Im, *J. Electrochem. Soc.*, 2008, **155**, H1009–H1014.
- 24 Y. Nam, H.-O. Kim, S. H. Cho and S.-H. K. Park, *RSC Adv.*, 2018, **8**, 5622–5628.
- 25 K. Nomura, T. Kamiya and H. Hosono, *ECS J. Solid State Sci. Technol.*, 2013, **2**, P5–P8.
- 26 Y. Nam, H.-O. Kim, S. H. Cho, C.-S. Hwang, T. Kim, S. Jeon and S.-H. K. Park, *J. Inf. Disp.*, 2016, **17**, 65–71.
- 27 Y. Hanyu, K. Domen, K. Nomura, H. Hiramatsu, H. Kumomi, H. Hosono and T. Kamiya, *Appl. Phys. Lett.*, 2013, **103**, 202114.
- 28 T. Kim, Y. Nam, J.-H. Hur, S.-H. K. Park and S. Jeon, *Nanotechnology*, 2016, **27**, 325203.
- 29 T. Kamiya and H. Hosono, *ECS Trans.*, 2013, **54**, 103–113.
- 30 J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang and H.-I. Kwon, *Appl. Phys. Lett.*, 2009, **94**, 222112.
- 31 K.-L. Han, K.-C. Ok, H.-S. Cho, S. Oh and J.-S. Park, *Appl. Phys. Lett.*, 2017, **111**, 063502.
- 32 S. J. Lim, J.-M. Kim, D. Kim, S. Kwon, J.-S. Park and H. Kim, *J. Electrochem. Soc.*, 2010, **157**, H214–H218.
- 33 B.-J. Kim, H.-J. Kim, S. M. Jung, T.-S. Yoon, Y.-S. Kim and H. H. Lee, *ECS Trans.*, 2010, **33**, 295–299.
- 34 C. G. Van De Walle, *Phys. Rev. Lett.*, 2000, **85**, 1012–1015.
- 35 H. J. Kim, S. Y. Park, H. Y. Jung, B. G. Son, C.-K. Lee, C.-K. Lee, J. H. Jeong, Y.-G. Mo, K. S. Son, M. K. Ryu, S. Lee and J. K. Jeong, *J. Phys. D: Appl. Phys.*, 2013, **46**, 055104.
- 36 S.-H. K. Park, M.-K. Ryu, H. Oh, C.-S. Hwang, J.-H. Jeon and S.-M. Yoon, *J. Vac. Sci. Technol., B: Nanotechnol. Microelectron.: Mater., Process., Meas., Phenom.*, 2013, **31**, 020601.
- 37 D.-G. Kim, S. Lee, D.-H. Kim, G.-H. Lee and M. Isshiki, *Thin Solid Films*, 2008, **516**, 2045–2049.
- 38 H. Henriquez, E. Munoz, E. A. Dalchiale, R. E. Marotti, F. Martin, D. Leinen, J. R. Ramos-Barrado and H. Gomez, *Phys. Status Solidi A*, 2013, **210**, 297–305.
- 39 P. K. Nayak, M. N. Hedhili, D. Cha and H. N. Alshareef, *Appl. Phys. Lett.*, 2013, **103**, 033518.
- 40 J. F. Moulder, W. F. Stickle, P. E. Sobol and K. D. Bomben, *Handbook of X-ray Photoelectron Spectroscopy*, ed. J. Chastain, Perkin-Elmer Corporation Physical Electronics Division: Eden Prairie, MN, 1992, ch. II, p. 45.
- 41 D.-G. Kim, J.-U. Kim, J.-S. Lee, K.-S. Park, Y.-G. Chang, M.-H. Kim and D.-K. Choi, *RSC Adv.*, 2019, **9**, 20865–20870.
- 42 B. D. Ahn, K.-B. Chung and J.-S. Park, *J. Electroceram.*, 2015, **34**, 229–235.
- 43 A. Song, H.-W. Park, K.-B. Chung, Y. S. Rim, K. S. Son, J. H. Lim and H. Y. Chu, *Appl. Phys. Lett.*, 2017, **111**, 243507.
- 44 S. Yoon, Y. J. Tak, D. H. Yoon, U. H. Choi, J.-S. Park, B. D. Ahn and H. J. Kim, *ACS Appl. Mater. Interfaces*, 2014, **6**, 13496–13501.
- 45 H.-K. Noh, J.-S. Park and K. J. Chang, *J. Appl. Phys.*, 2013, **113**, 063712.
- 46 Y. C. Park, J. G. Um, M. Mativenga and J. Jang, *ECS J. Solid State Sci. Technol.*, 2015, **4**, Q124–Q129.
- 47 J. Sheng, J. Park, D. W. Choi, J. Lim and J.-S. Park, *ACS Appl. Mater. Interfaces*, 2016, **8**, 31136–31143.
- 48 D.-H. Cho, S.-H. K. Park, S. Yang, C. Byun, K. I. Cho, M. Ryu, S. M. Chung, W.-S. Cheong, S. M. Yoon and C.-S. Hwang, *J. Inf. Disp.*, 2009, **10**, 137–142.
- 49 S. Singh and Y. N. Mohapatra, *Org. Electron.*, 2017, **51**, 128–136.
- 50 W. H. Lee, S. J. Lee, J. A. Lim and J. H. Cho, *RSC Adv.*, 2015, **5**, 78655–78659.
- 51 J.-M. Lee, I.-T. Cho, J.-H. Lee and H.-I. Kwon, *Appl. Phys. Lett.*, 2008, **93**, 093504.
- 52 X.-H. Zhang, S. P. Tiwari and B. Kippelen, *Org. Electron.*, 2009, **10**, 1133–1140.
- 53 T. Kamiya, K. Nomura and H. Hosono, *Sci. Technol. Adv. Mater.*, 2010, **11**, 1–23.