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Optics-Enabled Highly Scalable Inverter for Multi-Valued Logic

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The rapid advancements in machine learning have exacerbated the interconnect bottleneck inherent in binary logic-based computing architectures. An interesting approach to tackle this problem involves increasing the information density per interconnect, i.e., by switching from a two-valued to a multi-valued logic (MVL) architecture. However, current MVL implementations offer limited overall performance and face challenges in scaling to process data signals with radix (number of logic levels) even just above 3. In this work, a novel concept is introduced for implementation of a highly scalable and fully passive inverter based on the frequency-domain phase-only linear manipulation of the input MVL data signal, which is encoded in the amplitude variations of an electromagnetic wave along the time axis. As a key advantage, this solution is entirely independent of the input radix. The proposed design is implemented using an optical fibre Bragg grating device. Inversion of quaternary signals is experimentally demonstrated, as well as binary and ternary signals, at a remarkable operation speed of 32 GBaud, with an estimated energy consumption of ≈24 fJ/bit. The proposed method is universal and can be applied to any system that supports transmission and detection of coherent waves, such as microwave, plasmonic, mechanical, or quantum.

1. Introduction

Over the past few years, computing requirements have witnessed a six-fold increase, fueled by breakneck advancements in Artificial Intelligence (AI), cloud computing, augmented reality, and the Internet of Things (IoT).[1–5] These workloads require immense scalability while necessitating exceptional computational energy efficiency.[5] The relentless miniaturization of transistors coupled with technological process and material innovations have enabled the semiconductor industry to address the consumer needs for the past several decades.[6,7] However, to meet the performance demand of such data intensive tasks, electronics should overcome the interconnect bottleneck between logic units and memory.[1] Contrary to transistors, scaling of interconnects leads to larger parasitic capacitances and resistances, inducing large propagation delay and dynamic power dissipation.[8] A possible solution involves encoding more information per interconnect, i.e., by departing from traditional binary logic to a multi-valued logic (MVL) scheme.[9–11] Compared to binary logic, where all information is encoded in '0' and '1' bits, MVL logic supports additional intermediate states that exist between V_{DD} (1) and GND (0). For instance, by transitioning from binary (radix, $\mathfrak{R} = 2$) to ternary ($\mathfrak{R} = 3$) and quaternary ($\mathfrak{R} = 4$) logic, the system complexity, defined in terms of the number of interconnections, scales down to approximately 63% and 50%, respectively.[10] This reduction corresponds to a significant decrease in both the power consumption of the chip and the associated propagation delay or processing latency.[12] Furthermore, MVL has wide-reaching applications in fuzzy logic-assisted processing of linguistics, control system design, robotics, signal processing, medical services, and more.[13]

Despite the earliest theoretical reports on MVL algebra dating back to the 1920s[14] and some circuit-level implementations using binary transistors in the 1960s, the tremendous success of MOSFETs, as well as limited technological evolution in the synthesis of nanomaterials hindered the widespread development of MVL unit devices. In the last few years, this field has attracted considerable renewed interest with a focus toward realization of devices with stable, equiprobable, multiple quiescent (or operating) points using advanced emerging materials.[15–17] Most of the reported implementations to date are based on exploiting the negative differential transconductance (NDT) phenomenon

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in organic or 2-D heterojunction transistors.[18–22] Alternatively, devices utilizing the quantum confinement effects in embedded quantum dots[23] and single-electron transistors[24] have emerged as promising candidates. Notwithstanding this remarkable progress, most showcased demonstrations of MVL logic are based on the use of novel, sophisticated materials that either lack the technological maturity and the reliability of conventional CMOS-based binary transistors or necessitate impractical operating conditions.[17] Besides, in their attempts at realizing stable intermediate states in the voltage transfer characteristics (VTCs), these approaches pay a severe price in both speed and energy consumption by several orders of magnitude compared to their binary counterparts.[22] Consequently, these limitations severely restrict their practical utility in real-world applications. Moreover, to our knowledge, all MVL device realizations reported to date have been limited to operation on data signals with a maximum radix of 3, e.g., ternary inverters.[17] In fact, most of the proposed technology solutions cannot be scaled directly to quaternary or higher-valued logic systems without introducing significant, eventually unrealistic, complications to the involved device geometry or the manufacturing process. Nevertheless, the need for compatibility with binary signals necessitates the development of devices capable of processing MVL data signals with a power-of-2 radix, such as quaternary or even octonary signals,[11] resulting in simpler hardware circuits for radix conversion.[12,25]

We introduce and demonstrate a fundamentally distinct and universally applicable method called frequency-domain linear phase-only filtering. This innovative approach enables the realization of a fully passive and highly scalable MVL inverter. In the proposed scheme, the MVL data signals are encoded in the amplitude variation of an electromagnetic wave along the time domain. Compared to present solutions, which require stable multiple operating points, our method processes the entire input data signal at once by selectively imparting a $\pi-$ phase shift to the central or carrier frequency component of the encoded wave, enabling a radix-free operation. Hence, in principle, the same filtering device enables inverting an input MVL data signal with any given radix or number of logic levels. Interestingly, the inversion of $N-$ ary MVL signals through our proposed technique is analogous to the negation (NEG ¬) operator of the finite-valued Łukasiewicz logic family L_N.[26] In practice, the maximum achievable radix may be just limited by the capability to generate the data signals with the required number of logic levels. In previous work, passive logic circuits, including a NOT gate or inverter, have been proposed and demonstrated on binary signals using spectral linear phase filtering.[27,28] However, all this work has been strictly limited to the manipulation of standard binary data signals, i.e., signals with only two logic levels. Therefore, the possibility of applying the passive logic approach to process MVL signals has not been previously envisioned. Contrary to electronic transistors and other solutions, the energy consumption of a passive logic unit is determined by the practical insertion loss of the phase filtering device, whereas the maximum operating speed is limited only by the frequency bandwidth of the filter, allowing for simultaneous high-speed operation and low-energy consumption.

In this communication, we demonstrate the proposed concept using a light wave processing implementation. Specifically, the MVL data signals are modulated on a light wave, and the inverter is then implemented using an optical filtering solution, namely, a suitably designed optical fibre Bragg grating (FBG) device. Using this compact, integrated solution, we report the experimental realization of inversion of MVL data signals with different radices, i.e., with up to four logic levels. The demonstrated inverter offers a radix-independent performance, surpassing existing MVL implementations in terms of both speed and energy consumption by several orders of magnitude. Specifically, we demonstrate inversion of binary, ternary, and quaternary signals at an ultrafast symbol/baud rate of 32 Gigabaud (GBd), and with an estimated energy consumption as low as ≈ 24 fJ/bit. The potential of this same device to perform inversion of data signals with a higher radix, such as on octonary signals, has been also numerically validated.

2. Design Principle

The basic operation principle of our proposed inverter relies on encoding the data bits of an input MVL signal as different levels of amplitude of a light wave (i.e., with different logic levels being equidistant in amplitude). This is a well-known data modulation format in present telecommunication systems, referred to as pulse amplitude modulation (PAM). The frequency spectrum of the optically modulated MVL signal consists of a strong central or carrier spectral component, accompanied by the discrete and much-weaker spectral components corresponding to individual bit-by-bit transitions of the input data signal (see **Figure 1a**). It is important to note that the central frequency component represents the average value of the data signal in the time domain. By employing this technique, the individual bits of the input MVL sequence can be expressed as the sum of the average value of the entire data sequence and a constant additive factor that represents the corresponding bit value. Let us consider a quaternary sequence with amplitude levels of 0, 1, 2, and 3. In this case, the average value of the sequence is 1.5. The remaining factors for the bits 0, 1, 2, and 3 are −1.5, −0.5, +0.5, and +1.5, respectively. Our approach involves inverting the sign of these remaining factors while keeping the average value unchanged. This operation allows us to obtain the exact inverted bit at the output. For example, when the input is 0, the output is the average value (1.5) plus +1.5 (the inverse of the corresponding input factor, −1.5), resulting in a logic value of 3. This same inversion operation is applied to any input logic value, regardless of the number of logic levels involved. Conversely, inversion can be realized in the frequency domain by selectively applying a $\pi-$ phase shift over the central or carrier frequency component with respect to the continuous spectral components corresponding to the data bits, as shown in Figure 1a.

The intended function is typically implemented using an all-pass (phase-only) linear filter, a device that transmits all frequency components of an incoming wave while shifting the phase of some of the components relative to the others according to a prescribed profile. The equivalent relationship between amplitude values of the input MVL signal and its output-inverted counterpart can be mathematically expressed as: $a_{out} = 2a_{avg} - a_{in}$, where a_{in} and a_{out} are the respective amplitude values of the temporal data signals at the input and output, whereas a_{avg} denotes the average value of the data signal. Indeed, the input and output amplitude values of our proposed

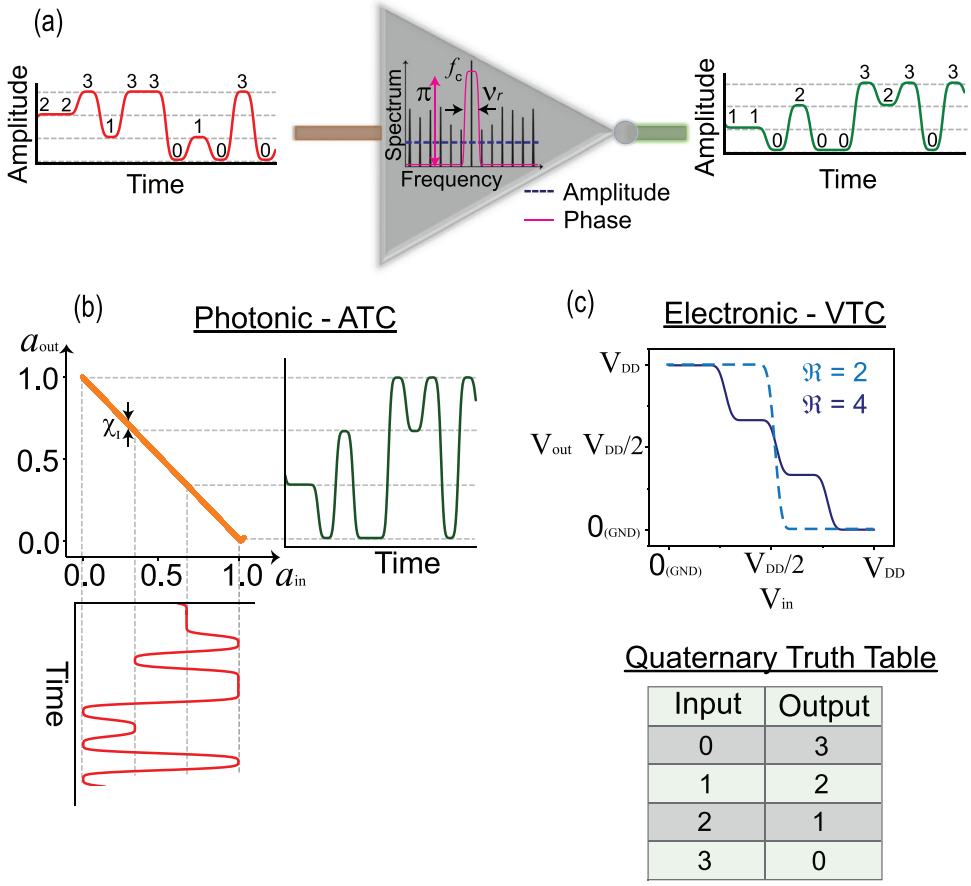

Figure 1. Operation principle of a fully-passive inverter for multi-valued logic (MVL) signals. a) A highly scalable inverter is implemented using an all-pass (phase-only) linear filter. The phase filter imparts a single π − phase shift with a frequency resolution (or the 3-dB bandwidth) of ν_r, over the carrier frequency component (f_c) with respect to the much weaker spectral components of the input MVL data signal, resulting in a bit-by-bit inversion at the output. This is schematically shown here for the case of a quaternary signal. This operation indeed follows the Boolean truth table of an inverter, shown below. b) The phase-only filtering scheme ensures a radix-free operation, as evident from the inverse one-to-one mapping between the input amplitude (a_{in}) and output amplitude (a_{out}), referred to as the amplitude transfer characteristic (ATC). The spread (χ_I) in the output amplitude values is inversely related to the ν_r of the phase filter. c) In comparison, the voltage transfer characteristics (VTCs) of the electronic-transistors is based upon the formation of stable intermediate states between GND and the voltage supply (V_{DD}), which in turn depend on the operation radix, shown here for the cases of binary (radix, $\mathfrak{R} = 2$) and quaternary ($\mathfrak{R} = 4$) signals.

inverter follow a one-to-one inverse relationship, see Figure 1b. Importantly, this relationship, defined as the amplitude transfer characteristic (ATC), remains independent of the input radix. This is in stark contrast to the VTC of traditional MVL inverters, wherein radix-dependent multiple stable operating points are required for inversion (Figure 1c). It is worth noting that the extent of variation (χ_I) in the output amplitude values of our proposed inverter is inversely proportional to the frequency resolution (ν_r) of the all-pass (phase-only) filter, which is defined as the 3-dB bandwidth of the π − phase shift. Consult Figure S1 (Supporting Information) for the related numerical simulations.

To highlight the outstanding potential and scalability of the proposed technique, we have carried out extensive numerical simulations aimed at the inversion of high-speed binary, ternary, quaternary, and octonary signals using an ideal all-pass (phase-only) filter. The filter amplitude response keeps the spectral content of the input signal unchanged, while the phase response exhibits a $(0 - \pi)$ phase shift with a Gaussian roll-off and a 3-dB bandwidth of 1 GHz. The input is a 63-bit long random bit sequence (RBS) at a baud rate of 50 GBd. Baud rate refers to the rate at which signal changes occur in a communication channel, typically measured in symbols per second. As observed from the temporal waveforms and related eye diagrams in **Figure 2**, for all the different MVL signals, distortion free bit-by-bit inversion is realized by a simple phase-only manipulation through the all-pass filter.

3. Experimental Results

The proposed concept is experimentally demonstrated using a light wave processing implementation. Specifically, the MVL data signals are encoded in the relative amplitude variations of a light wave, commonly known as optical PAM, see **Figure** 3a. This modulation strategy has been widely utilized in optical telecommunication systems to encode data signals with a prescribed number of logic levels (with demonstrations reporting up to 16 logic

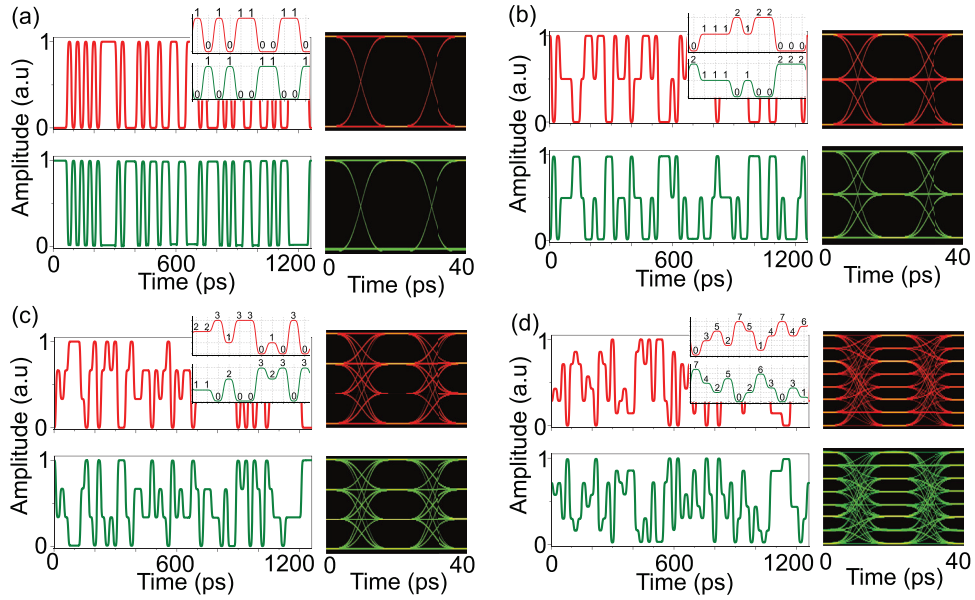

Figure 2. Numerical simulations related to inversion of high-speed MVL signals using a phase filter with frequency resolution, $v_r = 1$ GHz. The input consists of a 63 bits long random bit sequence (RBS) at a baud rate (f_s) of 50 GBd. (a, b, c, d) Temporal waveforms at the input (top) and the output (bottom) of the phase filter for binary, ternary, quaternary, and octonary signals, respectively. Inset shows the zoomed-in view of the bit-by-bit inversion. The corresponding eye diagrams (a folded representation of the temporal signal within a unit interval, given by the symbol duration time, $\Delta t_s = 1/f_s$) confirm the distortion-free inversion operation. Note that, for these simulations, an ideal signal generation and detection scheme is considered, i.e., with zero additional amplitude and phase noise.

levels.[29]) The optical MVL data signal is then processed using an optical all-pass (phase-only) filter. A fibre Bragg grating (FBG) is utilized to implement the required filter. An FBG is created through a well-designed quasi-periodic perturbation of the effective refractive index along the length of an optical fibre. This modification induces a user-defined coupling, known as the coupling coefficient, between a forward-propagating fibre mode and a backward-propagating one.[30] The resulting periodic structure functions as a wavelength-selective narrowband reflector, enabling multiple distributed reflections along each grating plane. These reflected signals undergo constructive interference within a narrowband centered around a particular wavelength, known as the Bragg wavelength. The main motivation behind the use of FBG lies in their remarkable versatility. By leveraging well-established synthesis and analysis techniques,[30,31] the linear spectral transfer function (in both amplitude and phase) of an FBG can be arbitrarily designed by tailoring the coupling coefficient profile along the length of the device, while operating

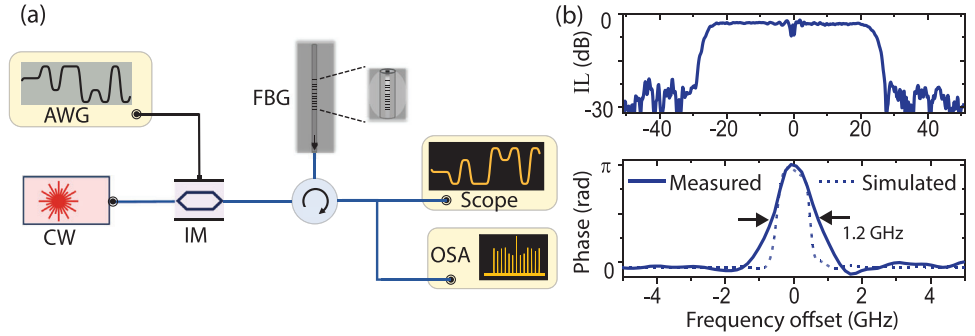

Figure 3. Schematic representation of the experimental setup and the measured response of the FBG-based phase filter. a) For the experimental demonstration, the varying logic levels are encoded in the relative amplitude modulation of a continuous-wave (CW) light source, referred to as PAM in optical telecommunication systems. The generation of input optical MVL data signals is achieved by utilizing an electro-optic intensity modulator (IM) coupled with an electronic arbitrary waveform generator (AWG). The resultant signal is coupled to the FBG using an optical circulator. The FBG inscription process involves utilizing a femtosecond laser-based plane-by-plane direct write technique, wherein the desired grating apodization is achieved by modulating the spacing between neighboring grating planes (refer to the inset). The temporal waveforms and the related spectra of the input and output MVL signals are captured using an optical sampling oscilloscope and an optical spectrum analyzer (OSA), respectively. Refer to Supporting Information for a detailed description of the experimental setup. b) The measured complex response of the FBG-based phase filter: Insertion loss (IL) (top) and the associated spectral phase response along the passband (bottom). The simulated phase response is denoted with a dashed trace. The passband of the device is centered at ≈ 1550 nm wavelength.

in reflection. The target specifications of the fabricated FBG are as follows: an amplitude spectral response with a nearly square shape, featuring a 3-dB BW of 50 GHz, and a peak intensity (or reflectivity) of 50% around the Bragg wavelength of ≈ 1550 nm. The corresponding spectral phase response exhibits a rectangular $(0 - \pi)$ phase shift, with a 3-dB BW or frequency resolution of 1 GHz. The latest represents an exceptional specification, surpassing the frequency resolution of a conventional optical waveshaper by more than tenfold.[32]

A femtosecond-laser based plane-by-plane direct writing scheme is used for the inscription of the designed FBG, wherein the required coupling coefficient profile is realized by modulating the spacing between adjacent grating planes, while maintaining a constant laser illumination power. A detailed description of the involved FBG design and fabrication process is provided in refs. [28, 33] The device length of the FBG is ≈ 21.3 cm. An optical vector analyzer is used to measure the complex (amplitude and phase) spectral response of the fabricated FBG, shown in Figure 3b. The measured spectral phase response matches with the simulated phase response, with the measured 3-dB BW of the π phase-shift of ≈ 1.2 GHz. The amplitude response exhibits a square roll-off with a peak reflectivity of ≈ 45%.

Figure 4a–c depicts the measured temporal waveforms of the 32-GBd 63-bit long RBS at the input (top) and the output (bottom) of the phase filter, along with the corresponding eye diagrams for binary, ternary, and quaternary signals, respectively. As evident from the measured eye diagrams, nearly distortion-free inversion is observed, even for quaternary signals. Note that the presented traces represent the optical intensity of the light waves. When the intensity modulator is biased at the quadrature point and the amplitude of the input electrical MVL signal is kept significantly smaller than the modulator's extinction voltage (V_π), both the electric field amplitude and the intensity (i.e., square of the amplitude) at the modulator output maintain a direct proportionality to the input RF signal.[34] A detailed description of the experimental setup and the related mathematical derivations are presented in Supporting Information. We emphasize that the observed inversion is solely due to frequency domain phase filtering of the carrier frequency component of the input signal achieved by using the compact FBG device, which enables a highly scalable and fully passive logic operation with simultaneous record high speed and low-energy consumption. The variation between the measured intensity values at the input and the output of the phase filter for different MVL signals is plotted in Figure 4d. This measured variation matches closely with the ATC of an ideal 1-GHz phase filter, considering an ideal intensity modulator with zero additional amplitude and phase noise. A slight nonlinear trend is observed between the output and input intensity values for input MVL signals with radix 3 and 4. This deviation is mainly attributed to the nonlinear transfer response of the intensity modulation device utilized in the experiments. To mitigate this variation, techniques such as cascaded Mach Zehnder modulators with complementary voltage signals[35] and adaptive pre-emphasis filters could be employed.[36] Furthermore, the non-ideal response of the intensity modulator results in intermodulation and harmonic distortion of the generated optical MVL signal,[37] which limited the operation to signals with radix up to 4 (quaternary). Yet, by utilizing the measured complex response of the FBG, we demonstrate the inversion of 32-GBd octonary (radix of 8) data signals through numerical simulations in Figure S3 (Supporting Information). It is worth highlighting that digital signal processing-based equalization techniques have been widely employed in fibre-optic telecommunication for generating high-speed MVL signals, with radices reaching up to 16.[29] The finite amplitude bandwidth (50 GHz) of the FBG creates a low-pass filtering effect on the input optical signal, thereby imposing a limit on the maximum operation speed of our inverter. On the other hand, the minimum speed is determined by noting that the π − phase shift should be applied solely to the carrier frequency component. This requirement translates to the frequency resolution, ν_r to be less than $2f_s/\mathrm{RBS}_{\mathrm{length}}$, where $\mathrm{RBS}_{\mathrm{length}}$ is the length of the input-RBS with baud rate, f_s.[28]

We further report polarization division multiplexing (PDM) of the inversion operation by exploiting the near-independent polarization response of the FBG-based phase filtering device. PDM is a well-known technique in fibre-optic communication systems, wherein two channels of information are simultaneously transmitted on the same carrier frequency by using two orthogonal polarization modes of the waveguiding medium, such as an optical fibre. This translates to doubling of the transmission capacity. For the application reported here, this strategy would enable using the same device for inversion of two different MVL data signals simultaneously, thus doubling the processing capability. The measured spectral response of the FBG filter for the two orthogonal polarization modes, i.e., transverse electric (TE) and transverse magnetic (TM), is shown in **Figure** 5a. The nearly identical amplitude and phase response of the device is evident, with a difference in the peak phase shift of < 0.5 rad.

Proof-of-concept experiments validate the simultaneous inversion of two independent 32-GBd binary data streams using the FBG, see Figure 5b, c. Notice that whereas data signals with the same radix and bit rate are used in this demonstration for experimental convenience, in general, the two signals to be simultaneously processed could exhibit a different radix and symbol rate. The performance of the FBG-based inverter is estimated by calculating the Q-factor from the measured eye diagrams of the input and output-inverted signals for the two polarization modes. The Q-factor is a metric that is widely used to estimate the quality of a digital binary signal, and this is calculated as the difference of the mean values of the two signal levels (a "0" and a "1" bit) divided by the sum of the noise standard deviations of the two levels.[38] The observed deviation in the Q-factor of the input and output signals is mainly attributed to the limited polarization extinction ratio of the polarization beam splitters used in the experiments, inducing polarization cross-talk at the output. Refer to Figure S4 (Supporting Information) for a detailed description of the experimental setup.

4. Discussion

The power consumption of the spectral phase-filtering based inverter is independent of the baud rate and the radix (or the complexity) of the input MVL signal, and is exclusively determined by the insertion loss of the FBG (−3.5 dB for the fabricated device). On the contrary, the power dissipation of electronic transistors scales proportionally with the input signal rate. Moreover, compared to their binary counterparts, most of the current MVL implementations operate at considerably

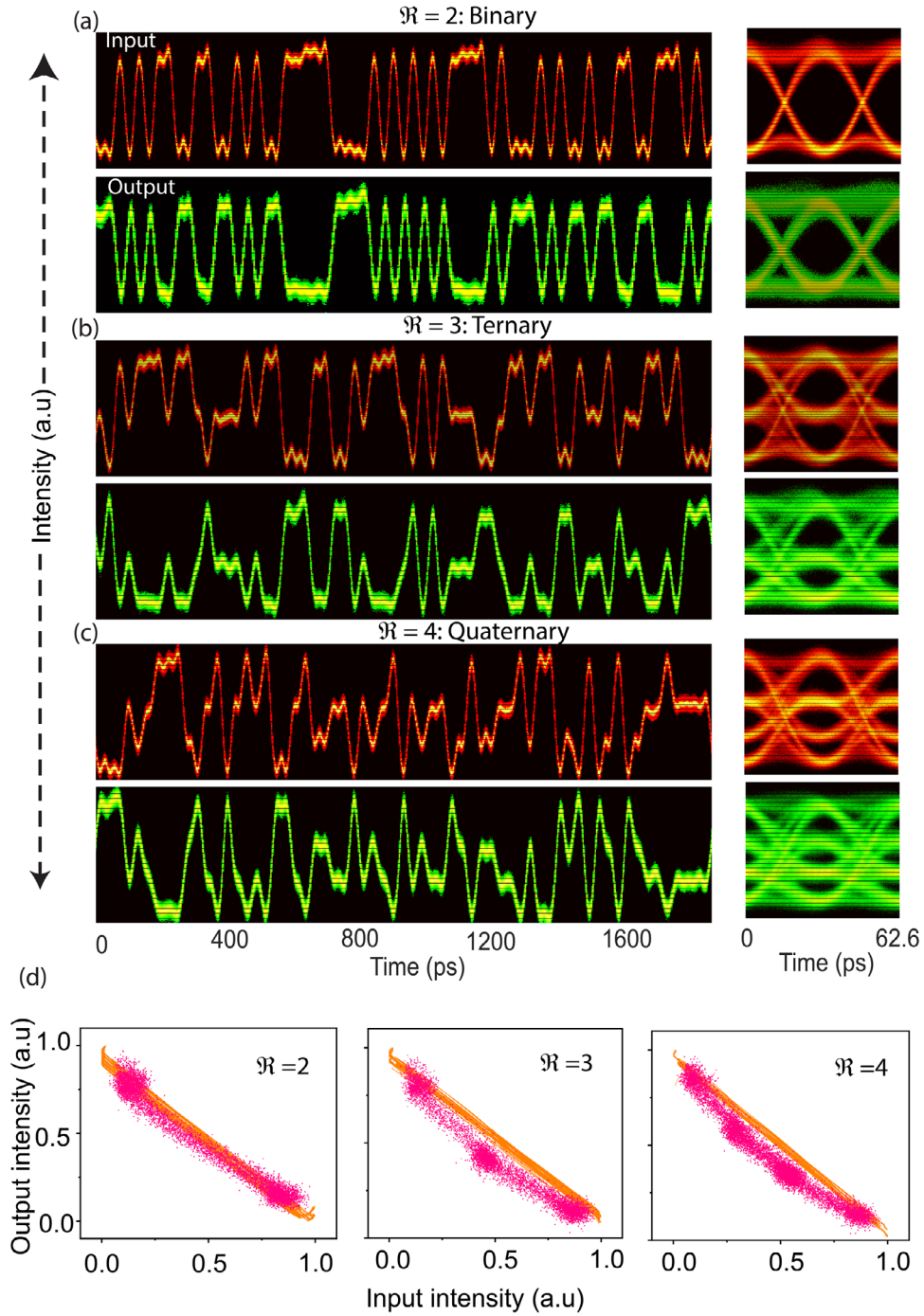

Figure 4. Experimental results. a–c) Measured temporal waveforms (instantaneous intensity) at the input (top) and the output (bottom) of the phase filter for binary, ternary, quaternary data signals, respectively. The corresponding eye diagrams of the input and output-inverted MVL signals are also presented. d) An inverse linear relationship is observed between the measured intensity values of the output and input optical signals for all three cases (plotted in magenta). The orange scatter plot represents the variation of numerically derived input and output amplitude, considering an ideal phase filter with zero additional amplitude and phase noise. It should be noted that in the experiments, the intensity modulator is operated within the small-signal limit to ensure that the intensity of the generated waveforms is directly proportional (within a constant bias) to the amplitude or magnitude of the electric field associated with the data signals. Further details can be found in Supporting Information.

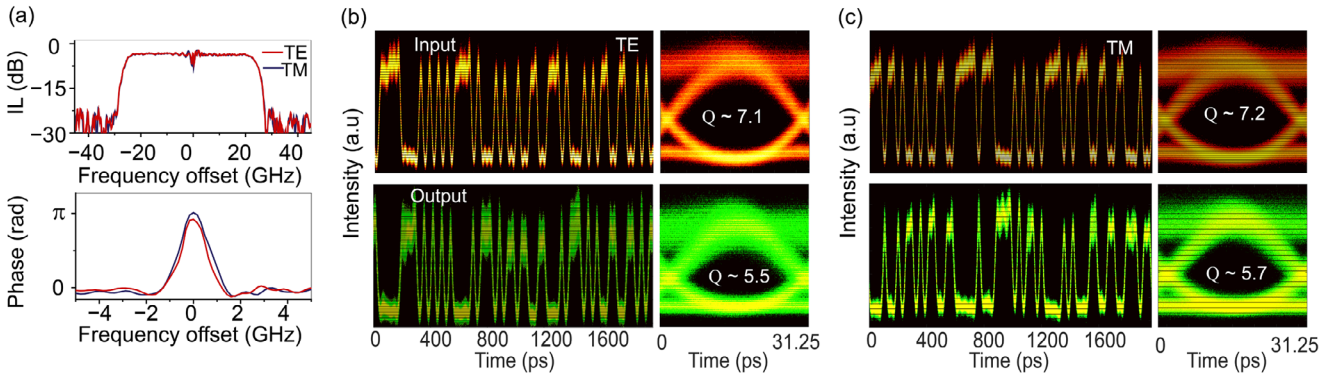

Figure 5. Experimental demonstration of polarization division multiplexing of the inversion operation using the FBG-based phase filter. a) Measured spectral amplitude and phase response of the FBG for the two orthogonal polarization modes: transverse electric (TE) and transverse magnetic (TM). The near-polarization independent response of the device is evident. Two independent 32-GBd binary data streams are simultaneously coupled into the FBG using polarization beam splitters. b, c) Measured temporal waveforms and eye diagrams of the two bit streams at the input (top) and the output (bottom) of the FBG, respectively. System-level evaluation of the FBG's performance is carried out by calculating the Q-factor metric from the measured eye diagrams of the input and output-inverted signals for both the bit streams. Q-factor is calculated as the difference of the mean values of the signal levels of the 0 and 1 bit divided by the sum of standard deviations of the two levels. The presented Q-factor values are estimated at a fixed average signal power of ≈ 5 dBm.

slower speeds,[22] require large operating voltages (up to 60 V in some systems,[39,40]) and in general, they are inherently inefficient from a power consumption standpoint.[22,39,41] The energy consumption of the passive inverter considering 32-GBd operation is estimated to be ≈ 48 fJ/bit for the binary signal, reducing to ≈ 32 fJ/bit and 24 fJ/bit for the ternary and quaternary signals, respectively. Refer to the detailed calculation of the energy consumption estimates in Supporting Information. We should note that the energy consumption of our proposed inverter is primarily constrained by the detection power threshold of the photoreceiver. By employing a more sensitive detector, it is feasible to lower the energy consumption to the sub-fJ/bit range.

It is crucial to emphasize that the single-channel all-pass (phase-only) response of the FBG can be duplicated across more than 45 successive multiple wavelength channels, with a desired channel spacing, using a simple loss-less phase-only sampling technique.[42,43] For instance, by simultaneously inverting 32-GBd quaternary data streams across 45 wavelength channels, with each channel employing polarization division multiplexing, we could potentially achieve a processing capacity in excess of 5.7 Tbps, thus unlocking the full potential of the photonics-based solution compared to electronics.

In terms of on-chip implementation, the design framework utilized to realize the in-fibre phase-only filter has been recently adopted to synthesize ultra-compact on-chip discrete phase filters using waveguide Bragg gratings (WBGs) designed in a spiral geometry.[44] As a result, we anticipate several orders of magnitude reduction in device footprint, from a few-cm^2 to sub-mm^2. The on-chip implementation holds particular significance for realizing phase-only filters with frequency resolution in the MHz range, given that FBG-based devices typically necessitate lengths nearing 1 meter (see Figure S5, Supporting Information). It is worth highlighting that integrated on-chip devices designed to realize an RF-photonic phase shifter functionality[45,46] could be potentially utilized to perform inversion of MVL data signals. However, to ensure distortion-free processing of data signals with speeds in the 10s of GBd range, such devices should exhibit a full $0-2\pi$ phase shift over a narrow spectral region of around 1 GHz and below. Meeting this specification in practical devices with minimal additional insertion losses remains a challenging task.

To summarize, we report the realization of a phase-only filtering based highly scalable inverter for high-speed multi-valued signals. In striking contrast to current MVL implementations in electronics, our approach translates to a radix-free operation, potentially enabling the processing of octonary signals and beyond. Through proof-of-concept experiments, we demonstrate inversion of 32-GBd binary, ternary, and quaternary signals using a compact fibre Bragg grating device, with energy consumption as low as ≈ 24 fJ/bit. This work reports the experimental demonstration of an energy-efficient inversion operation of a quaternary signal, while operating at speeds well beyond the reach of state-of-the-art techniques. With further development, designs combining the frequency domain phase filtering technique with linear interference could be potentially realized to implement other passive logic gates suitable for processing MVL signals. In a broader framework, the concept of phase-only filtering is a universal one and remains applicable to other physical domains that can transmit and detect coherent waves.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

fibre bragg gratings, multi-valued logic, optical computing, phase filters

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