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Bias-controlled multi-functional transport properties of InSe/BP van der Waals heterostructures

Sang-Hoo Cho¹, Hanbyeol Jang¹, Heungsoon Im¹, Donghyeon Lee¹, Je-Ho Lee², Kenji Watanabe³, Takashi Taniguchi³, Maeng-Je Seong², Byoung Hun Lee^{1,4} & Kayoung Lee^{1,5}✉

Van der Waals (vdW) heterostructures, consisting of a variety of low-dimensional materials, have great potential use in the design of a wide range of functional devices thanks to their atomically thin body and strong electrostatic tunability. Here, we demonstrate multi-functional indium selenide (InSe)/black phosphorous (BP) heterostructures encapsulated by hexagonal boron nitride. At a positive drain bias (V_D), applied on the BP while the InSe is grounded, our heterostructures show an intermediate gate voltage (V_{BG}) regime where the current hardly changes, working as a ternary transistor. By contrast, at a negative V_D , the device shows strong negative differential transconductance characteristics; the peak current increases up to $-5 \mu\text{A}$ and the peak-to-valley current ratio reaches 1600 at $V_D = -2 \text{V}$. Four-terminal measurements were performed on each layer, allowing us to separate the contributions of contact resistances and channel resistance. Moreover, multiple devices with different device structures and contacts were investigated, providing insight into the operation principle and performance optimization. We systematically investigated the influence of contact resistances, heterojunction resistance, channel resistance, and the thickness of BP on the detailed operational characteristics at different V_D and V_{BG} regimes.

Heterogeneous electron systems consisting of van der Waals (vdW) materials have recently been receiving elevated attention, accompanied by the remarkable development of fabrication techniques^{1–3}. The wide range of two-dimensional (2D) semiconductors with different band structure parameters presents the possibility of creating various band-edge alignments, depending on the desired device functionality. The absence of dangling bonds on the surfaces of 2D materials allows for high-quality heterointerfaces with minimal trap sites, regardless of lattice mismatch, and their atomically thin bodies render the band alignment properties and doping levels widely controllable by applying external electric fields^{4,5}. vdW heterostructures, therefore, have revealed promise for advanced data processing electronics, including gate-tunable negative differential resistance, negative differential transconductance (NDT), and multi-value logic (MVL) operating devices^{4–9}. For instance, Huang et al.⁵ demonstrated the multifunctionality of BP/MoS₂ heterostructures, i.e. rectification, high on/off ratio, NDT, and ternary and binary logics. In-plane and interlayer tunneling electronics have also been realized based on various assemblies of low-dimensional semiconductors^{6–12}.

NDT is a characteristic in which an increase in gate voltage results in a decrease in drain current; the so-called anti-ambipolar characteristic, one type of NDT, refers to a situation in which current is generated in the middle gate voltage region but is not generated at both positively and negatively large gate voltages^{4,13}. Various heterostructures consisting of multiple different semiconductors have been shown to have NDT characteristics, including MoS₂/single-walled carbon nanotubes⁴, MoS₂/WSe₂^{6,13}, MoS₂/MoTe₂^{14–16}, MoS₂/BP⁵, ReS₂/BP¹⁷, SnS₂/WSe₂¹⁸, MoS₂/rubrene¹⁹, InSe/BP²⁰, and heterostructures composed of *n*-type and *p*-type organic semiconductors^{21,22}. A strong anti-ambipolar behavior can be employed for multi-way switching¹³. NDT devices also have potential use as oscillators, memories, and other low power logics^{23,24}.

¹School of Materials Science and Engineering, Gwangju Institute of Science and Technology (GIST), 123 Cheomdangwagi-ro, Buk-gu, Gwangju 61005, Republic of Korea. ²Department of Physics, Chung-Ang University, Seoul 06974, Republic of Korea. ³National Institute for Materials Science, 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan. ⁴Center for Semiconductor Technology Convergence (CSTC), Electrical Engineering, Pohang University of Science and Technology (POSTECH), 77 Cheongam-ro, Nam-gu, Pohang, Gyeongbuk 37673, Republic of Korea. ⁵School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea. ✉email: kayoung.lee@kaist.ac.kr

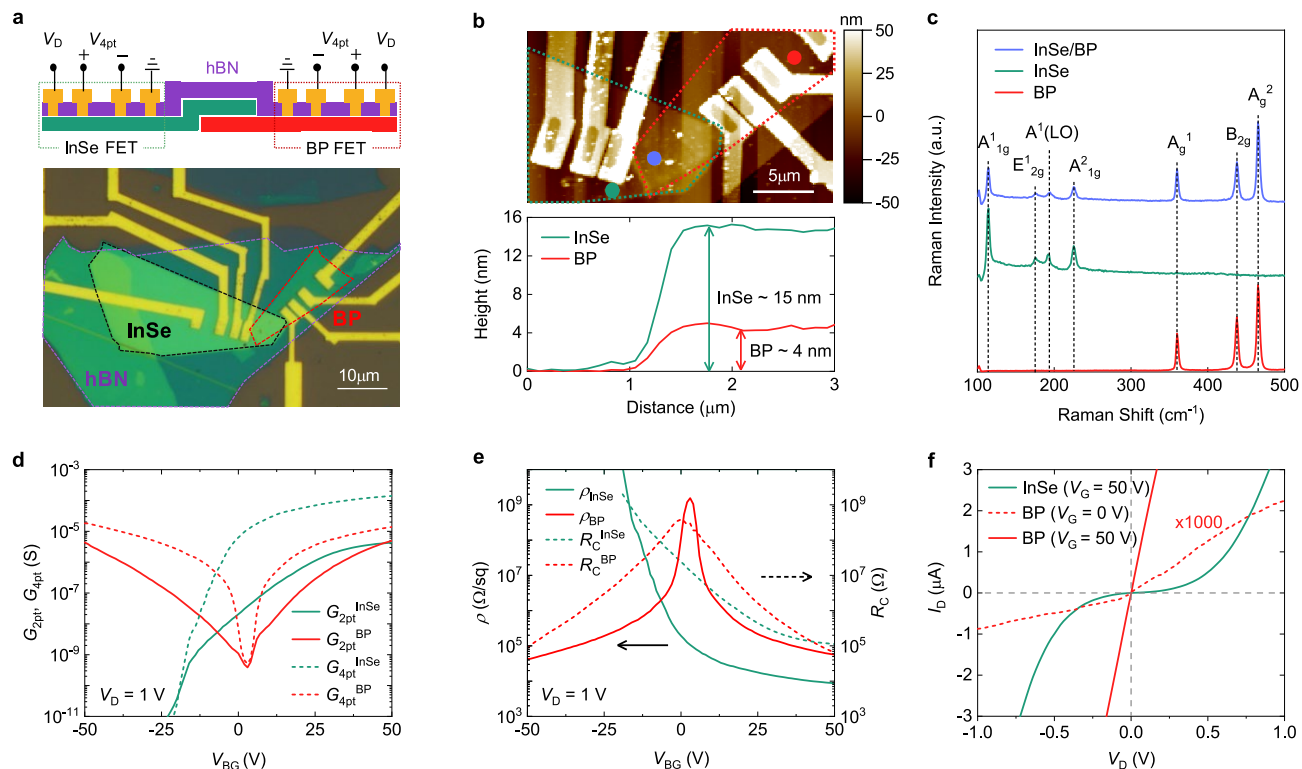


Figure 1. (a) Device schematic and optical micrograph of the InSe-BP-Ti device. The black, red, and purple dashed lines represent the InSe, BP, and hBN, respectively (lower micrograph). (b) Atomic force microscopic image of the device (upper) and the line profiles showing the thicknesses of the InSe and BP flakes (lower). (c) Raman spectra of the InSe/BP overlap region (blue), InSe region (green), and BP (red) region. (d) G_{2pt}^{InSe} , G_{2pt}^{BP} , G_{4pt}^{InSe} , and G_{4pt}^{BP} measured via the four-terminal methodology as a function of V_{BG} at $V_D = 1$ V. (e) R_C^{InSe} , R_C^{BP} , ρ_{InSe} , and ρ_{BP} extracted from (d) data. (f) I_D vs V_D of the InSe at $V_{BG} = 50$ V and that of the BP at $V_{BG} = 0$ and 50 V, showing the Schottky behavior of the Au/Ti contacts on the InSe and the ohmic characteristic of the contacts on the BP.

In this article, we present bias-controlled NDT and ternary *transistors* based on InSe/BP heterostructures encapsulated by hexagonal boron nitride (hBN). BP and InSe have mobilities notably superior than those of transition metal dichalcogenides^{25,26}. They have relatively small effective masses, and the InSe conduction band and the BP valence band are close each other. The combination of InSe and BP could be, thus, promising for high-speed tunneling based devices. Several studies have demonstrated ternary *inverters* by using a NDT device and the part of the constituent semiconductor of the NDT device as a load resistor^{5,6,14,22,27,28}. However, such approach is limited to inverting logics and cannot provide a versatile complementary metal–oxide–semiconductor (CMOS) circuit design strategy. Ternary *transistors*, where the drain current hardly changes within a specific gate voltage range (an intermediate logic state), are more essential to implement practical ternary-data-processing CMOS integrated circuits²⁹.

InSe and BP yield different contact properties when contacted with Au/Ti contacts, and this asymmetry leads to asymmetric electrical characteristics depending on the polarity of drain bias (V_D). While ternary states are developed at positive V_D , NDT characteristics are observed at negative V_D . Four-terminal measurements were performed on each layer, where, in principle, the contributions of contact resistances and channel resistance can be identified separately. We fabricated multiple devices with different contacts and device structures and systematically investigated the influence of contact resistances, heterojunction resistance, channel resistances, and the thickness of BP on the detailed operational characteristics.

Results and discussion

Figure 1a describes the structure of our hBN/InSe/BP heterostructure device with Au/Ti electrodes (InSe-BP-Ti device), accompanied by its optical micrograph. The hBN/InSe/BP heterostructure was achieved using the conventional dry transfer method^{2,3}. Individually exfoliated BP and InSe flakes were successively transferred on 300 nm-thick SiO₂, followed by encapsulation with a pre-patterned hBN flake. InSe and BP are vulnerable to the air, but the hBN encapsulation allows improved stability and decent mobility^{26,30}. Before the transfer, the hBN encapsulating layer was patterned using electron beam (e-beam) lithography and plasma etching to have eight openings. These allowed the InSe and BP to be partially exposed for metallization even after having the hBN cover on them. Four metal contacts on the InSe and BP were then defined by e-beam lithography, followed by Au(80 nm)/Ti(10 nm) deposition and lift-off. Figure 1b shows the atomic force microscopy (AFM) image,

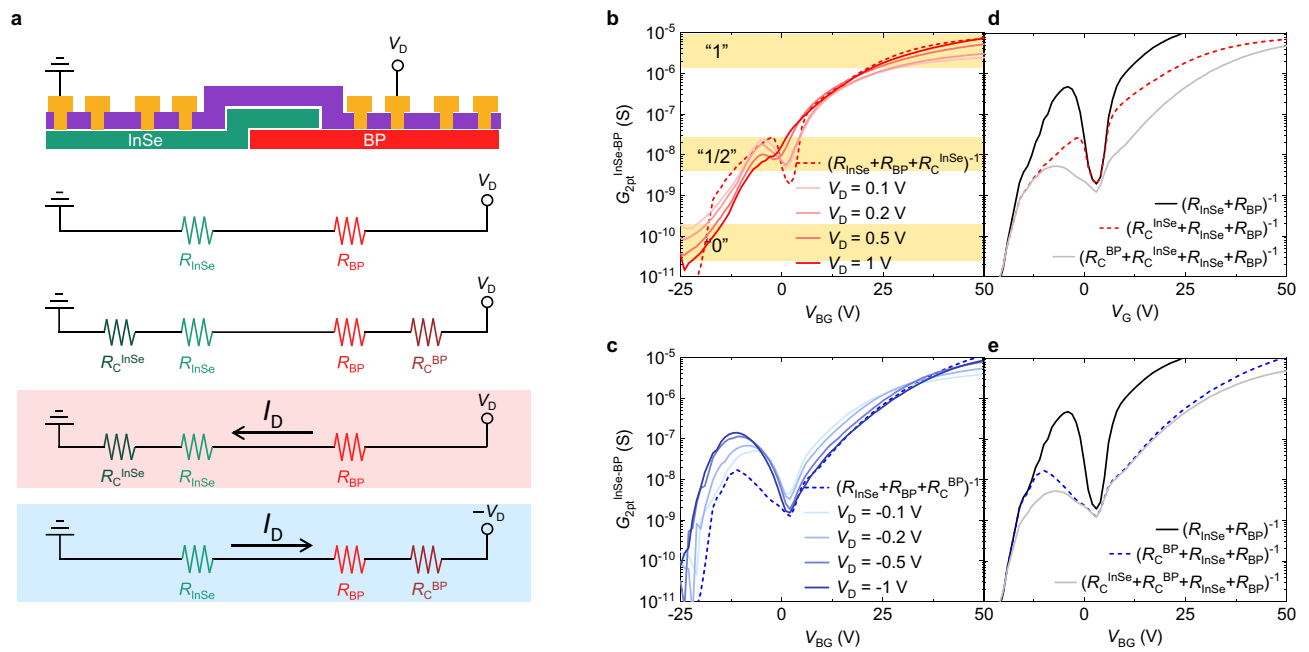


Figure 2. (a) Schematics describing the InSe-BP-Ti device (upper) and the four different equivalent circuits, consisting of R_{InSe} , R_{BP} , $R_{\text{C}}^{\text{InSe}}$, and R_{C}^{BP} . Depending on current direction, different contact resistance components are more effective. (b) $G_{2\text{pt}}^{\text{InSe-BP}}$ vs V_{BG} of the InSe-BP-Ti device measured at a forward V_{D} regime, which shows a distinct intermediate logic state with a small fluctuation. The dashed line represents $(R_{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{InSe}})^{-1}$, which is comparable to the measured $G_{2\text{pt}}^{\text{InSe-BP}}$. (c) $G_{2\text{pt}}^{\text{InSe-BP}}$ vs V_{BG} of the InSe-BP-Ti device measured at a backward V_{D} regime, which shows a strong NDT behavior with PVCR reaching $\sim 10^2$ at $V_{\text{D}} = -1$ V. The dashed line represents $(R_{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{BP}})^{-1}$, which is comparable to the $G_{2\text{pt}}^{\text{InSe-BP}}$. d,e) $(R_{\text{InSe}} + R_{\text{BP}})^{-1}$, $(R_{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{InSe}})^{-1}$, $(R_{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{BP}})^{-1}$, and $(R_{\text{C}}^{\text{BP}} + R_{\text{C}}^{\text{InSe}} + R_{\text{InSe}} + R_{\text{BP}})^{-1}$ for comparison with (b,c) data, respectively.

which reveals the thicknesses of the InSe and BP flakes as 15 nm and BP flakes and 4 nm, respectively. Figure 1c shows the three distinct Raman spectra measured on the InSe, BP, and InSe/BP overlap regions (excitation wavelength = 514 nm). The four peaks at 114 cm^{-1} , 175 cm^{-1} , 198 cm^{-1} , and 225 cm^{-1} from InSe, and the three peaks at 364 cm^{-1} , 440 cm^{-1} , and 467 cm^{-1} from BP are consistent with those previously reported^{31,32}, confirming the high quality of our flakes encapsulated by hBN. The Raman spectrum on the overlapped region shows the same peak positions originating from the InSe and BP. The Raman peak intensity is slightly weakened in the InSe/BP overlap region, compared to that in InSe/SiO₂. This Raman quenching is attributed to the weak but finite van der Waals coupling between the InSe and BP^{33,34}. Nearly consistent peak positions and the ratio of A¹(LO) peak to E¹_{2g} peak intensity suggest that the degree of strain and doping induced by having the heterostructure is negligible³⁰.

Electrical characterization was performed on the BP and InSe individually via the two-terminal and four-terminal methodology, as illustrated in the schematic in Fig. 1a^{26,35}. Figure 1d shows the two-terminal conductances ($G_{2\text{pt}}$) of the InSe ($G_{2\text{pt}}^{\text{InSe}}$) and BP ($G_{2\text{pt}}^{\text{BP}}$), and the channel conductances ($G_{4\text{pt}}$) of the InSe ($G_{4\text{pt}}^{\text{InSe}}$) and BP ($G_{4\text{pt}}^{\text{BP}}$) as a function of back-gate voltage (V_{BG}), where $G_{2\text{pt}} = I_{\text{D}}/V_{\text{D}}$, $G_{4\text{pt}} = (I_{\text{D}}/V_{4\text{pt}})(L_{4\text{pt}}/L_{2\text{pt}})$, I_{D} is the measured drain current, V_{D} is the drain bias applied on the InSe or BP, $V_{4\text{pt}}$ is the voltage difference between the two inner contacts on the InSe or BP, and $L_{4\text{pt}}$ ($L_{2\text{pt}}$) is the distance between the two inner (outer) contacts. While the BP shows an ambipolar characteristic, the InSe shows an *n*-type semiconducting behavior, similar to those of prior reports^{25,26}.

We note that the two-terminal field-effect mobilities of the InSe and BP are ~ 20 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and ~ 65 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively, and the four-terminal field-effect mobilities of the InSe and BP are ~ 370 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and ~ 120 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively (Figure S1). The two-terminal mobilities are obtained via $((1/C)(L_{2\text{pt}}/W)(dG_{2\text{pt}}/dV_{\text{BG}}))$ and the four-terminal mobilities are obtained via $((1/C)(L_{2\text{pt}}/W)(dG_{4\text{pt}}/dV_{\text{BG}}))$, where C is the back-gate capacitance and W is the channel width. The two-terminal mobilities are smaller than the four-terminal values due to contact resistances³⁶, as is particularly notable for the InSe. Figure 1e shows the channel resistivities (ρ) of the InSe (ρ_{InSe}) and BP (ρ_{BP}), and the contact resistances (R_{C}) for the InSe ($R_{\text{C}}^{\text{InSe}}$) and BP (R_{C}^{BP}), where $\rho = (1/G_{4\text{pt}})(W/L_{2\text{pt}})$ and $R_{\text{C}} = (1/G_{2\text{pt}} - 1/G_{4\text{pt}})/2$ ³⁷. R_{C}^{BP} ($R_{\text{C}}^{\text{InSe}}$) occupies a large portion of the two-terminal resistance, $1/G_{2\text{pt}}^{\text{BP}}$ ($1/G_{2\text{pt}}^{\text{InSe}}$). Figure 1f also provides I_{D} vs V_{D} output characteristics for the InSe and BP. The BP shows a linear dependence at high carrier density and even at charge neutrality (at $V_{\text{BG}} = 50$ V and 0 V), suggesting ohmic contacts, but the InSe shows a nonlinear characteristic, indicating Schottky contacts.

Figure 2a describes the measurement setup for the bias-controlled MVL and NDT properties of the InSe-BP-Ti device. While applying V_{D} to the BP and grounding the InSe, the two-terminal conductance between the source and drain ($G_{2\text{pt}}^{\text{InSe-BP}} = I_{\text{D}}/V_{\text{D}}$) was measured in our device. Figure 2b,c show the measured $G_{2\text{pt}}^{\text{InSe-BP}}$ as a function of V_{BG} at positive and negative V_{D} , respectively (Fig. 3a also provides the corresponding I_{D} as a function

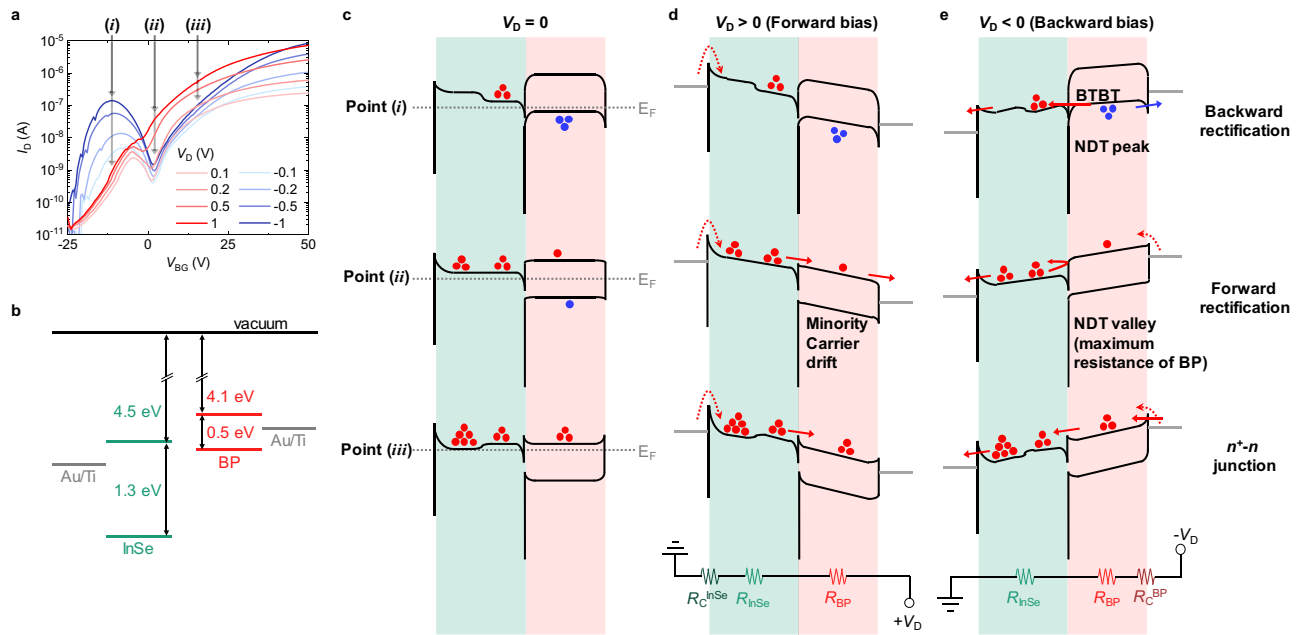


Figure 3. (a) I_D versus V_{BG} of the InSe-BP-Ti device at different V_D values. Characteristic points (i), (ii), and (iii) are marked. (b) Schematic showing the band parameters and alignment between the InSe, BP, and both Au/Ti contacts. Previously reported Schottky barrier heights of the Au/Ti contacts for the InSe and BP, rather than metal work functions, are marked^{43,44}. (c–e) Band diagrams of the InSe-BP-Ti device at points (i), (ii), and (iii) and at (c) $V_D = 0$, (d) $V_D > 0$, and (e) $V_D < 0$. Red dots represent electrons, and blue dots represent holes. Corresponding equivalent circuits are illustrated in (d,e).

of V_{BG}). In the positive V_D regime, we note the particular region where the $G_{2pt}^{InSe-BP}$ hardly changes, creating an intermediate state “1/2” (at $-6 \text{ V} < V_{BG} < 0$), accompanied by a state “0” (at $V_{BG} < -20 \text{ V}$) and a state “1” (at $V_{BG} > 25 \text{ V}$). Several studies have demonstrated ternary *inverters* based on NDT^{5,6,14,22,27,28}, where the potential inside of the constituent semiconductor barely changes within the negative transconductance region. However, this methodology is limited to the inverting logic and indeed not suitable for versatile CMOS circuitry design. Ternary *transistors* are indispensable to design versatile ternary-data-processing CMOS integrated circuits. In the negative V_D regime, a strong NDT behavior is observed, achieving a peak conductance (G_{peak}) of 140 nS and a peak-to-valley current ratio (PVCRR) of $\sim 10^2$ at $V_D = -1 \text{ V}$. Figure S2 shows transfer characteristics of our another InSe-BP-Ti device, which are qualitatively similar to those in Fig. 2b,c.

In the InSe-BP-Ti device, the total two-terminal resistance from source to drain can be approximately modeled as serially connected resistors (Fig. 2a), which can include R_C^{InSe} , R_C^{BP} , the channel resistances of the InSe (R_{InSe}), and of the BP (R_{BP}). Each of these components is acquired via the four-terminal measurements at $V_D = 1 \text{ V}$, as discussed in Fig. 1e. R_{InSe} (R_{BP}) corresponds to ρ_{InSe} (ρ_{BP}) multiplied by the appropriate dimension of the InSe (BP) region of the InSe-BP-Ti device; Figure S3 provides schematics and a table to define the multiple parameters we introduced more specifically. We assume that most of the current flows along the InSe rather than the BP in the InSe/BP overlap region. The InSe region that sits above the BP is not effectively gate-controlled due to the thick BP underneath, and thus, the InSe resistivity is assumed to be constant as ρ_{InSe} at $V_{BG} = 0 \text{ V}$, which is smaller than ρ_{BP} regardless of the applied V_{BG} (Fig. 1e). We also remark that the resistance at the heterojunction between the InSe and BP is not taken into account, which is further discussed below.

As described in the lower schematics of Fig. 2a, four different equivalent circuits are compared with our experimental data: (1) $R_{InSe} + R_{BP}$, (2) $R_C^{InSe} + R_{InSe} + R_{BP} + R_C^{BP}$, (3) $R_C^{InSe} + R_{InSe} + R_{BP}$, and (4) $R_{InSe} + R_{BP} + R_C^{BP}$. We present conductance rather than drain current in Fig. 2b,c for the comparison of the measurement to these series circuit models; there exist finite errors between them, which are discussed below. In the case of $(R_{InSe} + R_{BP})^{-1}$ without any R_C (black solid in Fig. 2d,e), a superior NDT peak arises at $V_{BG} \sim -4 \text{ V}$, which simply corresponds to when $R_{BP} + R_{InSe}$ becomes a minimum in the p -side of the BP (see Fig. 1d). When $V_{BG} < -4 \text{ V}$, the $(R_{InSe} + R_{BP})^{-1}$ value is strongly governed by R_{InSe} , which is in an insulating state. As the V_{BG} increases, R_{InSe} decreases and correspondingly $(R_{InSe} + R_{BP})^{-1}$ increases, reaching the NDT peak at $V_{BG} \sim -4 \text{ V}$. $(R_{InSe} + R_{BP})^{-1}$ then rapidly decreases and shows a valley as the BP reaches its charge neutrality, which is followed by an increase of $(R_{InSe} + R_{BP})^{-1}$ as the n -side of the BP turns on with increasing V_{BG} . The overall characteristic behavior of $(R_{BP} + R_{InSe})^{-1}$ is analogous to that of our experimentally measured $G_{2pt}^{InSe-BP}$ at negative V_D , but the G_{peak} of $(R_{BP} + R_{InSe})^{-1}$ is much higher than the experimental values. By contrast, the calculated $(R_C^{InSe} + R_{InSe} + R_{BP} + R_C^{BP})^{-1}$ value, including the R_C components, yields a largely reduced G_{peak} , which is even lower than the experimental values at both negative and positive V_D regimes.

Depending on the polarity of V_D , the R_C on the other side (R_C^{InSe} or R_C^{BP}) can be more effective due to the asymmetric nature of Schottky barriers^{38,39}. In particular, the channel of our InSe-BP-Ti device consists of two different materials, InSe and BP, which leads to strong asymmetric characteristics, depending on the polarity

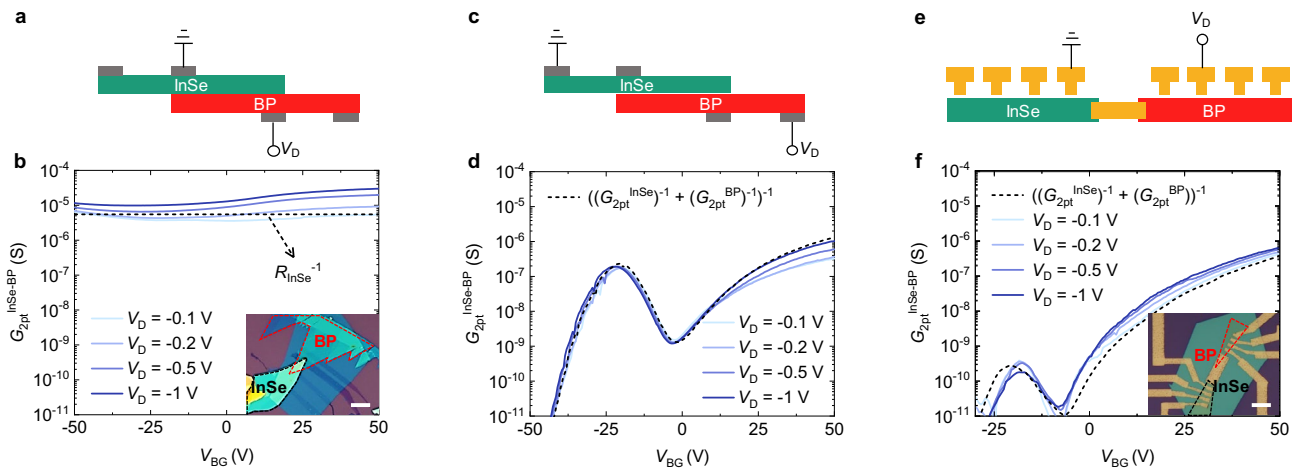


Figure 4. (a) Schematic describing the InSe-BP-FLG device and the measurement setup using the inner two electrodes. (b) $G_{2pt}^{InSe-BP}$ of the InSe-BP-FLG device measured as a function of V_{BG} at different V_D values, corresponding to the conductance of the InSe/BP overlap region. The inset shows an optical micrograph of the InSe-BP-FLG device (scale bar = 10 μ m). (c) Schematic showing the measurement setup using the outer two electrodes of the InSe-BP-FLG device. (d) $G_{2pt}^{InSe-BP}$ of the InSe-BP-FLG device as a function of V_{BG} at different V_D values, corresponding to the conductance over the whole channel region, including the non-overlapped InSe and BP regions. (e) Schematic describing the InSe-Ti-BP-Ti device and corresponding measurement setup. (f) $G_{2pt}^{InSe-BP}$ of the InSe-Ti-BP-Ti device as a function of V_{BG} at different V_D values. The inset shows an optical micrograph of the InSe-Ti-BP-Ti device (scale bar = 10 μ m).

of V_D . Interestingly, the $(R_C^{InSe} + R_{InSe} + R_{BP})^{-1}$ is similar to the measured $G_{2pt}^{InSe-BP}$ at positive V_D , while the $(R_{InSe} + R_{BP} + R_C^{BP})^{-1}$ is similar to the measured $G_{2pt}^{InSe-BP}$ at negative V_D . This is because when $V_D > 0$, electrons generally see a barrier at the junction between the Au/Ti contact and the InSe⁴⁰. By contrast, when $V_D < 0$, carriers generally see a barrier at the junction between the contact and the BP. The band diagrams further describe which side of the contact resistances, R_C^{InSe} or R_C^{BP} , is more effective, depending on the polarity of V_D (Fig. 3b–e).

Figure 3b represents the band parameters we used to build the band diagrams^{41–43}. The Schottky barrier for electrons at the junction between the 4-nm thick BP and Au/Ti contact was presumed to be ~ 0.2 eV⁴³, and the Schottky barrier at the junction between the InSe and Au/Ti contact was roughly presumed to be ~ 0.3 eV⁴⁴, as previously reported. Figure 3c–e describe the band diagrams at $V_D = 0$, $V_D > 0$, and $V_D < 0$ and at points (i), (ii), and (iii), marked in Fig. 3a. At $V_D > 0$ (Figs. 2b, 3d), the electrons entering the InSe/BP channel experience a barrier at the junction between the source and the InSe, resulting in R_C^{InSe} . The slightly smaller $G_{2pt}^{InSe-BP}$ compared to the $(R_C^{InSe} + R_{InSe} + R_{BP})^{-1}$ at point (i) is presumably due to the underestimated R_C^{InSe} value in the subthreshold region of the InSe. As the V_{BG} decreases, the R_C^{InSe} dramatically increases (Fig. 1e)²⁶, exceeding the reasonable range measurable via the conventional four-terminal methodology. The slightly higher $G_{2pt}^{InSe-BP}$, compared to the $(R_C^{InSe} + R_{InSe} + R_{BP})^{-1}$ at point (ii), is due to the minority carriers drifting in the BP injected from the InSe, a typical characteristic of a p - n diode at a forward bias. $G_{2pt}^{InSe-BP}$ agrees well with $(R_C^{InSe} + R_{InSe} + R_{BP})^{-1}$ at point (iii), where the n - n junction is made. At $V_D < 0$ (Figs. 2c, 3e), electron carriers generally see a barrier at the junction between the drain and the BP, experiencing R_C^{BP} . Distinctively, at point (i), electrons can be injected from the BP valence band, full of electrons, into the InSe via band-to-band tunneling (BTBT)¹¹. This leads to the reduced impact of R_C^{BP} and the corresponding enhanced NDT peak compared to $(R_{InSe} + R_{BP} + R_C^{BP})^{-1}$ (Fig. 2c). At points (ii) and (iii), the measured $G_{2pt}^{InSe-BP}$ agrees well with $(R_{InSe} + R_{BP} + R_C^{BP})^{-1}$. The band diagrams also explain the backward rectification at point (i) and the forward rectification at point (ii). The rectification ratio (I_D at positive V_D divided by I_D at negative V_D) values of our multiple InSe-BP-Ti devices are provided in Figure S4, where the backward rectification ratio reaches up to 10^5 .

We investigated multiple InSe-BP devices with different contacts and structures: (1) an InSe/BP heterostructure device with few-layer graphene (FLG) contacts (InSe-BP-FLG device, Fig. 4a–d), and (2) another device where InSe and BP are serially connected via Au/Ti contacts (InSe-Ti-BP-Ti device, Fig. 4e,f). As described in Fig. 4a, there are two FLG contacts on the InSe and two others under the BP in the InSe-BP-FLG device. Figure 4b shows the $G_{2pt}^{InSe-BP}$ measured using the inner two contacts, where the InSe and BP are vertically overlapped over the whole measured region. It is notable that the $G_{2pt}^{InSe-BP}$ barely depends on V_{BG} , without NDT behavior. The InSe-BP-FLG device is also measured using the outer two contacts as source and drain (Fig. 4c). In contrast to the Fig. 4a setup, the individual non-overlapped InSe and BP regions are included in the Fig. 4c setup. Figure 4d shows the correspondingly measured $G_{2pt}^{InSe-BP}$ as a function of V_{BG} . Note the NDT behavior, similar to that observed in the InSe-BP-Ti device at a negative V_D regime. This contrasts remarkably with the $G_{2pt}^{InSe-BP}$ in Fig. 4b, measured only in the InSe/BP overlap region. This clear distinction shows that the non-overlapped regions play a major role in inducing the NDT behavior. The measured $G_{2pt}^{InSe-BP}$ in Fig. 4d agrees well with $((G_{2pt}^{InSe})^{-1} + (G_{2pt}^{BP})^{-1})^{-1}$ (dashed), without considering the InSe/BP vdW junction resistance. The thicknesses of the BP and InSe layers used for the InSe-BP-FLG device are 4 nm and 15 nm (Figure S5), respectively, similar to those of the InSe-BP-Ti device. The $G_{2pt}^{InSe-BP}$ in Fig. 4b indeed agrees well with the R_{InSe}^{-1} (dashed) estimated

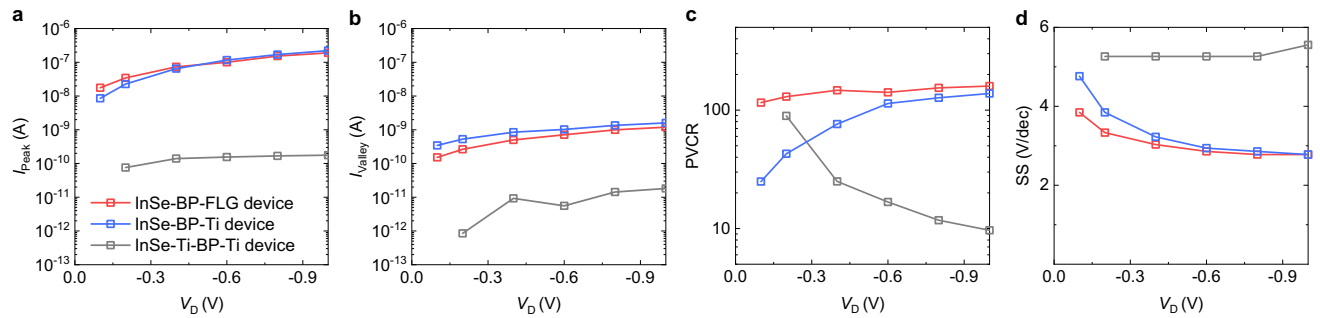


Figure 5. (a) I_{Peak} , (b) I_{Valley} , (c) PVCr, and (d) SS of the InSe-Ti-BP-Ti (grey), InSe-BP-Ti (blue), and InSe-BP-FLG (red) devices as a function of V_D .

using the ρ_{InSe} at $V_{\text{BG}} = 0$ V (data in Fig. 1e) and the dimension of the InSe region between the two inner contacts, without taking into account any of the BP region and the InSe/BP junction resistance. This suggests that the current flows mostly along the InSe, and the heterojunction resistance and FLG contact resistances are negligible compared to the InSe channel resistance. We thus neglect the InSe/BP junction resistance when considering the equivalent circuits of the InSe-BP-Ti device in Fig. 2. The low InSe/BP junction resistance even when the BP is *p*-type (at $V_{\text{BG}} < 0$) and $V_D < 0$ is due to BTBT between the InSe and BP, as described in the band diagram in Fig. 3e. The output characteristics of the individual InSe and BP regions with FLG contacts also reveal ohmic characteristics (Figure S6), which contrasts with the Schottky behavior of Au/Ti contacts on the InSe. This leads to the transconductance behavior being nearly the same regardless of the polarity of V_D (Figure S7), distinct from the InSe-BP-Ti device.

The schematic in Fig. 4e describes the InSe-Ti-BP-Ti device where InSe and BP are serially connected via Au/Ti contacts and the associated measurement setup. Figure 4f shows the $G_{2\text{pt}}^{\text{InSe-BP}}$ measured from the InSe-Ti-BP-Ti device as a function of V_{BG} at different V_D , ranging from -0.1 to -1 V. The NDT characteristics are also observed in this device, similar to the InSe-BP-Ti device and InSe-BP-FLG device. This further reveals that the NDT behavior originates from the individual InSe and BP parts rather than the vertically overlapped InSe/BP region. The measured $G_{2\text{pt}}^{\text{InSe-BP}}$ agrees well with $((G_{2\text{pt}}^{\text{InSe}})^{-1} + (G_{2\text{pt}}^{\text{BP}})^{-1})^{-1}$ (dashed line in Fig. 4f). However, we note the much lower G_{peak} (~ 0.1 nS), compared to those of the InSe-BP-Ti device and the InSe-BP-FLG device (> 0.1 μS). This is due to the additional Au/Ti contact resistances that exist between the InSe and BP, which are much larger than the InSe/BP vdW junction resistance. The thicknesses of the BP and InSe flakes in the InSe-Ti-BP-Ti device were 3 nm and 9 nm, respectively (Figure S8).

Figure 5a,b show the peak current (I_{Peak}) and valley current (I_{Valley}) of the InSe-BP-Ti, InSe-BP-FLG, and InSe-Ti-BP-Ti devices as a function of V_D from -0.1 to -1 V. Both I_{Peak} and I_{Valley} values of the InSe-Ti-BP-Ti device are far lower than those of the InSe-BP-Ti and InSe-BP-FLG devices. As mentioned above, this is attributed to the additional $R_{\text{C}}^{\text{InSe}}$ and R_{C}^{BP} from the Au/Ti contacts between the InSe and BP. Figure 5c,d show the extracted PVCr and subthreshold swing (SS) values of the devices, respectively. While the PVCr of the InSe-BP-Ti device increases as the V_D increases, the PVCr of the InSe-BP-FLG device weakly depends on V_D . In the InSe-BP-Ti device, as V_D increases, R_{C}^{BP} decreases; thus, the PVCr increases and the SS decreases. By contrast, the low FLG contact resistance in the InSe-BP-FLG device leads to the PVCr and SS being less dependent on V_D .

The transfer characteristics of the InSe-Ti-BP-Ti, InSe-BP-Ti, and InSe-BP-FLG devices can be compared to those calculated as $(R_{\text{InSe}} + R_{\text{C}}^{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{BP}})^{-1}$, $(R_{\text{InSe}} + R_{\text{BP}} + R_{\text{C}}^{\text{BP}})^{-1}$, and $(R_{\text{InSe}} + R_{\text{BP}})^{-1}$, respectively (Fig. 2a). The calculated conductances at their NDT valley points are similar (Fig. 2e), regardless of the inclusion of $R_{\text{C}}^{\text{InSe}}$ or R_{C}^{BP} . This is because the valley point characteristic is dominated by the large R_{BP} at the charge neutrality of BP. On the other hand, the conductance at the NDT peak strongly depends on whether $R_{\text{C}}^{\text{InSe}}$ or R_{C}^{BP} is included. The additional $R_{\text{C}}^{\text{InSe}}$ and R_{C}^{BP} existing in the InSe-Ti-BP-Ti device result in much lower PVCr and worse SS values due to reduced gate control. By contrast, the negligible vdW junction resistance renders better PVCr and SS values for the InSe/BP vdW heterostructure devices.

In many cases, ohmic contacts are more favorable than Schottky contacts. Our InSe-BP-FLG device also shows I_{Peak} and PVCr values higher than those of InSe-BP-Ti device (Fig. 5). The ohmic symmetric contacts in InSe-BP-FLG device lead to the nearly the same NDT characteristics for both positive and negative V_D regimes (Figure S7). On the other hand, the asymmetric Au/Ti contacts to the InSe and BP in InSe-BP-Ti device can provide dissimilar operational properties depending on the polarity of V_D , multi-valued transistor behavior at $V_D > 0$ and NDT at $V_D < 0$. Particularly at $V_D > 0$, the high Schottky barrier (contact resistance) at the junction between Au/Ti contact and InSe becomes highly effective (point (i) in Fig. 3). This suppresses the current in that regime, leading to the intermediate state for the multi-valued transistor instead of a NDT peak (Figs. 2, 3, and Figure S2). Our study as a function of multiple device parameters, including contact type and heterojunction type, can provides an idea for fine manipulation of electronic device characteristics.

In addition, we investigated the impact of BP thickness (t_{BP}) on the electrical characteristics of our InSe-BP-Ti devices. Figure 6a shows the I_D of two InSe-BP-Ti devices (solid) with different t_{BP} 4 nm and 14 nm, as a function of V_{BG} , shifted with respect to the V_{BG} at the minimum I_D of the BP. The most salient feature here is that the device with thinner BP shows significantly reduced I_{Valley} , resulting in a highly improved PVCr. The transfer curve of the BP side of each InSe-BP-Ti device is also provided for comparison (dashed). The on/off current ratio of the 4 nm-thick BP is much higher than that of the 14 nm-thick BP due to the increased band gap, as

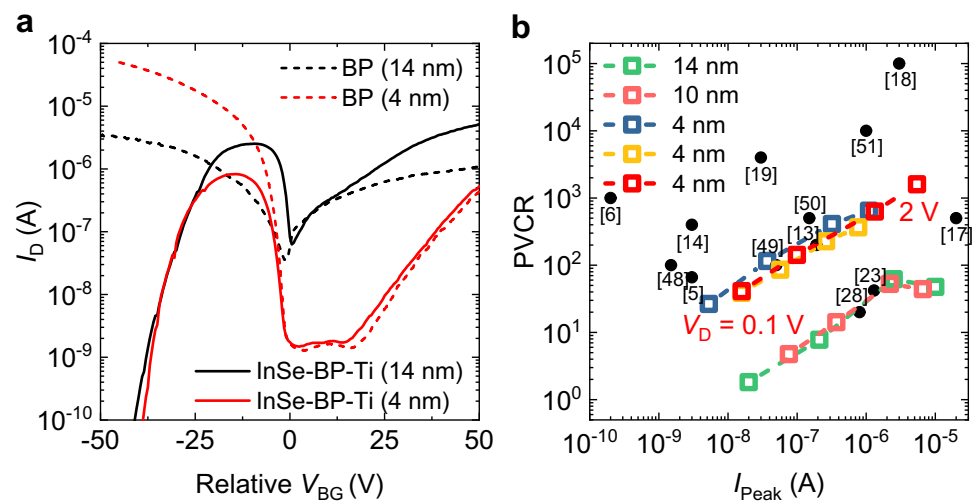


Figure 6. (a) I_D versus V_{BG} transfer characteristics of the InSe-BP-Ti devices (solid) and the BP (dashed) with different BP thicknesses, which are presented in parentheses. The V_{BG} is shifted relative to the minimum current point of the BP for each device. (b) PVCr versus I_{Peak} characteristics of our multiple InSe-BP-Ti devices with different BP thicknesses, accompanied by previously reported PVCr values of other 2D material-based NDT devices for comparison.

previously reported⁴⁵. Depending on the BP thickness ranging from 14 to 4 nm, the band gap of BP varies from 0.3 to 0.5 eV⁴³. The BP band gap change from 0.3 to 0.5 eV leads to a notable impact on the off current and corresponding PVCr of the NDT. On the other hand, the band gap change of InSe of similar thickness (4–14 nm) is 1.3–1.4 eV⁴⁶, and it does not cause much change in the off current because the band gap within that range is already quite large, compared to kT ; k is the Boltzmann constant and T is the temperature. Further thicker InSe might lead to improved I_{Peak} as the mobility increases for thicker InSe⁴⁷. Multiple InSe-BP-Ti devices with different t_{BP} , ranging from 4 to 14 nm, were examined. Figure 6b shows their PVCr values versus I_{Peak} at different V_D , along with previously reported PVCr values of other 2D material-based NDT devices^{5,6,13,14,17–19,23,28,48–51}. As noted above, the InSe-BP-Ti devices with thinner BP show higher PVCr values compared to the devices with thicker BP flakes thanks to the higher band gap and corresponding higher on/off ratio of the BP. I_{Peak} and PVCr further increase with increasing V_D , as seen in Fig. 5, achieving I_{Peak} of $\sim 5 \mu\text{A}$ and PVCr of ~ 1600 at $V_D = -2 \text{ V}$ (Figure S9). The performance also depends on the mobility and the initial doping level of BP. A few studies have reported PVCr values higher than ours, but these either applied much higher V_D ($\geq 10 \text{ V}$) or had a wider V_{BG} width of the peak^{18,19}.

Conclusion

In summary, we demonstrated bias-controlled MVL and NDT properties based on InSe/BP heterostructures. Due to the asymmetric nature of Schottky barriers at the junction between Au/Ti contact and InSe or BP, asymmetric electrical characteristics were developed depending on the polarity of V_D . At positive V_D , the InSe-BP-Ti devices worked as ternary transistors, but at negative V_D , the devices showed NDT characteristics. The contributions of contact resistances and channel resistance were identified separately via four-terminal measurements performed on each layer. Multiple devices with different contacts and device structures were investigated, and we systematically discussed the influence of contact resistances, heterojunction resistance, channel resistances, and the thickness of BP on the detailed operational characteristics of InSe/BP-based vdW heterostructures. These results provide insight into the operation principle and further performance optimization of general 2D material-based vdW heterostructures.

Experimental

Fabrication of the InSe-BP-Ti device. InSe and BP flakes were mechanically exfoliated on polydimethylsiloxane (PDMS) film using cleanroom tape, while hBN was exfoliated on 300 nm-thick SiO_2/Si substrate. Once appropriate InSe and BP flakes with the desired thicknesses were identified, the PDMS films with the flakes were cut into $10 \text{ mm} \times 10 \text{ mm}$ pieces and then attached to a glass slide for transfer to a designated location. The BP and InSe flakes on PDMS film were then successively transferred on 300 nm-thick SiO_2 , thermally grown on a highly doped Si substrate, resulting in an InSe/BP stack. To minimize the surface contamination of the device, the exfoliation and stacking processes were performed entirely in a glovebox, keeping the oxygen level below 5 ppm. The separately exfoliated hBN flake suitable for top encapsulation was patterned before the transfer using conventional e-beam lithography and reactive ion etching using SF_6 gas to have eight openings. These allowed the InSe and BP to be partially exposed for metallization even after having the hBN cover on them. The patterned hBN flake was annealed at 400°C for an hour in the Ar/H_2 atmosphere to remove polymethyl methacrylate (PMMA) residue, which also allowed the hBN to be easily picked up using a polypropylene carbonate (PPC)/PDMS stamp. The patterned hBN was then transferred onto the InSe/BP stack by melting the PPC

at ~ 120 °C. Then the hBN/InSe/BP heterostructure was washed with acetone. Additional e-beam lithography was performed to define metal contacts for the InSe-BP-Ti device, followed by Au(80 nm)/Ti(10 nm) deposition via e-beam evaporation and lift-off. The device was annealed at 400 °C for an hour in the Ar/H₂ atmosphere to remove the remaining polymer residues.

Fabrication of the InSe-Ti-BP-Ti device. The fabrication process for the InSe-Ti-BP-Ti device was similar to that of the InSe-BP-Ti device. One distinction was that the BP and InSe flakes were ~ 5 μm apart from each other without InSe/BP vdW heterojunction.

Fabrication of the InSe-BP-FLG device. FLG and hBN flakes were mechanically exfoliated on Si/SiO₂ substrates. They were annealed at 400 °C for an hour in the Ar/H₂ atmosphere. Individually exfoliated BP and InSe flakes were successively transferred on the FLG exfoliated on SiO₂, similar to the transfer process employed for the InSe-BP-Ti device. Finally, hBN and top FLG flakes were successively picked up using a PPC/PDMS stamp. Then the hBN/FLG stack was transferred to the prepared InSe/BP/FLG heterostructure on SiO₂. Au/Ti contacts were deposited on a non-encapsulated region of the FLG, followed by annealing in the Ar/H₂ atmosphere.

Material and electrical characterization. The surface topography and material quality of the fabricated devices were examined via AFM (Park systems, XE-100) and Raman spectroscopy (Renishaw, 514 nm wavelength laser). The electrical measurements were performed using a semiconductor analyzer (Keithley, 4200A-SCS) at high vacuum ($\sim 10^{-6}$ bar).

Received: 17 January 2021; Accepted: 25 March 2021

Published online: 12 April 2021

References

1. Wang, L. *et al.* One-dimensional electrical contact to a two-dimensional material. *Science* **342**, 614–617 (2013).
2. Pizzocchero, F. *et al.* The hot pick-up technique for batch assembly of van der Waals heterostructures. *Nat. Commun.* **7**, 11894 (2016).
3. Castellanos-Gomez, A. *et al.* Deterministic transfer of two-dimensional materials by all-dry viscoelastic stamping. *2D Mater.* **1**, 011002 (2014).
4. Jariwala, D. *et al.* Gate-tunable carbon nanotube–MoS₂ heterojunction p–n diode. *Proc. Natl. Acad. Sci.* **110**, 18076–18080 (2013).
5. Huang, M. *et al.* Multifunctional high-performance van der Waals heterostructures. *Nat. Nanotechnol.* **12**, 1148–1154 (2017).
6. Nourbakhsh, A., Zubair, A., Dresselhaus, M. S. & Palacios, T. Transport properties of a MoS₂/WSe₂ heterojunction transistor and its potential for application. *Nano Lett.* **16**, 1359–1366 (2016).
7. Xiong, X. *et al.* A transverse tunnelling field-effect transistor made from a van der Waals heterostructure. *Nat. Electron.* **3**, 106–112 (2020).
8. Yan, R. *et al.* Esaki diodes in van der Waals heterojunctions with broken-gap energy band alignment. *Nano Lett.* **15**, 5791–5798 (2015).
9. Fallahzad, B. *et al.* Gate-tunable resonant tunneling in double bilayer graphene heterostructures. *Nano Lett.* **15**, 428–433 (2015).
10. Roy, T. *et al.* Dual-gated MoS₂/WSe₂ van der Waals tunnel diodes and transistors. *ACS Nano* **9**, 2071–2079 (2015).
11. Liu, X. *et al.* Modulation of quantum tunneling via a vertical two-dimensional black phosphorus and molybdenum disulfide p–n junction. *ACS Nano* **11**, 9143–9150 (2017).
12. Kim, S. *et al.* Thickness-controlled black phosphorus tunnel field-effect transistor for low-power switches. *Nat. Nanotechnol.* **15**, 203–206 (2020).
13. Li, Y. *et al.* Anti-ambipolar field-effect transistors based on few-layer 2D transition metal dichalcogenides. *ACS Appl. Mater. Interfaces* **8**, 15574–15581 (2016).
14. Duong, N. T. *et al.* Modulating the functions of MoS₂/MoTe₂ van der Waals heterostructure via thickness variation. *ACS Nano* **13**, 4478–4485 (2019).
15. Balaji, Y. *et al.* MoS₂/MoTe₂ heterostructure tunnel FETs using gated Schottky contacts. *Adv. Funct. Mater.* **30**, 1905970 (2020).
16. Balaji, Y. *et al.* Tunneling transistors based on MoS₂/MoTe₂ van der Waals heterostructures. *IEEE J. Electron Devices Soc.* **6**, 1048–1055 (2018).
17. Xiong, X. *et al.* Reconfigurable logic-in-memory and multilingual artificial synapses based on 2D heterostructures. *Adv. Funct. Mater.* **30**, 1909645 (2020).
18. Wang, Y. *et al.* Light induced double ‘on’ state anti-ambipolar behavior and self-driven photoswitching in p-WSe₂/n-SnS₂ heterostructures. *2D Mater.* **4**, 025097 (2017).
19. Park, C. J. *et al.* Photovoltaic field-effect transistors using a MoS₂ and organic rubrene van der Waals hybrid. *ACS Appl. Mater. Interfaces* **10**, 29848–29856 (2018).
20. Lv, Q. *et al.* Interlayer band-to-band tunneling and negative differential resistance in van der Waals BP/InSe field-effect transistors. *Adv. Funct. Mater.* **30**, 1910713 (2020).
21. Kobashi, K., Hayakawa, R., Chikyow, T. & Wakayama, Y. Negative differential resistance transistor with organic p–n heterojunction. *Adv. Electron. Mater.* **3**, 1700106 (2017).
22. Yoo, H., On, S., Lee, S. B., Cho, K. & Kim, J. J. Negative transconductance heterojunction organic transistors and their application to full-swing ternary circuits. *Adv. Mater.* **31**, 1808265 (2019).
23. Liu, Y. *et al.* Vertical charge transport and negative transconductance in multilayer molybdenum disulfides. *Nano Lett.* **17**, 5495–5501 (2017).
24. Lee, S., Lee, Y. & Kim, C. Extraordinary transport characteristics and multivalued logic functions in a silicon-based negative-differential transconductance device. *Sci. Rep.* **7**, 11065 (2017).
25. Li, L. *et al.* Black phosphorus field-effect transistors. *Nat. Nanotechnol.* **9**, 372–377 (2014).
26. Choi, Y. *et al.* Multiterminal transport measurements of multilayer InSe encapsulated by hBN. *ACS Appl. Electron. Mater.* **3**, 163–169 (2021).

27. Kobashi, K., Hayakawa, R., Chikyow, T. & Wakayama, Y. Multi-valued logic circuits based on organic anti-ambipolar transistors. *Nano Lett.* **18**, 4355–4359 (2018).
28. Shim, J. *et al.* Light-triggered ternary device and inverter based on heterojunction of van der Waals materials. *ACS Nano* **11**, 6319–6327 (2017).
29. Lee, L. *et al.* ZnO composite nanolayer with mobility edge quantization for multi-value logic transistors. *Nat. Commun.* **10**, 1998 (2019).
30. Jang, H. *et al.* High-performance near-Infrared photodetectors based on surface-doped InSe. *Adv. Funct. Mater.* **31**, 2006788 (2021).
31. Wu, J., Mao, N., Xie, L., Xu, H. & Zhang, J. Identifying the crystalline orientation of black phosphorus using angle-resolved polarized Raman spectroscopy. *Angew. Chem. Int. Ed.* **54**, 2366–2369 (2015).
32. Sánchez-Royo, J. F. *et al.* Electronic structure, optical properties, and lattice dynamics in atomically thin indium selenide flakes. *Nano Res.* **7**, 1556–1568 (2014).
33. Dai, M. *et al.* Ultrafast and sensitive self-powered photodetector featuring self-limited depletion region and fully depleted channel with van der Waals contacts. *ACS Nano* **14**, 9098–9106 (2020).
34. Wang, F. *et al.* Tunable GaTe-MoS₂ van der Waals p–n junctions with novel optoelectronic performance. *Nano Lett.* **15**, 7558–7566 (2015).
35. Sucharitakul, S. *et al.* Intrinsic electron mobility exceeding 10³ cm²/(V s) in multilayer InSe FETs. *Nano Lett.* **15**, 3815–3819 (2015).
36. Perello, D. J., Chae, S. H., Song, S. & Lee, Y. H. High-performance n-type black phosphorus transistors with type control via thickness and contact-metal engineering. *Nat. Commun.* **6**, 7809 (2015).
37. Movva, H. C. P. *et al.* High-mobility holes in dual-gated WSe₂ field-effect transistors. *ACS Nano* **9**, 10402–10410 (2015).
38. Murali, K., Dandu, M., Das, S. & Majumdar, K. Gate-tunable WSe₂/SnSe₂ backward diode with ultrahigh-reverse rectification ratio. *ACS Appl Mater. Interfaces* **10**, 5657–5664 (2018).
39. Chen, X. *et al.* Analysis of the relationship between the contact barrier and rectification ratio in a two-dimensional P–N heterojunction. *Semicond Sci. Technol.* **33**, 114012 (2018).
40. Das, S. & Appenzeller, J. WSe₂ field effect transistors with enhanced ambipolar characteristics. *Appl. Phys. Lett.* **103**, 103501 (2013).
41. Man, M. K. L. *et al.* Imaging the motion of electrons across semiconductor heterojunctions. *Nat. Nanotechnol.* **12**, 36–40 (2017).
42. Cai, Y., Zhang, G. & Zhang, Y.-W. Layer-dependent band alignment and work function of few-layer phosphorene. *Sci. Rep.* **4**, 6677 (2015).
43. Liu, H. *et al.* Phosphorene: An unexplored 2D semiconductor with a high hole mobility. *ACS Nano* **8**, 4033–4041 (2014).
44. Chen, Y. H. *et al.* Oxidized-monolayer tunneling barrier for strong Fermi-level depinning in layered InSe transistors. *Npj 2D Mater. Appl.* **3**, 49 (2019).
45. Penumatcha, A. V., Salazar, R. B. & Appenzeller, J. Analysing black phosphorus transistors using an analytic Schottky barrier MOSFET model. *Nat. Commun.* **6**, 8948 (2015).
46. Sun, Y. *et al.* InSe: A two-dimensional material with strong interlayer coupling. *Nanoscale* **10**, 7991–7998 (2018).
47. Feng, W., Zheng, W., Cao, W. & Hu, P. Back gated multilayer InSe transistors with enhanced carrier mobilities via the suppression of carrier scattering from a dielectric interface. *Adv. Mater.* **26**, 6587–6593 (2014).
48. Park, H. J. *et al.* Hybrid characteristics of MoS₂ monolayer with organic semiconducting tetracene and application to anti-ambipolar field effect transistor. *ACS Appl Mater. Interfaces* **10**, 32556–32566 (2018).
49. Kim, J. K. *et al.* Trap-mediated electronic transport properties of gate-tunable pentacene/MoS₂ p–n heterojunction diodes. *Sci. Rep.* **6**, 36775 (2016).
50. Jariwala, D. *et al.* Hybrid, gate-tunable, van der Waals p–n heterojunctions from pentacene and MoS₂. *Nano Lett.* **16**, 497–503 (2016).
51. Wang, Z., He, X., Zhang, X. X. & Alshareef, H. N. Hybrid van der Waals p–n heterojunctions based on SnO and 2D MoS₂. *Adv. Mater.* **28**, 9133–9141 (2016).

Acknowledgements

This work was supported by Nano-Material Technology Development program (NRF-2016M3A7B4909942) through the National Research Foundation of Korea (NRF), funded by the Ministry of Science and ICT, Korea, and the NRF grant funded by the Korean government (NRF-2018R1C1B3002733).

Author contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary Information The online version contains supplementary material available at <https://doi.org/10.1038/s41598-021-87442-1>.

Correspondence and requests for materials should be addressed to K.L.

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