


Article

# Drain Current Stress-Induced Instability in Amorphous InGaZnO Thin-Film Transistors with Different Active Layer Thicknesses

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**Abstract:** In this study, the initial electrical properties, positive gate bias stress (PBS), and drain current stress (DCS)-induced instabilities of amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) with various active layer thicknesses ( $T_{IGZO}$ ) are investigated. As the  $T_{IGZO}$  increased, the turn-on voltage ( $V_{on}$ ) decreased, while the subthreshold swing slightly increased. Furthermore, the mobility of over  $13 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  and the negligible hysteresis of  $\sim 0.5 \text{ V}$  are obtained in all of the a-IGZO TFTs, regardless of the  $T_{IGZO}$ . The PBS results exhibit that the  $V_{on}$  shift is aggravated as the  $T_{IGZO}$  decreases. In addition, the DCS-induced instability in the a-IGZO TFTs with various  $T_{IGZO}$  values is revealed using current–voltage and capacitance–voltage ( $C$ – $V$ ) measurements. An anomalous hump phenomenon is only observed in the off state of the gate-to-source ( $C_{gs}$ ) curve for all of the a-IGZO TFTs. This is due to the impact ionization that occurs near the drain side of the channel and the generated holes that flow towards the source side along the back-channel interface under the lateral electric field, which cause a lowered potential barrier near the source side. As the  $T_{IGZO}$  value increased, the hump in the off state of the  $C_{gs}$  curve was gradually weakened.

**Keywords:** drain current stress; instability; InGaZnO; thin-film transistors; active layer thickness

## 1. Introduction

Recently, amorphous indium gallium zinc oxide (a-IGZO), as a representative of an amorphous metal oxide-based semiconductor, has been widely investigated for use in the active layer of thin-film transistors (TFTs) due to its high electron mobility, good transparency in visible light, chemical and thermal stability, low temperature processing, and smooth surface [1–4]. The a-IGZO TFT with excellent electrical properties, such as high mobility ( $\mu$ ) of over  $10 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  and low values of subthreshold swing, has become one of the research hotspots for the advanced display application in next-generation active-matrix liquid crystal displays (AM-LCDs) and active-matrix organic light-emitting diodes (AM-OLEDs) [5–8]. Hitherto, AM-OLEDs driven by the a-IGZO TFTs involve two or three transistors and one capacitor current-biased voltage-programmed pixel circuit. Therefore, the stability of the a-IGZO TFTs under long-term current-bias is a critical issue for these circuits in AM-OLEDs. However, the a-IGZO TFTs inevitably suffer gate and drain bias stresses during practical operation conditions, leading to device instability and hindering their development

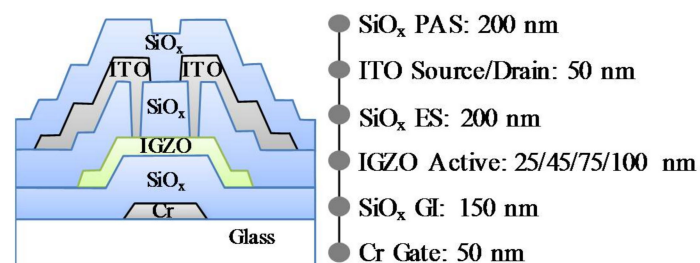
for commercial products [9,10]. Fujii et al. [11] have investigated the increase in internal temperature of the IGZO TFTs when the device was operated in the saturation region. Choi et al. [12] have reported that the electron-hole pair generation by impact ionization near the drain side contributed to the negative shift of the threshold voltage of IGZO TFTs with wide channel width under a high gate and drain bias stress. Valdinoci et al. [13] have reported that the electron-hole pair generation by impact ionization near the drain region caused the floating body effect in high  $\mu$  poly-Si TFTs. Consequently, the electrical stability under drain current stress was considered to be an important issue, especially for high- $\mu$  oxide TFTs.

Moreover, the active layer thickness is an important parameter to adjust device electrical properties, such as on/off ratio, threshold voltage, and field effect mobility [14–16]. As reported in previous publications, the device performance is significantly influenced by the semiconductor/gate insulator (GI) interfacial density [17,18] and the active layer trap density [19], indicating that the total trap density increases with the increase in the active layer thickness [20], which can effectively modify the threshold voltage and field effect mobility. Therefore, the impact of the active layer thickness ( $T_{IGZO}$ ) on the instability induced by the positive gate bias stress (PBS) and the drain current stress (DCS) in a-IGZO TFTs should be well investigated.

In this study, the initial electrical properties and PBS and DCS-induced instabilities of a-IGZO TFTs with various  $T_{IGZO}$  are investigated. Moreover, the DCS-induced instability in the a-IGZO TFTs with various  $T_{IGZO}$  is revealed by the combination of current-voltage ( $I$ - $V$ ) and capacitance-voltage ( $C$ - $V$ ) measurements.

## 2. Experimental

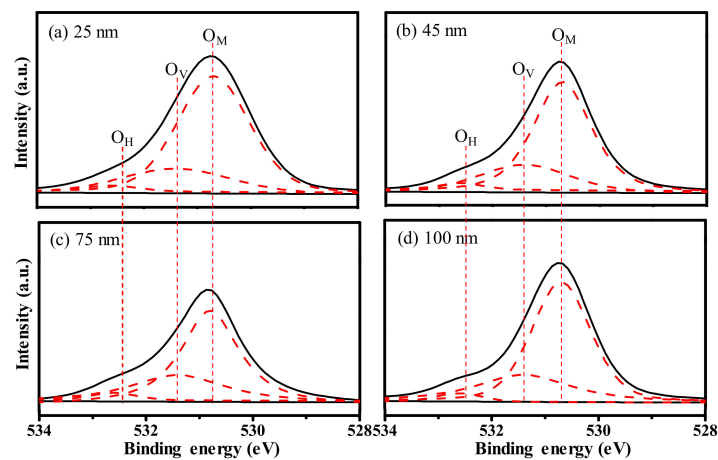
A schematic cross-sectional view and fabrication process of the bottom-gate IGZO TFT are shown in Figure 1. The fabrication procedure for the a-IGZO TFT is as follows. A chromium (Cr) gate electrode is firstly formed on a glass substrate. A  $\text{SiO}_x$  gate insulator (GI) with a thickness of 150 nm is then deposited at 350 °C by plasma-enhanced chemical vapor deposition (PECVD). The a-IGZO layer with thicknesses of 25 nm, 45 nm, 75 nm, and 100 nm are deposited at 160 °C from a sintered IGZO ceramic target by direct current (DC) magnetron sputtering with a mixed gas of  $\text{Ar}/\text{O}_2 = 29.4/0.6$  sccm at a deposition pressure of 1 Pa. After patterning the IGZO film as an active channel, a  $\text{SiO}_x$  film (200 nm) as an etch stopper is deposited by PECVD. Source and drain electrodes are formed using indium tin oxide (ITO) via contact holes. A 200-nm thick  $\text{SiO}_x$  passivation layer is also deposited by PECVD. Finally, the IGZO TFTs are annealed in  $\text{N}_2$  ambient at 350 °C for 1 h before electrical measurements. The channel width ( $W$ ) and length ( $L$ ) the IGZO TFTs are 50  $\mu\text{m}$  and 20  $\mu\text{m}$ , respectively. All of the  $I$ - $V$  characteristics are measured using an Agilent 4156C precision semiconductor parameter analyzer. The  $C$ - $V$  measurements, the channel capacitance ( $C_{gc}$ ), the gate-to-source capacitance ( $C_{gs}$ ), and the gate-to-drain capacitance ( $C_{gd}$ ), are measured at 1 kHz and an alternating current (AC) level of 100 mV. All of the measurements are carried out at room temperature in ambient air.



**Figure 1.** A schematic cross-sectional view and fabrication process of the bottom-gate indium gallium zinc oxide (IGZO) thin-film transistor (TFT).

### 3. Results and Discussion

To investigate the thickness impact on the chemical properties and bonding states of the IGZO films, an X-ray photoelectron spectroscopy (XPS, ESCALAB250Xi, Thermo Fisher Scientific, Waltham, MA, USA) measurement is performed. Figure 2 shows the O 1s XPS spectra of the IGZO films with various thicknesses. The O 1s spectra can be resolved into three nearly Gaussian distribution peaks approximately centered at 530.7 eV, 531.4 eV, and 532.6 eV. The peaks at the binding energy of 530.7 eV (labeled as  $O_M$ ), 531.4 eV (labeled as  $O_V$ ), and 532.6 eV (labeled as  $O_H$ ) are attributed to the  $O^{2-}$  ions combined with the metal atoms, oxygen deficiency, and hydroxyl groups in a stoichiometric IGZO structure, respectively [21]. The positions, areas, and area ratios of the O 1s three peaks for the IGZO films with various thicknesses are summarized in Table 1. For the 25-nm thick IGZO film, the  $O_M/(O_M + O_V + O_H)$  and  $O_V/(O_M + O_V + O_H)$  area ratios are 74.4% and 22.4%, respectively. It is suggested that the IGZO film contains a small quantity of oxygen-related defects during the short-time fabrication in the chamber. With the increase in the deposition duration, the  $O_V/(O_M + O_V + O_H)$  area ratio evidently increased, whereas the  $O_M/(O_M + O_V + O_H)$  area ratio obviously decreased. When the IGZO thickness is increased to 100 nm, the area ratios of  $O_V/(O_M + O_V + O_H)$  and  $O_M/(O_M + O_V + O_H)$  are changed remarkably to 29.1% and 67.7%, respectively. These results reveal that the long-time sputtering process deteriorates the quality of the IGZO film and accelerates the generation of the oxygen-related defects, which cause the unbalanced chemical bonds of metal and oxygen atoms. Interestingly, the area ratio of  $O_H/(O_M + O_V + O_H)$  keeps the small constant of ~3.2%, even for IGZO films fabricated under different durations, implying that the magnetron sputtering method is a promising approach to obtain a metal oxide semiconductor with small amounts of hydroxyl groups.

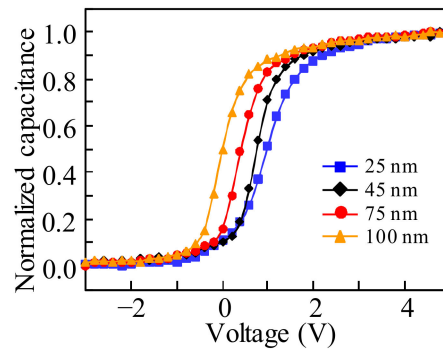


**Figure 2.** X-ray photoelectron spectroscopy (XPS) spectra of O 1s peaks of the IGZO films with the thickness of (a) 25 nm; (b) 45 nm; (c) 75 nm; and (d) 100 nm, respectively.

**Table 1.** The position, areas, and area ratios of the deconvoluted O 1s peaks for the IGZO films with various thicknesses.

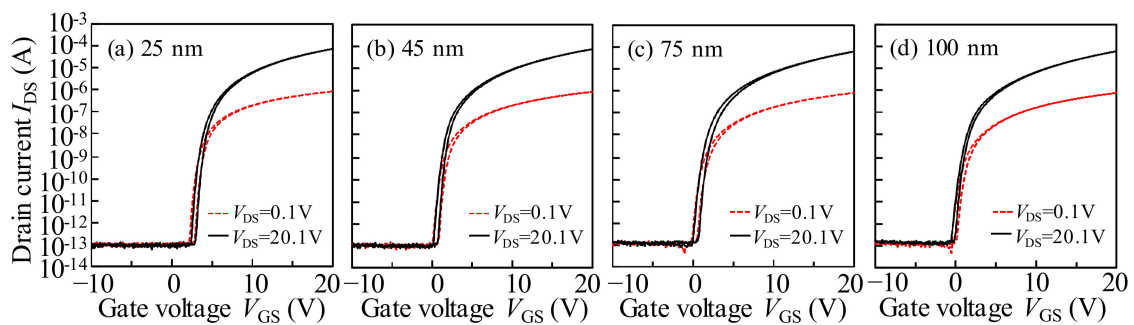
O 1s		IGZO Thickness (nm)			
		25	45	75	100
$O_M$	Position (eV)	530.7	530.7	530.7	530.7
	Area	177500	159500	158000	156000
$O_V$	Position (eV)	531.4	531.4	531.4	531.4
	Area	53500	55500	61000	67000
$O_H$	Position (eV)	532.6	532.6	532.6	532.6
	Area	7500	7000	7000	7500
$O_M/(O_M + O_V + O_H)$ area ratio (%)		74.4	71.8	69.9	67.7
$O_V/(O_M + O_V + O_H)$ area ratio (%)		22.4	25.0	27.0	29.1
$O_H/(O_M + O_V + O_H)$ area ratio (%)		3.2	3.2	3.1	3.2

Figure 3 illustrates the  $C$ - $V$  plot as a function of the thickness of IGZO in the ITO/IGZO/SiO<sub>2</sub>/Cr stack structure. It is noted that the increase in the IGZO thickness induces a negative shift of the flat band voltage ( $V_{FB}$ ). The variation of the  $V_{FB}$  in the negative direction implies that the threshold voltage ( $V_{th}$ ) of the ITO/IGZO/SiO<sub>2</sub>/Cr stack structure-based TFTs can be adjusted by using the IGZO layer with various thicknesses. In addition, the maximum negative shift of  $V_{FB}$  is observed for the IGZO film with the thickness of 100 nm, which contributes to the largest negative shift of the  $V_{th}$ .



**Figure 3.** Capacitance–voltage ( $C$ - $V$ ) characteristics of the indium tin oxide (ITO)/IGZO/SiO<sub>2</sub>/Cr stack structure with various  $T_{IGZO}$ .

Figure 4 shows the initial transfer characteristics ( $I_{DS}$ - $V_{GS}$ ) of a-IGZO TFTs with various active layer thicknesses ( $T_{IGZO}$ ) measured at  $V_{DS}$  values of 0.1 V and 20.1 V. The electrical properties, such as field effect mobility in the saturation region ( $\mu_{sat}$ ),  $V_{on}$  (defined by  $V_{GS}$  at  $I_{DS}$  of 1 nA), subthreshold swing ( $SS = dV_{GS}/d\log_{10}(I_{DS})$ ), and hysteresis of the transfer curves (defined by the difference of  $V_{GS}$  at  $I_{DS}$  of 1 nA between the forward and reverse sweeps) are summarized in Table 2.



**Figure 4.** The initial transfer characteristics ( $I_{DS}$ - $V_{GS}$ ) of amorphous indium gallium zinc oxide (a-IGZO) TFTs with various  $T_{IGZO}$  of (a) 25 nm; (b) 45 nm; (c) 75 nm; and (d) 100 nm measured at  $V_{DS}$  of 0.1 and 20.1 V, respectively.

**Table 2.** The electrical properties of a-IGZO TFTs with various  $T_{IGZO}$ .

Thickness (nm)	25	45	75	100
$\mu_{sat}$ (cm <sup>2</sup> ·V <sup>-1</sup> ·s <sup>-1</sup> )	14.17	14.01	13.62	13.04
$V_{on}$ at $I_{DS} = 1$ nA (V)	2.32	0.27	0.04	-0.33
Hysteresis $\Delta V_H$ (V)	0.52	0.54	0.55	0.43
Subthreshold swing (mV/dec.)	323	367	416	475

The saturation mobility  $\mu_{\text{sat}}$  is calculated by fitting a straight line to the plot of the square root of  $I_{\text{DS}}$  versus  $V_{\text{GS}}$  based on the following equation [22]:

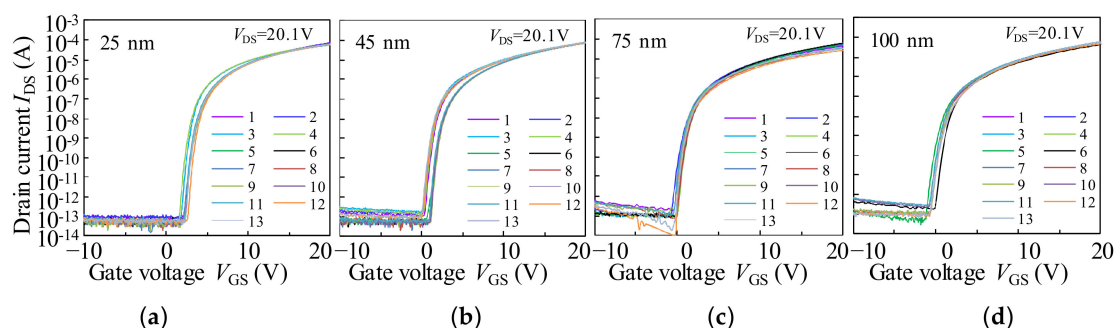
$$I_{\text{DS}} = \frac{\mu_{\text{sat}} W C_{\text{SiO}_x}}{2L} (V_{\text{GS}} - V_{\text{th}})^2 \quad (1)$$

where  $W$  and  $L$  are the channel width and length, respectively, and  $C_{\text{SiO}_x}$  is the capacitance per unit area of the GI. When the  $T_{\text{IGZO}}$  is increased from 25 nm to 100 nm, the  $\mu_{\text{sat}}$  is slightly degraded from  $14.17 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$  to  $13.04 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ . The  $\mu_{\text{sat}}$  is affected by the quality of the active layer and the a-IGZO/GI interface. To confirm the influence of the  $T_{\text{IGZO}}$  on the quality of the a-IGZO/GI interface, the hysteresis behaviors of the IGZO TFT with various  $T_{\text{IGZO}}$  are extracted, as listed in Table 1. The identically negligible clockwise hysteresis is obtained regardless of the  $T_{\text{IGZO}}$ , indicating that the good quality of the IGZO/GI interface is well kept during the fabrication processes for all of the IGZO TFTs. Moreover, the  $V_{\text{on}}$  and SS values are significantly changed from 2.32 V and 323 mV/dec. in the 25-nm thick IGZO TFT to  $-0.33 \text{ V}$  and 475 mV/dec. in the 100-nm thick IGZO TFT, respectively. The degraded SS value and the shifted  $V_{\text{on}}$  in the negative  $V_{\text{GS}}$  direction can be commonly interpreted as consequences of the total defect states and free carrier numbers being increased as the  $T_{\text{IGZO}}$  values increased, which is consistent with previous publications [23,24] and in agreement with the C–V measurements in Figure 3. Generally, the SS value is an indicator of the maximum area density of state ( $N_{\text{t}}$ ), including the interfacial ( $D_{\text{it}}$ ) and the semiconductor bulk traps ( $N_{\text{bulk}}$ ). The  $N_{\text{t}}$  value can be extracted from following equation [25]:

$$N_{\text{t}} = \left( \frac{SS \times \log(e)}{kT/q} - 1 \right) \frac{C_{\text{SiO}_x}}{q} \quad (2)$$

where  $q$  is the electron charge, and  $k$  is the Boltzmann constant. The  $N_{\text{t}}$  values were  $6.53 \times 10^{11}$ ,  $7.62 \times 10^{11}$ ,  $8.83 \times 10^{11}$ , and  $1.03 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$  for the IGZO TFTs with the  $T_{\text{IGZO}}$  values of 25 nm, 45 nm, 75 nm, and 100 nm, respectively. Obviously, the  $N_{\text{t}}$  is increased with the increase in the  $T_{\text{IGZO}}$  value, which is consistent with the XPS results. The results exhibit that the change in the  $N_{\text{t}}$  mainly originated from the  $N_{\text{bulk}}$ , owing to the similar a-IGZO/GI interfacial quality.

To confirm the uniformity and reproducibility of the a-IGZO TFTs with various  $T_{\text{IGZO}}$ , the  $I_{\text{DS}}-V_{\text{GS}}$  curves of the 13 individual devices measured at  $V_{\text{DS}}$  of 20.1 V are shown in Figure 5, respectively. The corresponding electrical properties, such as  $\mu_{\text{sat}}$ ,  $V_{\text{on}}$ , SS, and hysteresis, are listed in Table 3. Notably, the statistical distribution of all of the parameters has the same tendency as described in Table 1 and small standard deviations, thereby indicating very good reproducibility in the fabricated a-IGZO TFTs.

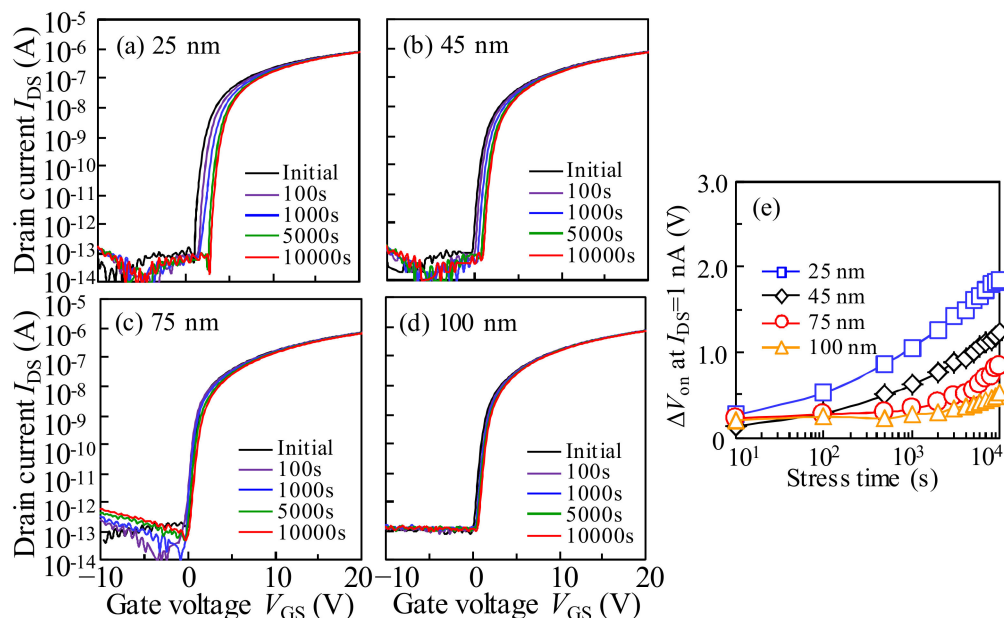


**Figure 5.** The  $I_{\text{DS}}-V_{\text{GS}}$  of 13 individual TFTs with various  $T_{\text{IGZO}}$  of (a) 25 nm; (b) 45 nm; (c) 75 nm; and (d) 100 nm measured at  $V_{\text{DS}}$  of 20.1, respectively.

**Table 3.** The statistical deviation of the electrical properties of a-IGZO TFTs with various  $T_{IGZO}$ .

Thickness (nm)	25	45	75	100
$\mu_{sat}$ ( $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ )	$13.91 \pm 0.92$	$13.70 \pm 0.39$	$12.50 \pm 1.01$	$11.88 \pm 0.34$
$V_{on}$ at $I_{DS} = 1$ nA (V)	$2.29 \pm 0.28$	$1.60 \pm 0.46$	$1.31 \pm 0.44$	$0.88 \pm 0.46$
Hysteresis $\Delta V_H$ (V)	$0.37 \pm 0.18$	$0.33 \pm 0.07$	$0.38 \pm 0.27$	$0.28 \pm 0.12$
SS (mV/dec.)	$279 \pm 24$	$287 \pm 19$	$314 \pm 23$	$351 \pm 26$

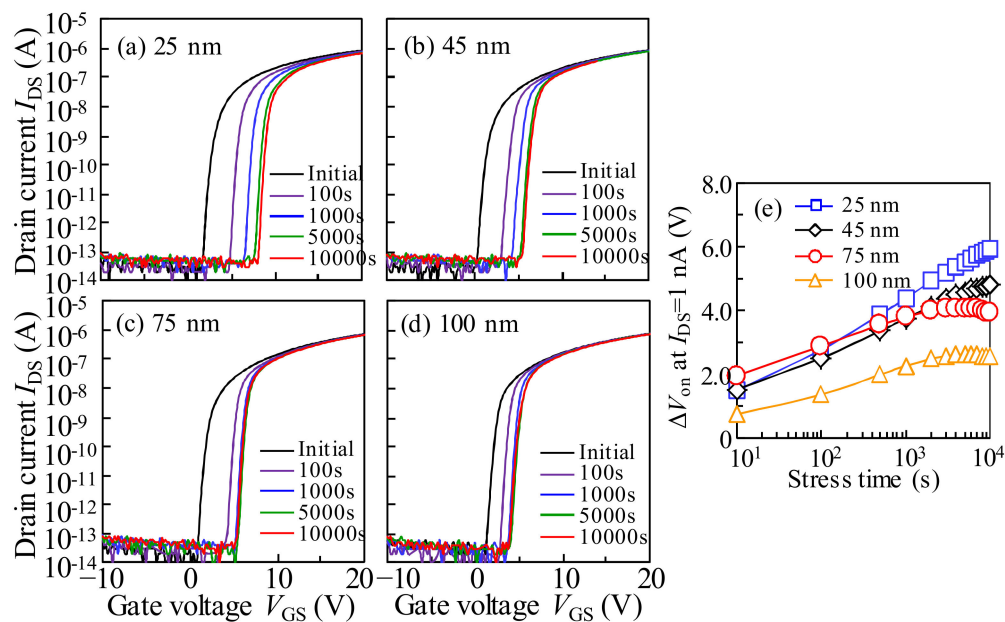
To investigate the impact of the  $T_{IGZO}$  on the stability of a-IGZO TFTs, the positive bias stress (PBS) is carried out. Figure 6a–d shows the variation in the transfer characteristics of the a-IGZO with various  $T_{IGZO}$  under PBS with a  $V_{GS}$  value of 20 V. The variation in  $V_{on}$  ( $\Delta V_{on}$ ) as a function of PBS duration for the a-IGZO TFTs with various  $T_{IGZO}$  values is shown in Figure 5e. It is found that the transfer characteristics for all of the TFTs under PBS shift parallel in the positive  $V_{GS}$  direction without SS degradation, indicating that the electrons are trapped at the interface of the a-IGZO or in the GI without introducing any defects. When the  $T_{IGZO}$  is decreased from 100 nm to 25 nm, the  $\Delta V_{on}$  is remarkably increased from 0.52 V to 1.85 V after the stress duration of  $10^4$  s. The obtained results can be explained by the vertical electrical field distribution. Generally, the electric potential exponentially declines inside the active layer, and has a maximum transfer length called the Debye length. For the a-IGZO TFT, the calculated Debye length was  $\sim 40$  nm [19]. When the  $T_{IGZO}$  is less than Debye transfer length ( $T_{IGZO} = 25$  nm), the surface potential will exponentially decline into the whole active layer. Therefore, with the decrease in the  $T_{IGZO}$  value, the electrical field will be enhanced. Under PBS, the electrons in the thinner  $T_{IGZO}$  will be accelerated by the enhanced surface field, which are accumulated by electrical field energy and are trapped at the interface of the a-IGZO/GI or in the GI under the positive bias, leading to the large positive  $V_{GS}$  shift. When the  $T_{IGZO}$  increased to more than the Debye length of 40 nm, the electric field at the front-interface becomes lower, contributing to the few electrons that are trapped at the front-interface, which exhibits the small  $\Delta V_{on}$  with the increase in the  $T_{IGZO}$  value.



**Figure 6.** Evolution of transfer characteristics in the a-IGZO TFT with the  $T_{IGZO}$  values of (a) 25 nm; (b) 45 nm; (c) 75 nm; and (d) 100 nm as a function of the 20 V positive gate bias stress (PBS) duration for  $10^4$  s; and (e) the variation in  $\Delta V_{on}$  as a function of PBS duration for the a-IGZO TFTs with various  $T_{IGZO}$ .



To simulate the practical operation conditions, the drain current stress (DCS) is applied to the a-IGZO TFTs with various  $T_{IGZO}$  values. Figure 7a–d shows the variation in the transfer characteristics of the a-IGZO with various  $T_{IGZO}$  under DCS with  $V_{GS} = V_{DS} = 25$  V. The variations in  $\Delta V_{on}$  as a function of the DCS duration for the a-IGZO TFTs with various  $T_{IGZO}$  values are shown in Figure 7e. Noticeably, the transfer curves of all of the a-IGZO TFTs exhibit a parallel shift in the positive  $V_{GS}$  direction without SS degradation during the DCS duration. In the initial stage of DCS (<100 s), all of the transfer curves shift significantly towards the  $V_{GS}$  direction without SS degradation. In the subsequent stage (>100 s), the amplitude of  $\Delta V_{on}$  becomes weakened, and the  $\Delta V_{on}$  increases with the decrease in the  $T_{IGZO}$  after the DCS for  $10^4$  s.

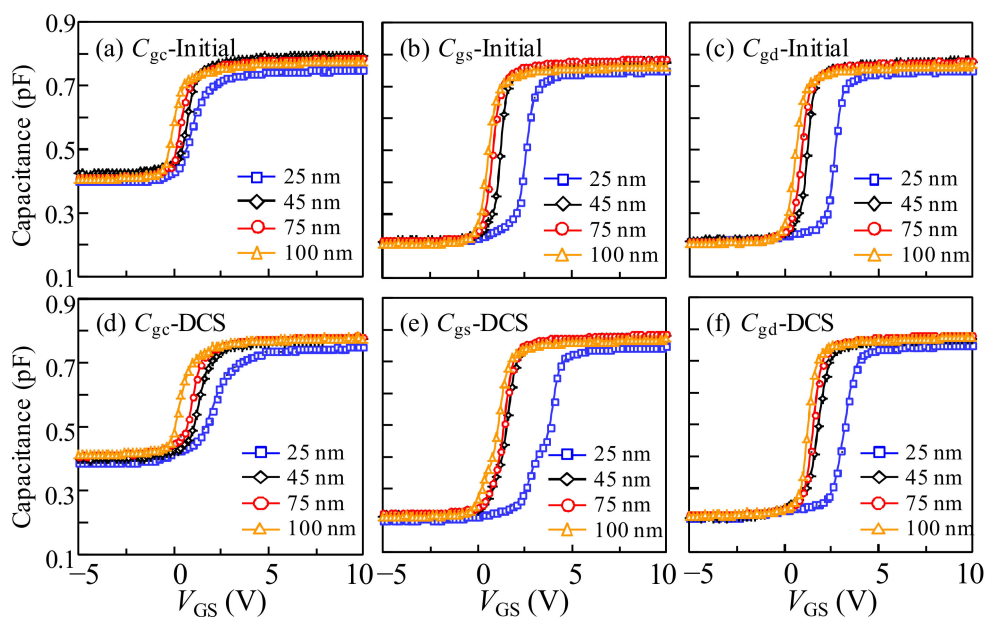


**Figure 7.** Evolution of transfer characteristics in the a-IGZO TFT with the  $T_{IGZO}$  values of (a) 25 nm; (b) 45 nm; (c) 75 nm; and (d) 100 nm as a function of the drain current stress (DCS) ( $V_{GS} = V_{DS} = 25$  V) duration for  $10^4$  s, and (e) the variation in  $\Delta V_{on}$  as a function of DCS duration for the a-IGZO TFTs with various  $T_{IGZO}$ .

To clarify the mechanism of the DCS-induced instability in the a-IGZO TFTs with various  $T_{IGZO}$ , the  $C-V$  analyses of  $C_{gc}$ ,  $C_{gs}$ , and  $C_{gd}$  before and after DCS duration of  $10^4$  s are carried out, as shown in Figure 8. Compared with the  $C_{gc}$  curves of the a-IGZO TFTs with various  $T_{IGZO}$  values in the initial stage and after DCS duration, all of the  $C_{gc}$  curves exhibited a positive  $V_{GS}$  shift with distortion in the off state of the  $C-V$  curves. The shift of the  $C-V$  curves is weakened as the  $T_{IGZO}$  value increases, which has a similar tendency to the  $I-V$  curves, as shown in Figure 7. However, the shift amplitude of the  $C-V$  curves is smaller than that of the  $I-V$  curves, indicating that the less free carriers are trapped, or the trapped carriers are partly de-trapped during the  $C-V$  measurement after the DCS. Furthermore, the hump phenomenon in the off state of the  $C-V$  curves becomes weakened as the  $T_{IGZO}$  values increase, which is hardly observed in the  $I-V$  curves. To further investigate the origin of the hump phenomenon in the off state of the  $C-V$  curves, the  $C_{gs}$  and  $C_{gd}$  values before and after the DCS are measured. Note that the both  $C_{gs}$  and  $C_{gd}$  curves exhibit a parallel shift in the positive  $V_{GS}$  direction. However, the hump phenomenon is only observed in the  $C_{gs}$  curve rather than the  $C_{gd}$  curve during the DCS.

In terms of the a-IGZO TFT with a  $T_{IGZO}$  of 25 nm under the DCS ( $V_{DS} = V_{GS}$ ), the electrons are transported from the source to drain side along the front-channel interface, which contributes to a depletion region near the drain side. Combined with the case of 25-nm thick IGZO TFT under the PBS, in the initial stage of DCS (<100 s), the electrons are accelerated to the front-channel under the

high vertical electric field. Then, they are trapped at the interface of the a-IGZO/GI or injected into the GI, resulting in a significantly positive  $V_{GS}$  shift of the transfer curve. Simultaneously, the electrons are accelerated from the source to the drain side under the lateral electric field, resulting in the impact ionization occurring at the drain side of the channel [12]. Subsequently, the electron-hole pairs are generated by impact ionization near the drain side. The generated electrons and holes are collected at the front-channel and the etch-stopper/IGZO (back-channel) interfaces, respectively. The generated holes flow towards the source side along the back-channel interface and cause a lowered potential barrier near the source side, leading to the additional charge response in the  $C-V$  measurement, which contributes to the hump in the off state of the  $C_{gs}$  curve. The schematic diagram of DCS-induced degradation in the IGZO TFT with the  $T_{IGZO}$  of 25 nm is illustrated in Figure 9a. In the subsequent stage ( $>100$  s), with the extension of DCS duration, the more generated holes are accumulated near the source side, which contributes to the increase in the body potential. Therefore, the  $\Delta V_{on}$  of the transfer curve is weakened with the DCS duration.



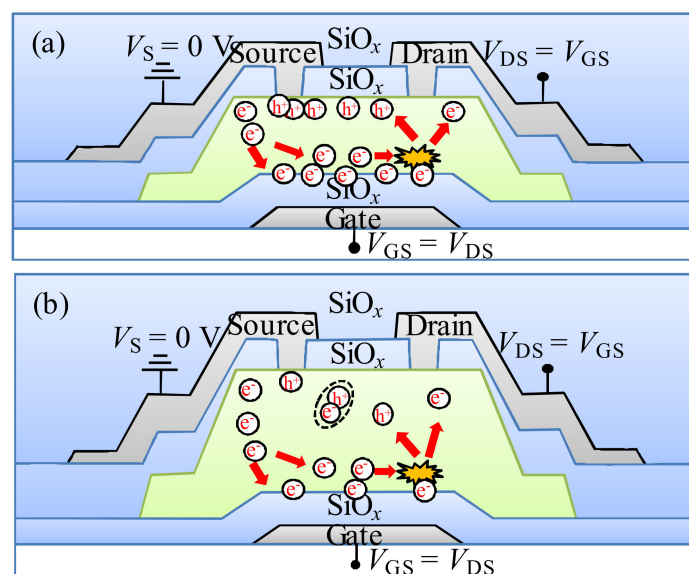
**Figure 8.**  $C-V$  curves of (a)  $C_{gc}$ ; (b)  $C_{gs}$ ; and (c)  $C_{gd}$  in the initial and (d)  $C_{gc}$ ; (e)  $C_{gs}$ ; and (f)  $C_{gd}$  after a DCS duration of  $10^4$  s with various  $T_{IGZO}$ .

When the  $T_{IGZO}$  value is increased to 45 nm, a similar phenomenon is observed in the a-IGZO TFT under the DCS of  $10^4$  s. Due to the reduction of the vertical electric field, the amount of the trapped electrons are decreased at the interface of the channel/GI or into the GI, leading to the smaller  $\Delta V_{on}$  of the transfer curves compared with the 25-nm thick IGZO TFT, which is in agreement with the  $I-V$  and  $C-V$  results. Meanwhile, the impact ionization occurs near the drain side under the lateral electric field. The electrons are accelerated from the source to the drain side, which induces the generation of the electron-hole pair near the drain side. The generated holes drift towards the source side along the back-channel interface. Due to the amount of free electrons that increase with the increase in the  $T_{IGZO}$ , the recombination probability of the holes and electrons are enlarged during the hole drifting. The number of the collected holes at the source side is reduced, contributing to the small hump in the off state of the  $C_{gs}$  curve. When the  $T_{IGZO}$  is further increased to 75 nm or 100 nm, the positive  $V_{GS}$  shift of the transfer curves is significantly decreased due to the weaker vertical electric field with the increase in the  $T_{IGZO}$  value, contributing to the slightly positive  $V_{GS}$  shift of the  $I-V$  and  $C-V$  curves. The schematic diagram of the mechanism of DCS-induced instability in the IGZO TFT with the thicker  $T_{IGZO}$  is illustrated in Figure 9b. The generated holes induced by the impact ionization in the drain region are drifted from the drain to the source side along the back-channel under the vertical and



lateral electric fields. The holes would suffer easily from the recombination with the more free electrons in the thicker IGZO layer. Therefore, the slight hump in the off state of the  $C_{gs}$  curve is attributed to the few holes that are accumulated at the back-channel near the source side.

Besides the  $T_{IGZO}$  value, the architecture of devices also plays a critical role in the DCS-induced instability of the TFTs. On the basis of our previous publication [26], the role of impact ionization is strongly dependent on channel scale, and exhibits two types of dependences on channel length and width. When the DCS is applied to the TFTs with a fixed channel length and different channel widths, the stronger impact ionization can be observed for the wider channel width TFT, leading to the high heating temperature. On the other hand, when the DCS is carried out on the devices with a fixed channel width and different channel lengths, the stronger impact ionization can be obtained for the shorter channel length TFT. Therefore, besides the proper  $T_{IGZO}$ , the a-IGZO TFTs with the relatively long length and short width may effectively minimize the impact ionization effect, improving the DCS-induced stability of the a-IGZO TFTs.



**Figure 9.** The schematic diagram of the mechanism of DCS-induced instability in the IGZO TFT with the  $T_{IGZO}$  value of (a) 25 nm and (b) 45 nm, 75 nm, or 100 nm.

#### 4. Conclusions

In this study, the initial electrical properties, PBS, and DCS-induced instabilities of a-IGZO TFTs with various  $T_{IGZO}$  are investigated. As the  $T_{IGZO}$  values increased, the  $V_{on}$  decreased, while the SS slightly increased because the total defect states and free carrier numbers were increased as the increase in the  $T_{IGZO}$ . It is found that the  $\Delta V_{on}$  under PBS is aggravated as the decrease in the  $T_{IGZO}$ , which is due to the enhancement of the vertical electrical field in the channel. In addition, the DCS-induced instability in the a-IGZO TFTs with various  $T_{IGZO}$  values is revealed by the combination of  $I-V$  and  $C-V$  measurements. The  $C-V$  results indicate that an anomalous hump phenomenon is only observed in the off state of the  $C_{gs}$  curve for all of the a-IGZO TFTs. This is because the impact ionization occurs near the drain side of the channel and the generated holes flow towards the source side along the back-channel interface under the lateral electric field, which causes a lowered potential barrier near the source side. Since the amount of free electrons increase with the increase in the  $T_{IGZO}$  values, the recombination probability of the generated holes and electrons are enlarged during the hole drifting, leading to the weakened hump phenomenon as the  $T_{IGZO}$  values increased. This study points out that material and fabrication engineering in the drain region should be well considered, even for the high-performance oxide TFTs.

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