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Implementation of a fully implantable middle-ear hearing device chip

Jyung Hyun Lee[a], Dong Wook Kim[b], Ki Woong Seong[c], Myoung Nam Kim[a] and Jin-Ho Cho[d,*]
[a]*Department of Biomedical Engineering, School of Medicine, Kyungpook National University, Daegu, Korea*
[b]*Gyeongbuk Branch Office, Korea Testing Certification, Daegu, Korea*
[c]*Department of Biomedical Engineering, Kyungpook National University Hospital, Daegu, Korea*
[d]*Institute of Biomedical Engineering Research, Kyungpook National University Korea, Daegu, Korea*

Abstract.
BACKGROUND AND OBJECTIVE: Recently, with the increase in the population of hearing impaired people, various types of hearing aids have been rapidly developed. In particular, a fully implantable middle ear hearing device (F-IMEHD) is developed for people with sensorineural hearing loss. The F-IMEHD system comprises an implantable microphone, a transducer, and a signal processor. The signal processor should have a small size and consume less power for implantation in a human body.
METHODS: In this study, we designed and fabricated a signal-processing chip using the modified FFT algorithm. This algorithm was developed focusing on eliminating time delay and system complexity in the transform process. The designed signal-processing chip comprises a 4-channel WDRC, a fitting memory, a communication 1control part, and a pulse density modulator. Each channel is separated using a 64-point fast Fourier transform (FFT) method and the gain value is matched using the fitting table in the fitting memory.
RESULTS AND CONCLUSION: The chip was designed by Verilog-HDL and the designed HDL codes were verified by Modelsim-PE 10.3 (Mentor graphics, USA). The chip was fabricated using a 0.18 μm CMOS process (SMIC, China). Experiments were performed on a cadaver to verify the performance of the fabricated chip.

Keywords: Fully implantable middle ear hearing device, wide dynamic range, CMOS process, Verilog-HDL, Cadaver experiment

1. Introduction

Recently, the population of hearing impaired people has increased, with many people suffering from hearing problems [1–4]. To deal with this problem, various types of hearing aids are being rapidly developed [5–16]. In particular, a fully implantable middle ear hearing device (F-IMEHD) is developed for people with sensorineural hearing loss. Otologics MET Carina^{TM} and Envoy Esteem are examples of F-IMEHDs [17–25]. The F-IMEHD system comprises an implantable microphone, a vibration transducer, and a signal processor [26–28]. In the design of the signal processor, the input and output characteristics, such as the output signal level of the microphone and the resonance frequency of the vibration transducer, must be considered. Furthermore, the signal processor should have a small size and low power consumption for implantation in a human body.

*Corresponding author: Jin-Ho Cho, Institute of Biomedical Engineering Research, Kyungpook National University, 680 Gukchaebosang-ro, Jung-gu, Daegu, Korea. E-mail: jhcho@ee.knu.ac.kr.

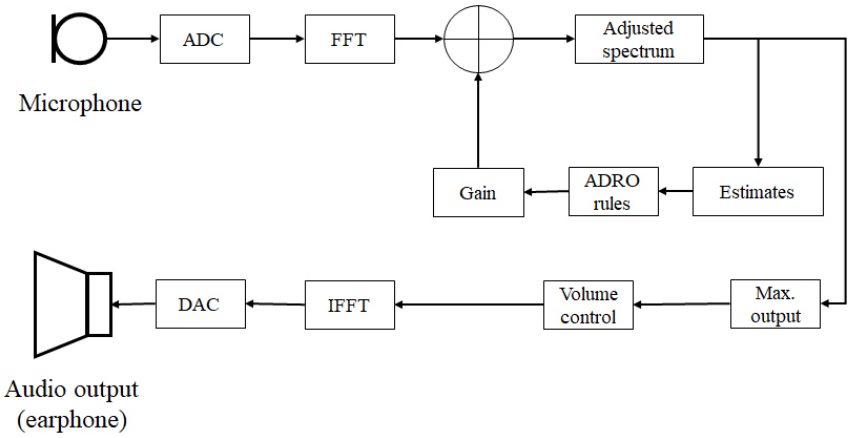


Fig. 1. Block diagram of WDRC using FFT [34].

The main function of the signal processor is to compensate for the hearing loss via amplification, filtering, and compression. Hence, the signal processor for the F-IMEHD must comprise a wide dynamic range compression (WDRC) algorithm and a wireless fitting function to effectively compensate for the hearing loss. The WDRC algorithm is a widely used compensation algorithm in digital hearing aids. The function of the WDRC is to incorporate an additional input range of 100 dB into the existing dynamic range of the user. The WDRC algorithm is employed because non-linear fitting algorithms are required for digital hearing aids [1–3,29–32]. The fitting algorithms are used to compensate for the hearing loss of a user. Hence, because the F-IMEHD is implanted in the human body, a wireless fitting function is employed.

Generally, the filterbank or fast Fourier transform (FFT) is used for WDRC algorithm [33]. The filterbank needs many band-pass filters for multi-channel WDRC. Moreover, the narrow band-pass filter that consists of FIR or IIR filter needs a lot of taps. The filter bank that consists of narrow band-pass filter has signal delay problems [34]. The flow diagram of signal processing of WDRC that use the FFT is shown as Fig. 1.

In this case, the FFT transmitted signal is needed inverse fast Fourier transform (IFFT) for conversion to time domain signal. The process of FFT and IFFT cause time delay and increase the system complexity. A time delay occurs corresponding to the window size, because it has to store and process the signal as much as the window size for the FFT and IFFT at one time. And, the complexity of the system increases by logic circuit for IFFT processing and memories for IFFT processing. So, the WDRC system that has a new signal processing method for low time delay and minimum complexity for low power consumption is needed.

In this study, we designed and fabricated a signal-processing chip using the modified FFT algorithm. This algorithm was developed focusing on eliminating time delay and system complexity in the transform process. The designed signal-processing chip comprises a 4-channel WDRC, a fitting memory, a communication control part, and a pulse density modulator. Each channel is separated using a 64-point fast Fourier transform (FFT) method and the gain value is matched using the fitting table in the fitting memory. The FFT algorithm was improved to reduce the computational complexity and the size of the memory. The output signal of the WDRC is converted to a pulse density modulation (PDM) signal using the designed pulse density modulator. The PDM signal is then interpolated four times to obtain a high-quality analog signal. The communication control part is designed to perform the wireless fitting and control.

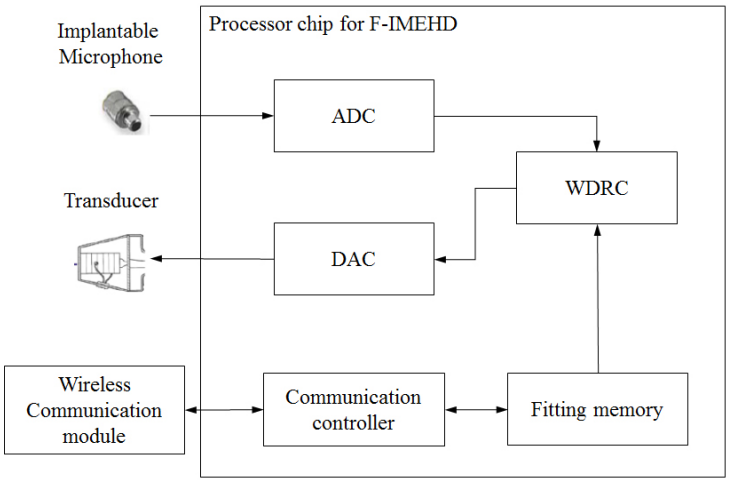


Fig. 2. Block diagram of the F-IMEHD.

The chip was designed by Verilog-HDL and the designed HDL codes were verified by Modelsim-PE 10.3 (Mentor graphics, USA). The chip was fabricated using a 0.18 μm CMOS process (SMIC, China). Experiments were performed on a cadaver to verify the performance of the fabricated chip.

2. Design and simulation of the processor chip

The design and verification of the processor chip were performed in three steps. In the first step, the FFT algorithm was modified, and subsequently, verified. In the second step, the chip was designed including the WDRC, fitting memory, communication control part, and pulse density modulator using the Verilog-HDL codes. In the third step, the designed HDL codes were verified by conducting a computer simulation. Figure 2 shows the block diagram of the processor chip used in the F-IMEHD.

The F-IMEHD comprises an implantable microphone, a transducer, and a wireless communication module. The implantable microphone receives the sound that the user wishes to hear coming from outside the body. The sound received by the microphone is then converted into an electrical signal and is inputted to the chip. The input signal is converted to a digital signal using an analog-to-digital convertor (ADC). The WDRC is used to compress and amplify the input signal based on the extent of hearing loss of the user. The compression and amplification criteria are determined using the fitting algorithm, which are recorded in the fitting memory. In an air-conduction type hearing aid, the fitting operation is performed via wire communication; however, a wireless communication is required for the F-IMEHD, because the components of the F-IMEHD are located in the body. The processed signal, based on the extent of hearing loss, is then converted to an analog signal and is inputted to the transducer. The vibration of the transducer allows the user to hear the appropriately amplified sound.

2.1. Modification of the FFT algorithm

Generally, the FFT or a filter bank is used to separate the frequency channels in the WDRC. The advantage of the FFT algorithm is that the signal delay time is less; however, the disadvantage is the high computational complexity. In contrast, the filter bank method exhibits low computational complexity and

long delay time. We suggest an FFT algorithm modified without using the phased information of the twiddle factor to reduce the computational complexity. The equation for an N point FFT can be expressed as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n) W^{nk}, 0 \leqslant k \leqslant N-1 \tag{1}$$

Here, N is the fundamental period of the sequence, the frequencies are $\{\frac{2\pi}{N}k, k = 0, 1, \ldots, N-1\}$, and $x(n)$ is the input value at the nth time. The twiddle factor is given as follows.

$$W^{nk} = \mathrm{e}^{-j\frac{2\pi}{N}nk} \tag{2}$$

The formula is inverse FFT, similar to Eq. (3) [35,36]:

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k) W^{-nk} = \frac{1}{N}\sum_{k=0}^{N-1}\left(\sum_{n=0}^{N-1} x(n) W^{nk}\right) W^{-nk} \tag{3}$$

The characteristics of the twiddle factor are the same as that expressed in Eq. (4).

$$W^{Nk+r} = -W^{Nk+\frac{N}{2}+r}, r = 0, 1, 2, \ldots N/2-1 \tag{4}$$

The input data $x(n)$ is real, in which case the outputs symmetric about $X(N/2)$ [37]. We calculated $X(k)$ from $k = 0$ to $(N/2) - 1$, and the imaginary values of the twiddle factor are set to zero. In this case, $x(0)$ is calculated using Eq. (5):

$$\begin{aligned} x(0) &= \frac{1}{\frac{N}{2}}\left(\sum_{k=0}^{\frac{N}{2}-1} X(k) - \sum_{n=0}^{\frac{N}{2}-1} x(2n+1)\right) \\ &= \frac{1}{\frac{N}{2}}\left[\sum_{k=0}^{\frac{N}{2}-1}\left(\sum_{n=0}^{N-1} x(n)\, Re\left(W^{nk}\right)\right) - \sum_{n=0}^{\frac{N}{2}-1} x(2n+1)\right] \end{aligned} \tag{5}$$

We designed a 64-point FFT module using the modified FFT algorithm. Hence, k ranged from 0 to 31, and only a simple summation was used in the inverse FFT calculation to obtain the value of $x(0)$. To verify the modified FFT method, a computer simulation was performed using MATLAB (MathWorks, USA). The FFT and IFFT results were calculated using the original and proposed methods. The results were compared up to 12 decimal places. Figures 3 and 4 show the simulation results.

The input signal was mixed comprising sinusoidal signals with magnitudes of 1.1 kHz and 177.8 mV and 3.7 kHz and 177.8 mV, as shown in Figures 3a and 4a. The bias point was 900 mV. In this simulation, the IFFT and cross correlation results of the original and proposed methods were similar.

2.2. Design and simulation of a signal processor

The designed processor comprises the WDRC, fitting memory, communication control part, and pulse density modulator. Figure 5 shows the block diagram.

The proposed FFT algorithm comprises 64 channels. Hence, the total input is designed to store 64 channels ranging from $x(0)$ to $x(63)$, as shown in Fig. 4. As the frequency of each channel is predetermined, the twiddle factor for the FFT operation is pre-computed and is stored for 32 values of each frequency channel. In the proposed FFT module, the FFT is performed using the proposed method and the result is outputted for each frequency channel. The output signals of each channel are summed to

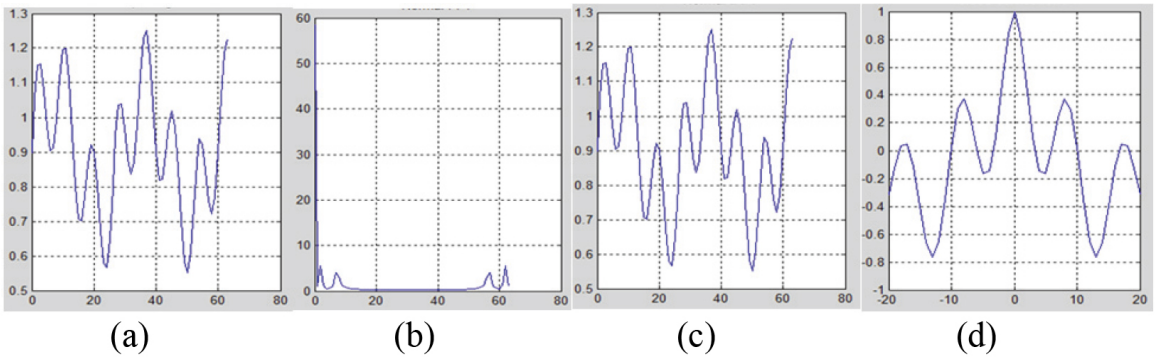


Fig. 3. Simulation results obtained using the original FFT method: (a) input signal, (b) FFT results using the original method, (c) IFFT results using the original method, and (d) cross correlation with input signal and IFFT results using the original method.

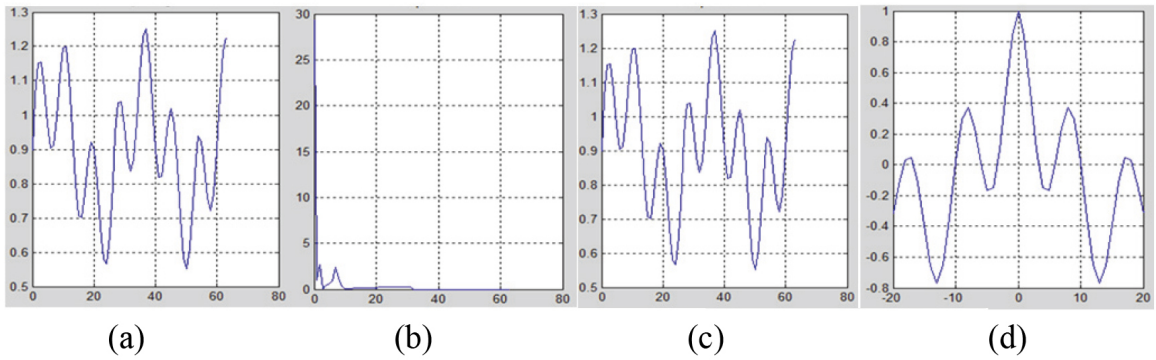


Fig. 4. Simulation results obtained using the proposed FFT method: (a) input signal, (b) FFT results obtained using the proposed method, (c) IFFT results obtained- using the proposed method, and (d) cross correlation with input signal and IFFT results obtained using the proposed method.

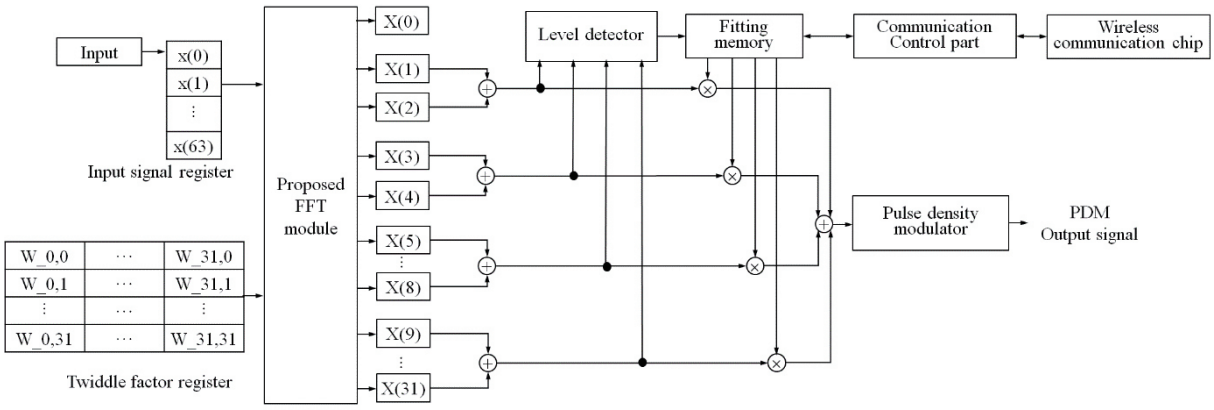


Fig. 5. Block diagram of the designed signal processor for the F-IMEHD.

determine the magnitude, based on which a suitable fitting gain is derived. The signals of each channel to which the gain is applied are summed using the proposed IFFT method. The final output signal is then

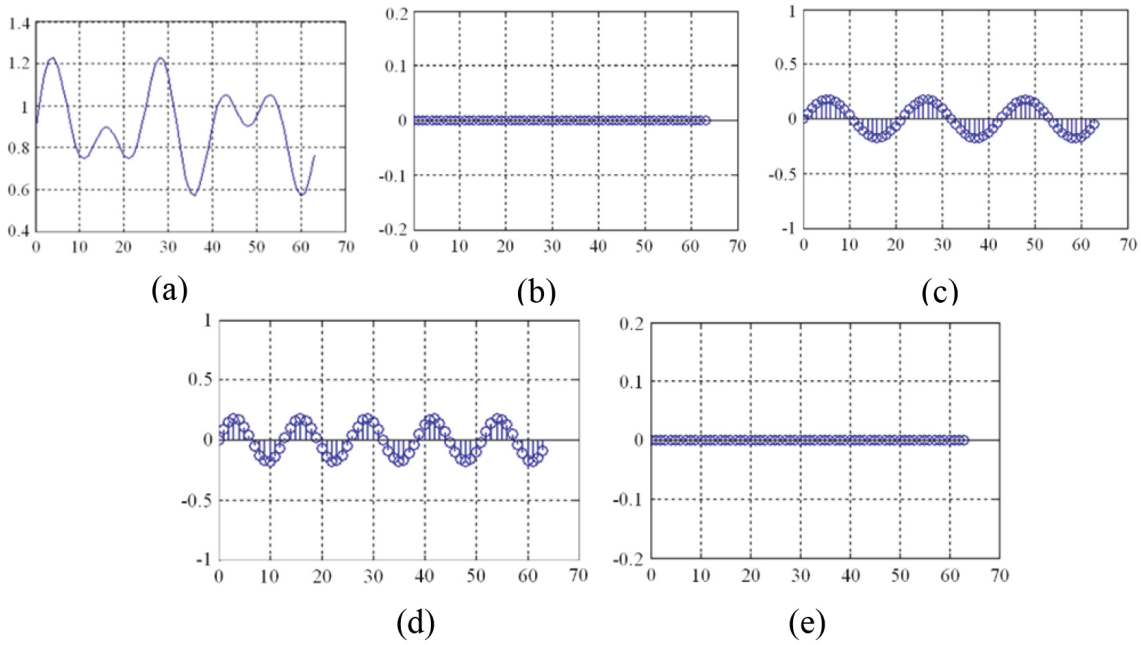


Fig. 6. Simulation results of channel separation: (a) input signal, (b) separated signal on channel 1, (c) separated signal on channel 2, (d) separated signal on channel 3, and (e) separated signal on channel 4.

converted to a PDM signal. The fitting gain values are stored in the fitting memory, which can be varied via wireless communication from the outside. To change the fitting gain values and control the functions of the chip, a communication control part is designed. The communications controller supports two wireless communication chips: TMS37157 (Texas instruments, USA) and nRF24L01 (Nordic semiconductor, Norway) [38,39].

The channels of the WDRC were divided into four based on the vibration characteristics of the electromagnetic transducer. The ranges of channels 1, 2, 3, and 4 were 0.1–1, 1.1–2, 2.1–4, and 4.1–8 kHz, respectively. The twiddle factors based on the frequency of each channel were calculated in advance and applied to the proposed algorithm. The channel segmentation, gain application, and time-domain signal restoration pertaining to the proposed algorithm were simulated using MATLAB (MathWorks, USA). Figures 6 and 7 show the simulation results.

The input signal was mixed comprising sinusoidal signals with magnitudes of 2.5 kHz and 177.8 mV and 3.5 kHz and 177.8 mV, as shown in Figs 6a and 7a. The bias point was 900 mV. In this simulation, the signals with frequencies of 2.5 and 3.5 kHz were separated into channels 2 and 3, respectively, as shown in Figs 6b–e. The gain of channels 1, 2, and 4 was 1, and the gain of channel 3 was 2. Figures 7d and e show the gains applied to channels 2 and 3. The IFFT signal obtained using the proposed method and the mixed signal comprising the sinusoidal signals (2.5 kHz, 177.8 mV and 3.5 kHz, 355.6 mV) were the same, as shown in Fig. 7b and c.

The PDM is a modulation technique in which an analog signal can be expressed in the form of a binary digital signal and is generally used as an output coding method for a hearing aid chip attached to a receiver or an electromagnetic transducer. In the designed signal-processing device, the sampling rate of the input signal is 32 kHz and the output signal of the proposed modified FFT method is also outputted at 32 kHz. Thus, the PDM signal outputted at 64 kHz is selected as the final output signal using a linear interpolation method.

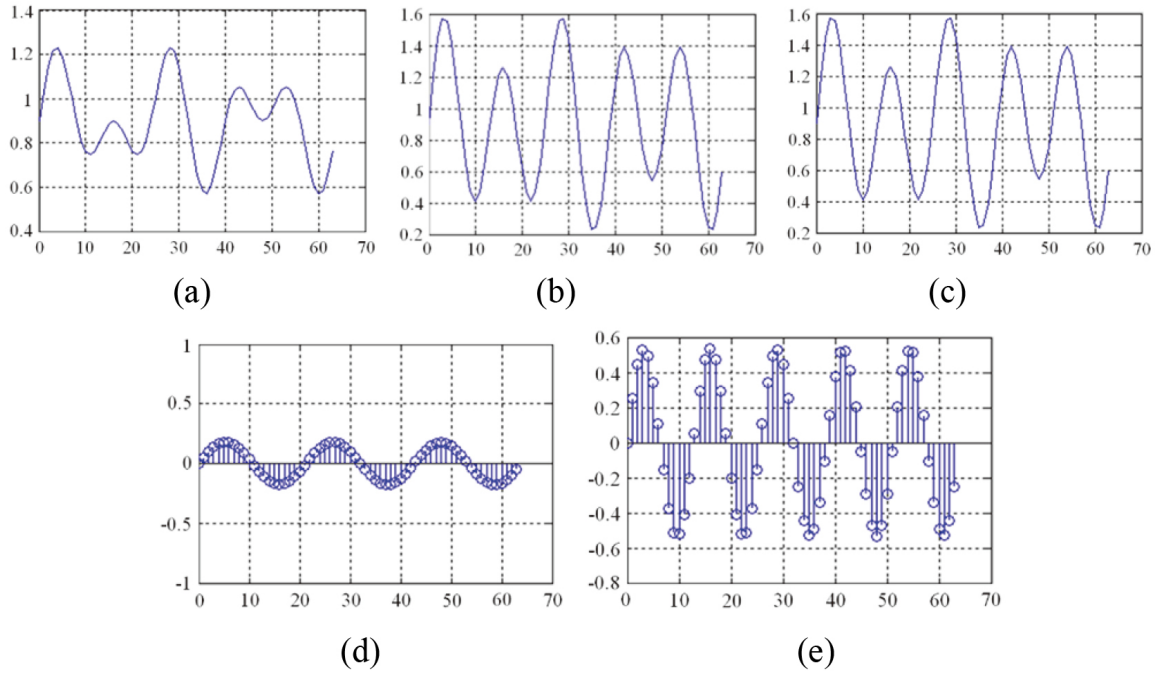


Fig. 7. Simulation results of gain-applied IFFT: (a) input signal, (b) result of applying gain to input signal, (c) result of gain-applied IFFT using proposed method, (d) gain signal applied to channel 2, and (e) gain signal applied to channel 3.

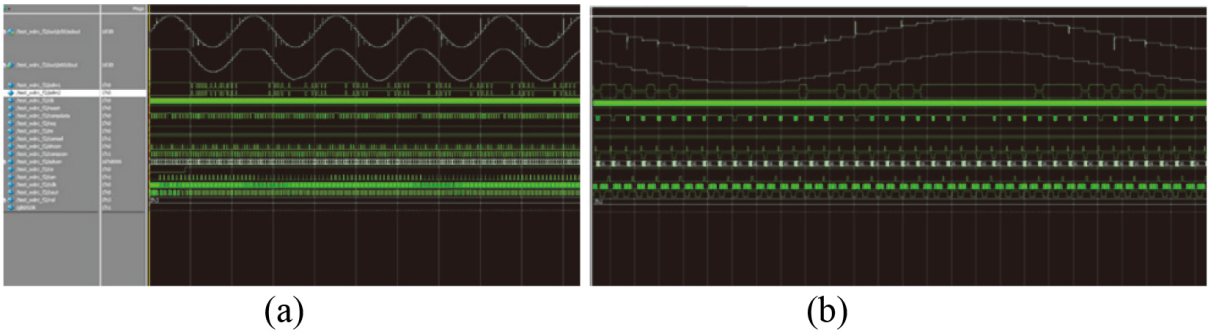


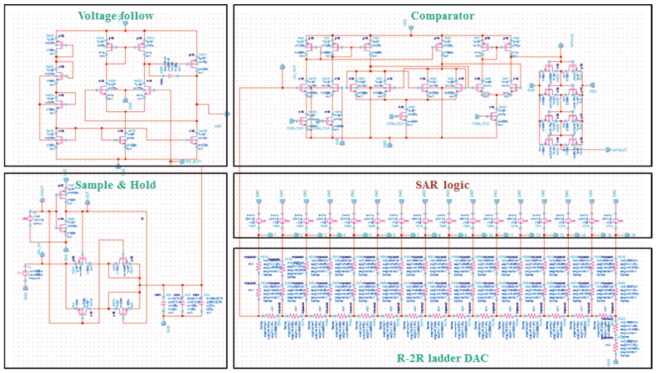
Fig. 8. (a) Simulation results of the designed processing chip, and (b) enlarged graph on time axis of (a).

2.3. Design and fabrication of the chip

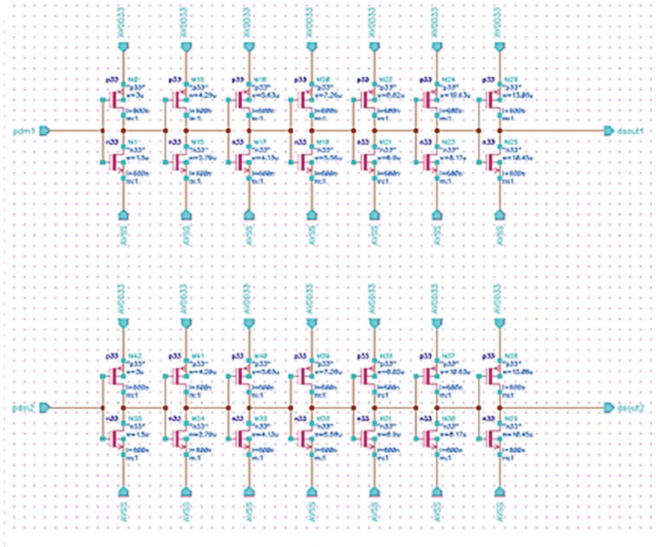
To fabricate the chip, the proposed processor was designed using Verilog-HDL codes. The design results of the Verilog-HDL were verified via simulation using Modelsim-PE 10.3 (Mentor graphics, USA). Figure 8 shows the simulation results.

The input signal is an ADC output signal for sinusoidal input of 1 kHz, 90 dBSPL and the gain of all channels is assumed to be 1. There was a time delay of 8 us as shown in Fig. 8a, but this is very short time compared to the time delay of other systems [40].

An SAR ADC and a class-D amplifier were inserted inside the fabricated chip for operating test of the designed processor. Figure 9 is the circuit of SAR ADC and class-D amplifier.



(a)



(b)

Fig. 9. The circuit of (a) SAR ADC and (b) class-D amplifier using Cadence spectre.

The designed SAR ADC include sample & hold, voltage follow, SAR logic and comparator as shown in Fig. 9a. The voltage follow used for voltage stabilization of sample & hold output. The class-D amplifier was designed to minimize propagation delays using a fixed taper buffer strategy. Figure 10 is layout of SAR ADC and class-D amplifier.

The SAR ADC and class-D amplifier were designed by Virtuoso (Cadence, USA). The size of designed SAR ADC was 124.9 $\times$ 152.1 um. The size of designed class-D amplifier was 36.0 $\times$ 36.7 um.

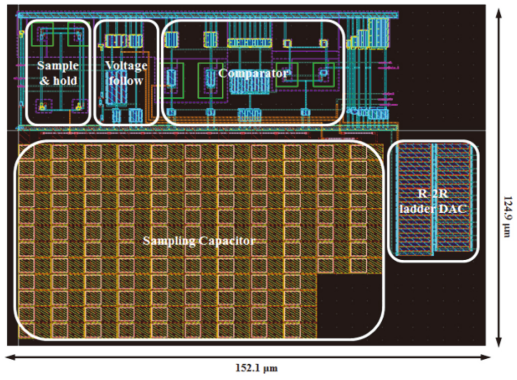
The digital processors designed with Verilog-HDL verified the logic algorithm using the Design Compiler (Synopsys, USA).

The processor chip was designed using Cadence EDA tools. The entire chip, including SAR ADC, class-D amplifier and WDRC, was designed by Virtuoso. Figure 11 is the layout of designed chip.

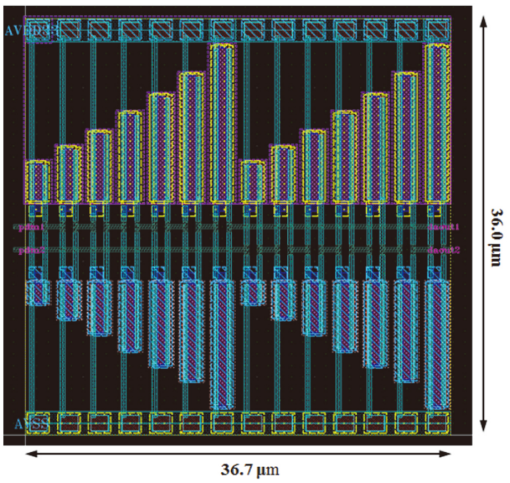
The chip was fabricated using a 0.18 μm CMOS process (SMIC, China). Figure 12 is the fabricated die chip and packaging chip. Figure 12a shows the fabricated die chip. Figures 12(b) and (c) show the packaged chip. Table 1 lists the specifications of the fabricated chip. The dimensions of the implemented die chip and packaged chip are 2.1 mm $\times$ 2.1 mm and 6.0 mm $\times$ 6.0 mm, respectively. The supply

Table 1
Specifications of the fabricated processing chip

Specification	Value
Die chip size	2.1 mm × 2.1 mm
Packaged chip size	6.0 mm × 6.0 mm
Number of gates	190,469
Supply voltage	
Core	1.8 V
Digital I/O	3.3 V
Analog	1.8 V
Power consumption of core (simulation)	0.13 mW
Total current consumption at maximum output	10 mA
Package type	48 pin QFN



(a)



(b)

Fig. 10. The layout of (a) SAR ADC and (b) class-D amplifier using Cadence Virtuoso.

voltage of the core was 1.8 V, the digital I/O voltage was 3.3 V, and the analog supply voltage was 1.8 V. The power consumed by the core was 0.13 mW obtained via simulation using Voltage Storm (Cadence, USA). The total current consumed by the implemented chip was 10 mA, including the core, digital I/O, analog part, and transducer.

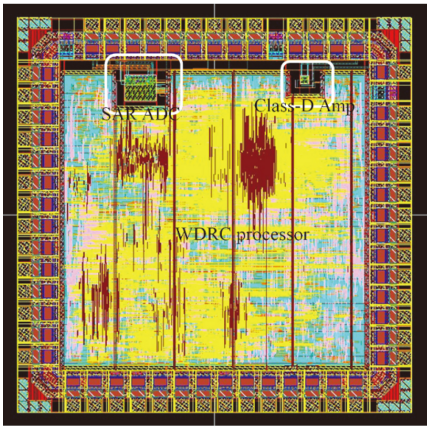
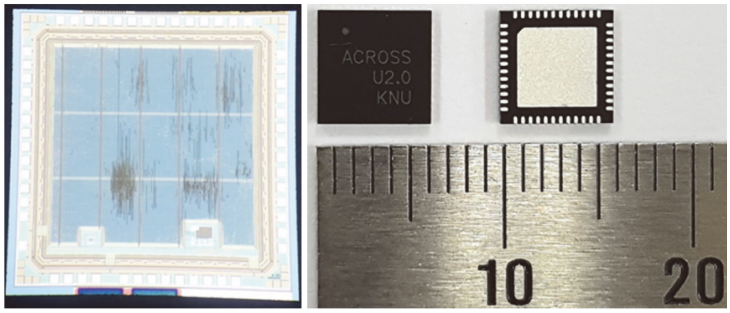


Fig. 11. The layout of designed chip using Cadence Virtuoso.



(a) (b) (c)

Fig. 12. (a) fabricated die chip micrograph, (b) top of packaged chip, and (c) bottom of packaged chip.

3. Experiments and results

3.1. Performance verification of the fabricated processor chip

To verify the performance of the fabricated chip, the vibration characteristics of the electromagnetic transducer were compared with the two input signals. One of the inputs was the signal outputted from the function generator and the other was the signal outputted from the proposed chip. A test board was prepared for the experiment. Figure 13a and b show the schematic and image pertaining to the chip performance experiment, respectively. Figure 14 shows the experimental results.

The output signal of the function generator (HP, 3310B) was sinusoidal with a peak of 300 mV. The vibration characteristics of the electromagnetic transducer were measured using a laser vibrometer (Polytec, OFV-2200). The vibration characteristics of the electro-magnetic transducer were similar when the output of the function generator was directly connected and when the PDM output of the proposed chip was connected.

3.2. Experiments on human cadaver

Experiments were performed on a human cadaver to verify the applicability of the fabricated chip on the implantable hearing device. The F-IMEHD prototype including the implantable microphone,

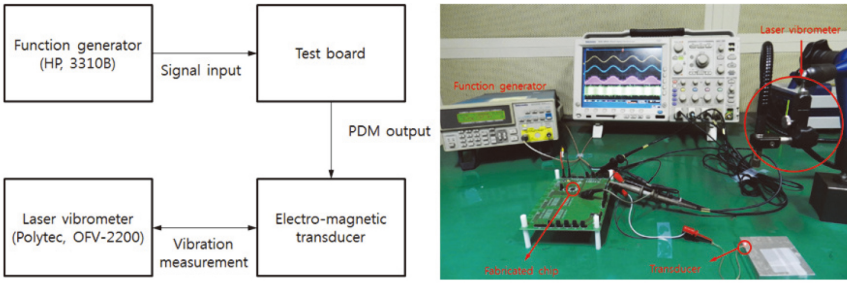


Fig. 13. (a) Schematic of the experiment, and (b) Image of the experiment.

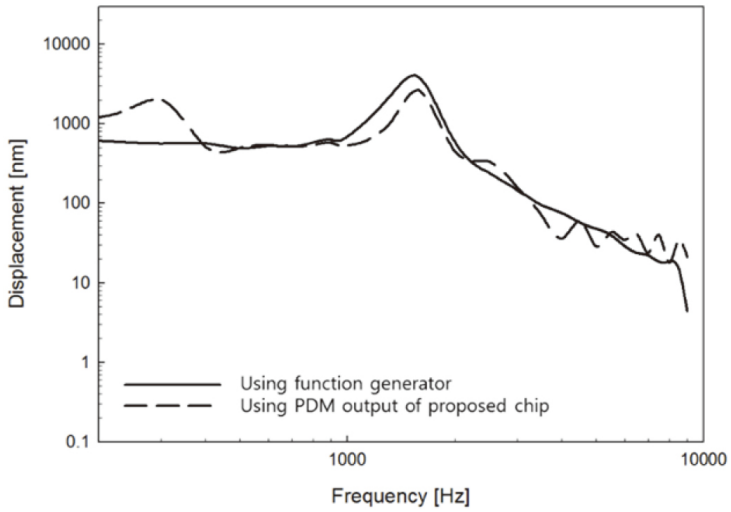


Fig. 14. Experimental results.

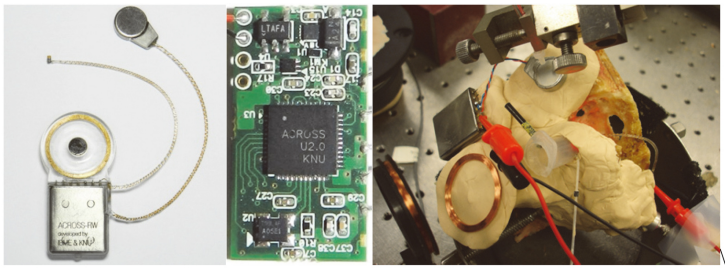


Fig. 15. Images of (a) prototype system, (b) minimized test board, and (c) human cadaver experiments.

electro-magnetic transducer, and minimized test board was placed on a human cadaver. Figure 15 shows the images of the implemented prototype and the experiment. Figure 16 shows the experimental results.

The baseline was the stapes velocity obtained via acoustic stimulation of 94 dB sound pressure level (SPL), as shown in Fig. 16a. The baseline measurement results were used to confirm that the proposed prototype, installed on the cadaver, functioned normally during the experiment. To confirm the normal

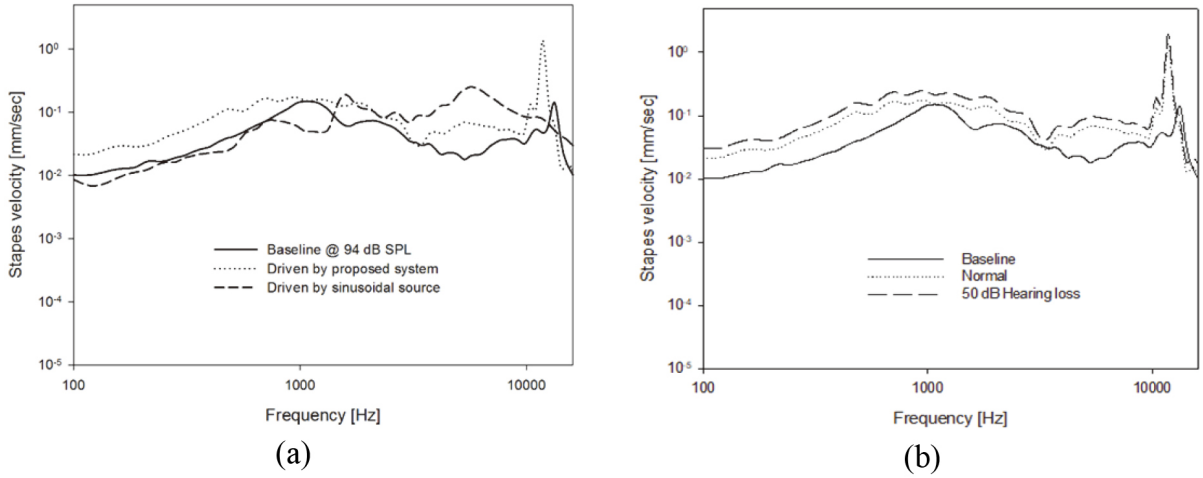


Fig. 16. Results of human cadaver experiments; (a) basic output characteristic with no gain, (b) comparison of gain characteristic for normal hearing loss and 50 dB hearing loss by FIG6 fitting rule.

operation of the implanted transducer, a sinusoidal signal was applied to the implanted transducer, and the stapes velocity was then measured. From this measurement, it was confirmed that the transducer was correctly implanted. Finally, the stapes velocity was measured using the implemented prototype. The results were confirmed to be similar to the stapes velocity produced via sound stimulation, sinusoidal signal, and output signal of the implemented prototype with 94 dB SPL input sound. In addition, we fitted the implemented chip for 50 dB hearing loss from 2 kHz to 10 kHz. The hearing compensation was calculated by FIG6 fitting rule. The FIG6 rule procedure specifies how much gain is required to normalize loudness, at least for medium-and hig-level input signals [1]. The stapes velocity increased about 3.02 dB as shown in Fig. 12b. The performance of implemented chip was confirmed from this experiment results.

4. Discussion and conclusion

This study designed and implemented a signal-processing chip with a small size and a low power consumption for the F-IMEHD system. The implemented chip comprises a multi-channel WDRC, a fitting memory, a wireless communication control part, and an output stage. A modified FFT algorithm was proposed for the WDRC. The digital system was designed using Verilog-HDL codes and verified using Modelsim-PE 10.3 (Mentor graphics, USA). The designed chip was implemented using a 0.18 μm CMOS process. The dimensions of the implemented die chip and packaged chip are 2.1 mm $\times$ 2.1 mm and 6.0 mm $\times$ 6.0 mm, respectively. Table 2 is comparison table to compare the performance of our chip with other studied chips.

Although many studies have been conducted on the implementation of low-power hearing aid processors, there is no study on the implementation of a processor chip for the F-IMEHD. Kim et al. [41] proposed a chip with a total power consumption of 107 μW. However, it cannot be applied to the F-IMEHD, because an ear canal modeling filter circuit was used in this study. Gata et al. [42] developed a mixed-signal hearing-aid chip using a CMOS process; they obtained a total current consumption of 270 μA at a supply voltage of 1.1 V under the no-signal condition. The power consumption of the chip proposed in this study is greater than that proposed in other studies, though the comparison is based under

Table 2
Comparison of the implemented chip with other studied chips

Chip	Kim's chip	Gata's chip	Lan Dai's chip	Our chip
Power consumption [μW]	107 (Except receiver)	270 (No signal condition)	89	33,000 (Maximum output)
Voltage [V]	0.9	1.1	1	3.3
Current [mA]	0.133	0.27	0.089	10
Chip size [mm^2]	3.744	12	1.127	4.41
Function block	ADC, DAC, DSP, Receiver driver	ADC, DAC, DSP, Receiver driver	OTA, Comparator, AGC	ADC, DAC, FFT, WDRC, Receiver driver, Wireless communication control

the state where the signal is not applied. And, Lan Dai et al. [43] has developed a small-size, low-power multi-frequency signal processor. Although the developed processor has a core size of only 1.127 mm^2, it contains only peak-statistical algorithm and judgment logic for multi-frequency signal application of AGC.

In this study, the simulation results show that the total current consumption was 10 mA at a supply voltage of 3.3 V with maximum output. Moreover, the current consumption of the core was 0.13 mW, including the operating current of the transducer. In the F-IMEHD, an electromagnetic transducer is generally used. The electromagnetic transducer comprises a permanent magnet and a coil. The resistance of the electromagnetic transducer is in the range of 50–300 Ω [44,45]. The current consumed by the electromagnetic transducer was approximately 10 mA, because the output signal of the implemented chip is a PDM signal with a magnitude of 3.3 V. Moreover, the resistance of the electromagnetic transducer was 300 Ω. The implemented chip includes a controller (consumes additional current) for wireless communication, which is not included in other studies. However, it is never low that the power consumption of core is 0.13 mW. Hence, further research is required on a low-power consumption design to reduce the same.

The experiments performed on the cadaver confirm that the implemented chip has sufficient functional performance. Therefore, the proposed processor can be implemented on a ASIC chip and helps in improving the performance of the F-IMEHD system. We are trying to carry out the human clinical trial to implant implemented hearing aids in the near future. It expected that the main research will be the study for performance improvement for recognition of speech using obtained human clinical trial data.

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Conflict of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

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