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Nano-engineered thin-film thermoelectric materials enable practical solid-state refrigeration

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Jake Ballard ¹, Matthew Hubbard ¹, Sung-Jin Jung ², Vanessa Rojas ¹, Richard Ung ¹, Junwoo Suh ², MinSoo Kim ², Joonhyun Lee ², Jonathan M. Pierce ¹ & Rama Venkatasubramanian ¹ □

Refrigeration needs are increasing worldwide with a demand for alternates to bulky poorly scalable vapor compression systems. Here, we demonstrate the first proof of practical solid-state refrigeration, using nano-engineered controlled hierarchically engineered superlattice thin-film thermoelectric materials. With 100%-better thermoelectric materials figure of merit, ZT, than the conventional bulk materials near 300 K, we demonstrate (i) module-level ZT greater than 75% and (ii) a system-level refrigeration ZT 70% better than that of bulk devices. Thin-film thermoelectric modules offer 100-300% better coefficient-of-performance than bulk devices depending on operational scenarios; system-level coefficient-of-performance is ~15 for temperature differentials of 1.3 °C. The thin-film devices enable more heat pumping per P-N couple, relevant for distributed and portable refrigeration, and electronics cooling. Beyond the demonstration of nano-engineered materials for a systemlevel advantage, we utilize 1/1000th active materials with scalable microelectronic manufacturing. The improved efficiency and ultra-low thermoelectric materials usage herald a new beginning in solid-state refrigeration.

Refrigeration needs in scaled down systems for essential refrigeration demand alternates to conventional mechanical refrigeration systems for worldwide applications. Refrigeration needs are increasing in both the developed and developing world, particularly in scaled down <100-Watt to a few Watt systems for refrigeration in home to hospital environments. There is a significant need to make refrigeration devices more compact, efficient when scaled down in size from a large system, and also meet higher efficiency standards while lowering manufacturing costs. Conventional mechanical refrigeration systems do not scale well and also present environmental concerns due to the use of chemical refrigerants like Hydrofluorocarbons (HFCs)—they are greenhouse gases (GHGs) that can have a global warming potential (GWP) that is 700 to 4000 times greater than carbon dioxide (CO₂), with leak rates worsening the problem.

In contrast, solid state thermoelectric systems scale very well, from a 1-Watt to 1-kW level, because they are made of solid-state device components. We can add less or more thermoelectric devices depending on the cooling need, just like Li-ion battery systems - from a few Watts in our mobile phone to a multi-kilowatt system in an electric vehicle. Further, solid state devices are proverbially reliable because there are no moving parts and the cost can be decreased to competitive levels, as scalable semiconductor fabrication technologies can be applied.

Thermoelectric cooling modules stand out as an ideal cooling technology for scaled-down systems due to their ability to provide environmentally friendly cooling without the need for refrigerants, along with precise and rapid temperature control using only simple components. Thermoelectric cooling refrigerators provide significant benefits, including fast response times, accurate temperature

¹Johns Hopkins University Applied Physics Laboratory (JHUAPL), Laurel, MD, USA. ²Samsung Research, Samsung Electronics, Seoul 06765, Republic of Korea. E-mail: rama.venkatasubramanian@ihuapl.edu

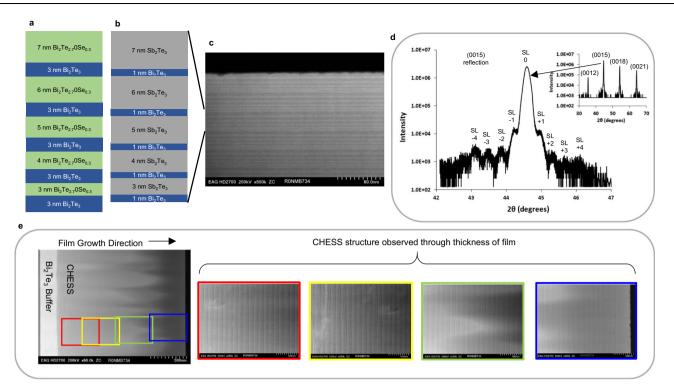


Fig. 1 | **CHESS structure in P- and N-type thin film materials. a, b** Schematic of CHESS structures in P- and N-type materials; **(c)** exemplar TEM cross-section data; **(d)** hi-resolution XRD data of the (0015) reflection showing the CHESS periodicity

matching with the TEM data and the wider 2Θ - ω scan (30–70°) inset showing the c-plane orientation in the epitaxial film; (e) Detailed TEM data through the thickness of the CHESS film indicates uniformity.

regulation, and remarkable temperature consistency. These characteristics greatly reduce the time needed to achieve the desired temperature and improve the uniformity of temperatures within the refrigerator. Consequently, they can enhance the preservation and freshness of food stored for extended periods. Furthermore, the simple design of the system offers flexibility, enabling the creation of innovative cooling appliances with new shapes and partitioning, paving the way for advanced refrigeration technology.

To our knowledge, while major advances in materials ZT has been reported¹⁻⁵ at various operating temperatures over the last two decades, in both thin-films and bulk materials, there have been limited device results⁶⁻¹⁰ to validate the performance of the improved materials with targeted or unique applications. Thin-film thermoelectric cooling (TFTEC) device technology demonstrated >1 kW/cm²-level hotspot cooling of single-core microelectronics in 20096 but the wider application has been hampered by the movement of chip designers to multi-core architectures and thereby significantly changing the thermal requirements at the chip level. We have recently demonstrated that CHESS TFTEC technology can be applied for creating thermal sensations for haptics in augmented reality and prosthetics for amputees' quality-of-life enhancement⁷. The reported advances in bulk materials' ZT have seen some limited translation into real device advancements in power generation¹¹⁻¹⁴ although there is still significant work to be put into commercial practice. The limited device results and consequential commercial relevance have significantly impacted new materials science developments in the thermoelectrics area in the past decade, in spite of the fact that solid-state refrigeration and similarly, solid-state heat-to-electric conversion would have enormous impact for energy efficiency and environmental relief. Here we report, nano-engineered TFTEC materials and device technology, through demonstrating solid state refrigeration capability in a commercial scale unit, showcasing the value of thermoelectric material advances into real-world, large-volume, energy-efficiency-relevant practical application.

Specifically, we demonstrate that TFTEC modular devices are ready for mainstream refrigeration applications. Towards that goal, using CHESS material ZT with -100% better than the bulk materials near 300 K, we demonstrate a system-level refrigeration ZT almost 70% better than bulk TE in the same configuration during significant heat pumping in conventional refrigeration. Under low-heat-pumping, with minimal role of parasitics, TFTEC modules offer four times the Coefficient of Performance (CoP) advantage over bulk devices. As an example, system-level CoP with a 16-couple TFTEC module is - 15 for small temperature differentials of 2 °C, pumping about 1.2 W heat load using 80 mW of electric power. Such small-scale high-CoP cooling is relevant for distributed refrigeration or compartmentalized refrigeration as well as for use in future electronic thermal management. 15-17.

Results

We use controlled hierarchically engineered superlattice structures (CHESS) grown by metal-organic chemical vapor deposition (MOCVD) in the p-type Bi_2Te_3/Sb_2Te_3 materials system and n-type $Bi_2Te_3/Sb_2.7Se_{0.3}$ materials system. Figure 1 shows the schematic of the specific structures used for the p-type (Fig. 1a) and n-type (Fig. 1b) materials, an exemplar transmision electron microscopy (TEM) data for the p-type CHESS (Fig. 1c) and corresponding hi-resolution x-ray diffraction (XRD) of the (0015) reflection and the wider $2\Theta-\omega$ scan ($30-70^\circ$) inset from the corresponding structure (Fig. 1d). The inset of the wider angle scan shows only ($00\ l$) reflections indicating the c-plane orientation of the single crystal epitaxial film. The intended periodicity of the CHESS structure is evident from the high resolution scan of the (0015) reflection, where multiple satellite reflections corresponding to the targeted CHESS structure are observed. In Fig. 1e, we show that the high-quality TEM cross-section image is evident through the thickness

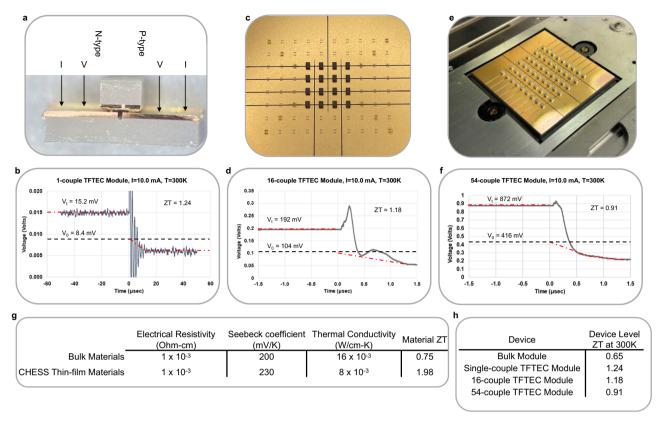


Fig. 2 | 300 K device level thermoelectric figure of merit (ZT) measured by Harman method. a ZT is measured at the individual P-N couple in a 4-wire configuration and (b) transient showing ZT - 1.24 in a single couple; (c) 16-couple

TFTEC module and (**d**) transient showing module ZT - 1.18; (**e**) 54-couple TFTEC module and (**f**) transient showing module ZT - 0.9. Material properties of CHESS and bulk TE materials are compared in (**g**) and measured device ZT in (**h**).

of the CHESS film, supported by the satellites observed in the XRD data (Fig. 1d) as well.

We have carried out frequency domain thermo-reflectance measurement of thermal conductivities in both the P- and N-type CHESS films, showing significant reduction in lattice thermal conductivities better than in single-period superlattices^{18,19}, and the p-type ZT and n-type ZT determined from material properties range from >2 in P-type CHESS and ~2 in N-type CHESS materials, more than 100% better than 300 K ZT of bulk TE materials used in current commercial off the shelf (COTS) device technology. The dominant reason for the improved materials ZT comes from the lower thermal conductivities of the CHESS materials, for about the same electrical conductivity as bulk TE materials. The lower thermal conductivities of CHESS materials have been validated by both time domain thermo reflectance (TDTR) at University of Virginia¹⁹ and frquency domain thermo-relectance (FDTR)²⁰ at JHU-APL discussed in Supplmentary Note 1. FDTR data measurement of thermal conductivities in both P-type and N-type CHESS thin-film materials, getting close to an average of ~8 mW/cm-K mentioned in ref. 7, are shown in Supplementary Fig. 1. The translation of these improved properties and materials-level ZT into device-level ZT of TFTEC modules is decribed next in Fig. 2.

While high material P-type and N-type ZTs have been reported⁷, the p-n couple and module ZT with such materials had been limited to about 0.94⁷ as measured by the Harman method. This method is using the quasi-steady state followed by turning off the current flow to detect the voltage developed from a temperatre gradient under adiabatic conditions described in deatil^{1,7,21}. The details of the ZT measurement methodlogy are further described in Supplementary Note 2. In this work, we have reduced the electrical sheet resistance of the traces as well as the connecting common header through the use of thicker Cu (~200 microns vs. 30 mcirons) interconnects with the

P-type and N-type CHESS thin-film materials into p-n device couples. Each P-N couple is a die of 1.2 mm \times 1.2 mm \times 1.0 mm and constists of two p-n couples with an AlN header connecting the p-n couples (Fig. 2a, b). The couples in the array were connected electrically in series using gold (Au) coated copper (Cu) traces on the AlN substrate. Each p-n couple is sandwiched between AlN headers and connected electrically in series using contact metallization of the CHESS semi-conductors creating a wide range of modular arrays like a 16-couple array (Fig. 2c, d) and a 54-couple array (Fig. 2e, f), showing the flexibility to scale up to larger heat pumping.

The CHESS TFTEC P-N couple ZT has been measured to be as high as 1.24 at 300 K (Fig. 2a, b); this is almost 65% better than typical P-N couple ZT of ~0.75 observed in bulk P-N couples at 300 K. For refrigeration applications, depending on the heat load, we need multicouple modules. Towards that objective, we have attempted a range of TFTEC modules, containing a few couples (16-couples) to 54 couples to as many as 80-couples. The builds of such multi-couple module arrays are scalable using automatic pick-and-place tools commonly utilized in the microelectronic chip fabrication. It is exciting that a 16-couple TFTEC module offers a ZT of ~1.18 at 300 K (Fig. 2c, d), almost 78% better than a bulk module array commercially avialble with a ZT ~ 0.65 at 300 K⁷. Note this ZT of ~1.16 at 300K, for a 16-couple TFTEC module, is about 23% better than a ZT ~ 0.94 reported for a 12-couple TFTEC module more than a year ago⁷ due to the reduction of parasitic electrical resistances. As the TFTEC module is scaled up, for increased heat pumping, to 54-couples (Fig. 2e, f) the ZT of the TFTEC module ranges about 0.91, about 53% better than COTS multi-couple module. We have scaled up the TFTEC module builds to 80-couples (Supplementary Fig. 2), with an estimated ZT ranging between 0.85 and 0.95, and validated by IR-imaging of cooling at the individual die level. As the devices scale from single-couple to 16 couple module, there is some

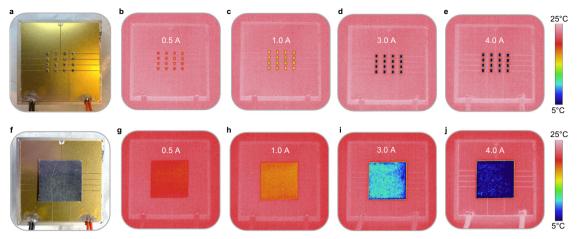


Fig. 3 | HAF-LIOF capability of TFTEC dies to cool large-area with minimal number of P-N couples. The implementation of HAF-LIOF allows high heat flux through the active thin-film thermoelectric P-N couple while achieving low input heat flux from the refrigeration compartment and similarly low output heat flux rejected to the heat-sink. This implementation is shown as a function of current

(0.5 A, 1.0 A, 3.0 A and 4.0 A) at the die-level of the module (**a**-**e**) and with a common heat-spreader (**f**-**j**). This approach also allows for the minimization of TE materials usage and simpler heat-source and heat-sink requirements, needed for cost-effective solid-state refrigeration.

variation in In-bumping from P-N couple to P-N couple, that lowers the ZT from 1.24 to 1.18 (Fig. 2h). Similarly, when we carry out an assemblage of larger P-N couples, such as a 54-couple TFTEC module, the ZT drops a little further to 0.94. The variation is mainly due to the variation in resistance of the Indium bump [Ref. 7, Extended data Fig. 2a] with the process at 175 °C, implemented for a larger assemblage of dies; with further advancements in packaging of the TFTEC module, we expect the ZT values to be maintained in larger modules.

We have shown the value of the TFTEC in offering high cooling power density in hot-spot cooling⁶ and also the benefit of both high cooling power density and faster cooling speed in creating thermal sensations in haptics and prosthetics⁷. The higher cooling density can also be utilized to achieve a range of refrigeration capacity with much smaller number of P-N couples and limited materials usage, by controlling the packing fraction of cooling dies per unit area and utilizing an appropriately sized common header using the concept of High Active Flux, Low Input-Output Flux (HAF-LIOF).

The cooling power density achievable in a TE device is given by the relation (1)

$$q_{max} = \frac{1}{l} \left\{ \left[\left(\frac{1}{2} \frac{\alpha^2 T_c^2}{\rho} \right) \right] - \left[k \left(T_h - T_c \right) \right] \right\}$$
 (1)

where q_{max} is the maximum cooling power density, l is the thickness of TEC device (see Supplementary Note 3 for full derivation). T_c is the cold-side (refrigeration cold-source) temperature, α is the Seebeck coefficient, ρ is the resistivity of thermoelectric (TE) material, k is the thermal conductivity of the material and T_h is the hot-side (heat-sink) temperature. For about the same ρ , T_h , and T_c , q_{max} is significantly higher in TFTEC devices, compared to the conventional thermoelectric devices. This difference q_{max} is largely due to the reduction of l (25 μ m in TFTEC vs. mm thick in bulk) and to a smaller extent from lower k for about the same α and ρ , due to the higher thermoelectric figure of merit in CHESS materials. The capability of the sparsely populated P-N couple array for large area cooling can be understood with the IR imaging shown in Fig. 3, at the individual P-N couple level and with a common header. The IR-imaging at the discrete die-level within a TFTEC module can be used to track the improved ZT measured by Harman method (see Supplementary Fig. 3). The applicability of the HAF-LIOF concept (described further in Supplementary Note 4 and shown schematically in Supplementary Fig. 4) is extendible to larger

array modules such as 80-couple TFTEC modules and higher, for higher cooling needs.

Ahead of refrigeration tests on TFTEC modules as well as on reference bulk TE modules, Samsung team carried out detailed modeling on heat flow based on the design outlined in Fig. 4. To estimate the total heat load of thermoelectric refrigerator (Samsung, CRS25T950005W) during operation²²⁻²⁴, we calculated it as the sum of the heat loads across temperature differences of each wall of the refrigerator, as illustrated in Fig. 4a. The thermal resistance of the refrigerator walls were modeled as the combination of three serial thermal resistances: natural convection heat transfer from the atmosphere, thermal conduction through the insulation wall, and convection heat transfer within the refrigeration chamber (Fig. 4b). The convective heat transfer coefficients for the external atmosphere and the internal refrigeration chamber were assumed to be h_0 , $8 \text{ W/m}^2 \cdot \text{K}$ and hc, 5 W/m²·K, respectively. The effective thermal conductivity of insulation was determined using standard thermal conductivity values for each component, including the casing, polyurethane insulation, and glass. (Fig. 4c). The schematic of the details of the integration of the TFTEC module are captured in Fig. 4d-f. The mathematical relations used to calculate heat flow from outside to the inside of the refrigeration chamber are described in Supplementary Note 5.

The refrigeration tests allow for the determination of system-level ZT of the bulk and TFTEC modules, using the power input that is required to achieve certain chamber temperature, as well as the CoP of the modules when the heat load is rather small and therefore independent of the number of couples in the module. The system-level ZT speaks to the quality of the TE technology when significant heat pumping is achieved, notwithstanding some issues involved in the integration of early-stage TFTEC technology. The CoP at small ΔT speaks to the potential intrinsic capability of the modules. The power input to the TE module is easily determined and the heat flow is known from both modeling and experimental measurements in Samsung labs (see Supplementary Note 5). The refrigeration characteristics of the conventional bulk TEC and a range of TFTEC modules are shown in Fig. 5. For comparison of the TFTEC modules and the bulk TEC modules, the same refrigeration test system, integration procedures and test methodologies were employed. The analytical relations derived from canonical energy balance in a TE cooling device to extract system-level ZT from the measured refrigeration data and the relationship between measured ZT and CoP are discussed in Supplementary Notes 6 and 7, respectively. Additional data in control bulk

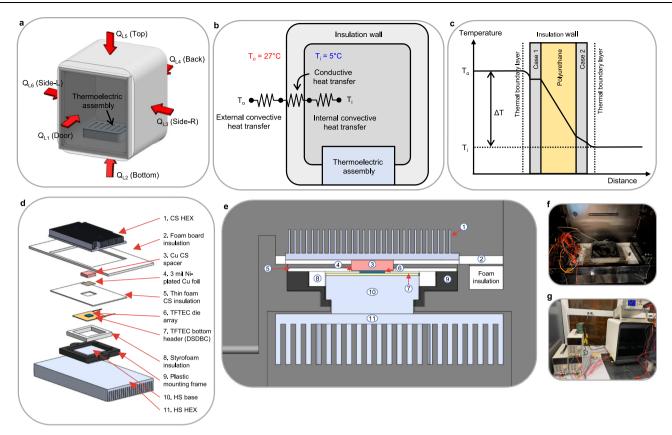


Fig. 4 | **Thermal modeling and implementation of TFTEC modules into a refrigeration system. a** Heat flow into the refrigeration system was considered from all the six sides of the refrigerator; **(b)** thermal circuit used for calculating the

heat load from each face of the refrigeration unit; (\mathbf{c}) qualitative temperature profile through the insulation wall; (\mathbf{d} - \mathbf{g}) details of the TFTEC module integration into the refrigeration system.

modules are provided in Supplementary Fig. 5 in two refrigeration configurations.

A 241-couple bulk TEC showed a system-level ZT ~ 0.62, while the 1st 80-couple module showed a system-level ZT of ~0.71, a 15% improvement. Next, a 77-couple TFTEC module, where three of the inferior dies from an 80-couple module were removed, demonstrated a system-level ZT of 1.05, almost a 70% improvement compared to the bulk technology. The refrigeration data, the heat-pumped per couple and other parameters are also summarized in Fig. 5. There is a good correlation between the system-level refrigeration ZT and the intrinsic parameters at low-current / low heat pumping CoP. We note that the heat pumped per p-n couple is a complex function of several parameters, including the temperature differentials; hence, the purpose of this data is to show the intrinsic advanatges of the CHESS TFTEC technology.

We noted earlier, how the In-bumping process variation in the assembly of large die (54 to 80 couples) modules affect the observed ZT (Fig. 2h). After the TFTEC module build, but prior to integration in the refrigeration system (Fig. 4d, e) of the 80-couple module, we have the ability to measure the individual resistances of each couple. In general, the inferior dies (meaning higher electrical resistance) result from inferior In-bumping process in the assembly of the TFTEC module. When we removed the three inferior dies, and made the 80-couple module to a 77-couple module, the ZT improved from -0.95 and the refrigeration system-level ZT was measured as high as -1.05, as discussed above.

The validity of the approach of extracting system-level ZT and key device parameters from the refrigeration data was carried out with two similar bulk modules in two different refrigeration configurations, using the same refrigerator implying similar heat loads. We obtained

similar coefficients (for the square and linear terms for the ΔT -vs-I relationship in Fig. 5a) and hence similar system-level ZT. The data is included in Supplementary Fig. 5.

The TFTEC modules are integrated deep into the refrigeration system as shown in Fig. 4d, to enable refrigeration, and the focus has been on the measurement of temperature difference between the ambient and the inside of the refrigeration chamber. Since the TFTEC modules pump heat from the refrigeration chamber, any measurement of temperature at two ends of the TFTEC module will be under load. However, in an earlier publication⁷, as part of extended data Fig. 4a, we have measured cooling across CHESS TFTECs of as much as ~69 K under no thermal load. The CHESS TFTECs intended for refrigeration, here, are designed for higher current operation and more heat-pumping. Also, the intrinsic large temperature differential across the TFTEC allows parasitic thermal drops across hot-side and cold-side heat-exchangers, thermal interfaces, and still obtain efficient refrigeration inside the chamber.

We also investigated a 4×4 TFTEC module with a Harman ZT of 1.16 in the refrigeration mode. The data is shown in Supplementary Fig. 6, and we can observe the correlation between enhanced ZT and CoP at low current levels. We note that the system-level CoP with a 16-couple TFTEC module is -15 for small temperature differentials of 1.3 °C, pumping about 1.2 W heat load with 80 mW of electric power, with more heat load per P-N couple. This is relevant for portable and distributed refrigeration, in addition to packaged electronics thermal management. In 4×4 TFTEC arrays (Supplementary Fig. 6) with a module ZT of 1.16, we observe a small-current/small-load CoP of 300% higher than observed for a bulk module (i.e., CoP of -25.7 vs. 5.9). The analytical relationship between the measured ZT and CoP is derived in Supplementary Note 7 to explain the measured data in two bulk

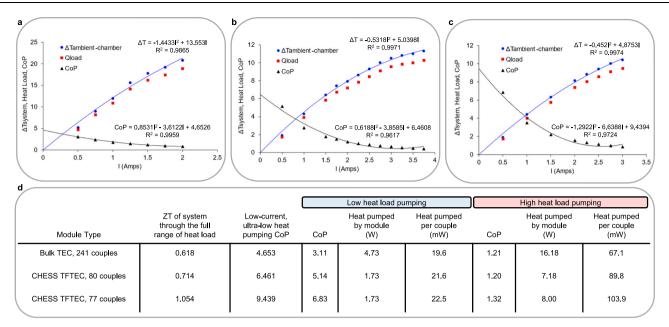


Fig. 5 | **Measured thermoelectric refrigeration characteristics.** Refrigeration data from **(a)** Samsung-provided bulk TEC module with 241 couples and **(b, c)** two exemplar 80-couple and 77-couple TFTEC modules. All the three modules were evaluated in the same configuration shown in Fig. 4d-f. The system-level

refrigeration data extracted include: (d) ZT for the bulk TEC module, a medium-performance 80-couple TFTEC module and a higher-performance 77-couple TFTEC module are -0.62, 0.71, and 1.05, respectively. CoP and heat pumped at the module and at the couple level are shown for the various modules.

modules and several higher-ZT TFTEC modules in Supplementary Fig. 7a. General relationship between CoP (at the limit of low heat pumping conditions from refrigeration tests) to the measured module ZT is consistent with the enhanced ZT in TFTEC directly translating to high CoP that is achievable in low-level heat pumping due to less impact of heat exchangers and number of couples. The relative variation of Z and ZT of CHESS TFTEC P-N couple, as a function of temperature between 300 K to as low as 220 K, is shown in Supplementary Fig. 7b. We observe that the nano-engineered CHESS materials allow the preservation of ZT over a substantial temperature range. The slight improvement in Z, as a function of temperature, is evident in the observed increase in CoP in going from ambient temperatures of ~29.3 °C to ~23.1 °C for several cases of heat-pumping in the actual refrigeration system with the TFTEC modules in Supplementary Fig. 7c. These results also indicate translatability of improved CHESS materials performance to refrigeration results.

Since the 77-couple TFTEC module offered a higher system-level ZT relative to the COTS bulk TEC technology, we carried out a continuous 24-h operational assessment (Supplementary Note 8) at a steady state current of 3 Amps; the data is shown in Supplementary Fig. 8a. A 16-couple module was tested for -100 h and the data is shown in Supplementary Fig. 8b. The sustained operational stability at higher current levels can be undertood from device-level electrical contacts. The typical CHESS device structure with Ni/Au electrical contacts on either end of the CHESS material is shown in Supplementary Fig. 9a. Additionally, a zoomed-in-view of the crystalline cross-sectional structure shows the presence of covalent bonds in the plane and Van der Waals gaps in the cross-section (Supplementary Fig. 9b). Thus, any possible diffusion of Au is prevented by the presence of both the Ni diffusion barrier as well as the strong covalent networks in the plane of the film adjacent to the electrical contacts.

More long-term tests are needed with improved packaging of the TFTEC module-based refrigeration technology. In early studies, the TFTEC modules like those shown in Fig. 2c, e, in other tests²⁵ have withstood vibration tests to 35 G_{rms} and shock tests to as much as 350 G_{rms} , making them suitable for space launch requirements and certainly rugged enough for household and commercial refrigeration

applications. Further advances in engineering scale-up, packaging, robust manufacturing, and robotic integration into the refrigeration system, without significant manual handling, should enable long-life operation in household, hospital, laboratory, commercial and industrial refrigeration as well as in space environments.

Discussion

The unique combination of high capacity and high-performance thermoelectric cooling with TFTEC modules prepared with nanoengineered CHESS materials has been demonstrated in solid state refrigeration in this study. This development is significant because it demonstrates that newly developed and nano-engineered thermoelectric materials can be transitioned to applications that are of potential large volume. Due to the compactness, reduced energy consumption, thermal power density, and speed of the TFTEC device, future HFC-free, GWP-free refrigeration could be achieved. We have demonstrated useable refrigeration with as few as 16 P-N couples in a TFTEC module for potential applications in small scale (5 W) refrigeration unit. Such a modular capability within a refrigerator can be attractive for overall system-level energy efficiency. The developments with CHESS TFTEC devices will meet some of the key requirements for emerging and future refrigeration-such as compactness, scalability, low materials usage, reliability, performance, and low manufacturing cost. The results presented in this paper represent an initial but important step in the journey to demonstrating and validating advanced higher ZT materials for efficient and practical solid-state refrigeration.

The paradigm changes that TFTEC devices, with nano-engineered epitaxially grown materials -25-microns-thick, can enable practical refrigeration also shows epitaxial materials engineering is a way to develop new and advanced thermoelectric materials. This is akin to the most advanced higher efficiency photovoltaic devices of today^{26,27} are based on epitaxial growth of multi-junction devices in contrast to bulk Si PV technology²⁸. The materials requirement for TFTEC and scalability of fabrication for a range of refrigeration needs are discussed in Supplementary Note 9. This is particularly important for reducing materials usage, summarized in Supplementary Table 1, along with

device technology being implemented with scalable microelectronic manufacturing²⁹ as shown in Supplementary Fig. 10. The scalability of solid-state refrigeration and cooling with TFTECs are expected to be analogous to the scalability of Li-ion battery storage technologies that power mobile phones to electric vehicles³⁰.

The MOCVD technique allows the fabrication of nanoengineered CHESS structures, as exemplified by the data shown in Fig. 1c-e in the manuscript. The use of an excellent ZT (Fig. 2) thin film thermoelectric device having a CHESS structure will enable the implementation of large-scale home appliances such as a refrigerator. The operational costs of the MOCVD technique are extremely advantageous for not only getting high-quality materials but epitaxial growth can be carried out at wafer scale up to 6" diameter in production reactors; hence MOCVD is the preferred deposition technique for worldwide production of white/ blue/green/red LEDs and solid-state laser devices. Most importantly, the quantity of materials needed with thin-film thermoelectric approach are very small, as noted in Supplementary Table 1, almost 1/1230th of bulk materials. MOCVD is one of the ways to realize the CHESS structure, however if any other deposition method can realize similar CHESS structures, a highefficiency refrigeration system can be realized as shown by the results of this study. Realization of high ZT and high-performance devices using sputtering and solution-based techniques to create nano-engineered thin-film thermoelectric materials are future possibilities for large volume refrigeration applications.

Recently, Samsung Electronics has unveiled a new hybrid cooling refrigerator by combining a conventional bulk thermoelectric module and a compressor. This hybrid system demonstrated better cooling efficiency, longer food preservation, and more internal space³¹. As the first case applied to the mainstream cooling system market, this approach highlights the need for the development of high-performance thermoelectric modules, to build refrigerators entirely with thermoelectric modules, thereby eliminating all mechanical components. It is anticipated that future higher-performance designs of hybrid cooling refrigerators as well as full-thermoelectric refrigeration systems could be enabled by the CHESS TFTEC technologies reported here.

The technology of thermoelectric cooling can be applied not just to refrigerators but also to a wide range of heat-regulating applications. TFTECs capacity for precise temperature regulation and maintenance makes it an adaptable solution for products requiring universal heat management. This allows for its integration into various cooling and heating systems, broadening its usage beyond conventional refrigeration³² to other temperature-sensitive needs. The ability to carry out open-air freezing/refrigeration (Supplementary Note 10) at the individual couple to the module level, due to the high heat pumping capacity of the TFTEC devices, are shown in Supplementary Fig. 11. The ability of refrigeration/open air freezing with TFTEC modules to run continuously, managing latent heat of freezing, are shown in Supplementary Fig. 11 and Supplementary Movie 1 (credit: JHUAPL). The small foot-print of TFTEC modules will allow us to meet the refrigeration needs of cauterization, localized cryo-surgery, and cryotherapy using the extreme cold conditions to freeze and remove abnormal tissues33. The TFTECs can also enable neuronal-blocking of pain³⁴ and thermal sensations in bionic limbs^{7,35,36} in medical applications. The demonstrated CoP advancements with CHESS TFTEC devices apply to efficient cooling of microelectronic thermal management at chip level^{6,37} to innovative cooling for energy-efficient data servers³⁸ and in portable HVAC applications. The compact high-performance CHESS refrigeration technology can also be applied to enhance the acoustic range in chip-scale thermoacoustics, enabling devices that can produce sound and more faithfully reproduce music and speech^{39,40}.

Methods

Thin-film CHESS Materials Growth by MOCVD and characterization

The thin-film controlled hierarchically engineered superlattice structures (CHESS) were deposited by metal-organic chemical vapor deposition (MOCVD) for the p-type Bi₂Te₃/Sb₂Te₃ materials system (Fig. 1b) and n-type Bi₂Te₃/Bi₂Te_{2.7}Se_{0.3} materials systems (Fig. 1a). Both n-type and p-type CHESS films are grown on semi-insulating (001) GaAs substrates. CHESS films are grown using hydrogen as a diluent and carrier gas with a chamber pressure of 350 Torr. The growth temperatures are 385 °C and 430 °C for p-type and n-type materials, respectively. After the growth is completed room temperature characterization such as XRD, Hall, and Seebeck measurements are performed to determine the structural, electrical, and thermoelectric 41-44 properties of the CHESS film. In Fig. 1e, we show the accomplishment of the intended CHESS structures by HAADF (High Angle Annular Dark Field) STEM measurements carried out on MOCVD-grown CHESS Bi₂Te₃/Sb₂Te₃. CHESS structures, with varying layer thicknesses at the nanoscale, are evident in spite of unavoidable sample damage that can occur during current TEM sample prep methodologies like Focused Ion Beam (FIB) preparation which can diminish or distort the material contrast between various layers. Hence, we have utilized cryogenic FIB to minimize the sample damage.

Thin-film thermoelectric cooling device fabrication

The fabrication of the TFTEC cooling module utilizing the higherperformance Controlled Hierarchically Engineered Superlattice Structures (CHESS) materials with DBC headers⁷. The TFTEC device was fabricated using MOCVD to grow 25 µm thick p-type (Bi₂Te₃/ Sb₂Te₃) and n-type (Bi₂Te₃/Bi₂Te_{2.7}Se_{0.3}) CHESS materials; then transferred to an aluminum nitride (AIN) substrate. Each thin-film die was 1.2 mm × 1.2 mm × 0.3 mm and consisted of two p-n couples with an AlN header connecting the p-n couples (Fig. 2a). Each of the p-n couples were thermally and electrically in parallel for built-in redundancy but each of these couples were in a series electrical circuit of anywhere between a 4×4 (or 16-couple), 6×9 or (or 54-couple), or 10×8 (or 80couple) module. The individual p-n couples in the array were connected electrically in series utilizing commercially available directbond copper (DBC) AIN substrate, consisting of gold coated copper traces. Each of the thin-film p-n couples were sandwiched between the DBC AIN headers and they are connected electrically in series using the respective contact metallization of the CHESS semiconductors (Fig. 2a). All the individual p-n thin-film couples in a TFTEC module operate thermally in parallel with the placement of a common header (Fig. 3) for realizing the HAF-LIOF concept.

Thermoelectric figure-of-merit (ZT) characterization

ZT characterizations of the thermoelectric devices were carried out at room temperature (\sim 25 °C) in atmosphere and in vacuum (35 mTorr), to minimize any unwanted thermal effects of room air drafts as well as from ambient humidity. The figure of merit (ZT) for each device was estimated using the Harman method by measuring the voltage across the module when the steady-state input current to the device was stopped^{1,7}. The device-level ZT for thermoelectric devices can be experimentally obtained using the ratio of the Peltier voltage (V₀) and the Ohmic voltage (Vr); the details are further described in Refs. 1,7.

Reporting summary

Further information on research design is available in the Nature Portfolio Reporting Summary linked to this article.

Data availability

All data generated or analyzed during this study are included in this published article (and its supplementary information files). Data and

any files used to analyze the results are available through Materials Transfer Agreement upon request to the corresponding author.

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Author contributions

R.V., J.M.P., and J.B. implemented and conducted the TFTEC solid state refrigeration experiments, with inputs from S.-J.J., J.S., M.K., and J.L. at Samsung, J.M.P. and R.V. discussed the epitaxial CHESS thin-film growth needed for the TFTEC devices and the MOCVD growth of films were carried out by J.M.P, J.B., and R.U. The TFTEC modules were designed by R.V., J.M.P. and the team at JHUAPL. The epi for the TFTEC modules were processed and tested for various parameters by M.H., V.R., R.U. and J.B., with oversight from R.V. The IR imaging on the TFTEC modules were obtained by J.M.P. and J.B. The TFTEC modules assembly into the refrigerators was led by J.B., with support from J.M.P. and oversight from R.V. and tests were carried out. The heat load calculations from the ambient into the refrigerator was modeled and necessary experiments were validated by the Samsung team in discussions with R.V. The refrigeration data modeling and the analytical expressions were derived by R.V. in discussions with J.M.P. and Samsung team. R.V. wrote the manuscript, with inputs from J.M.P., J.B., and the Samsung team. R.V. served as the Principal Investigator of the technology development and validation with J.M.P. as the project operations lead at APL and J.L. as Project administration lead at Samsung.

Competing interests

R.V. and J.M.P., are inventors on intellectual property pertaining to thinfilm thermoelectric devices and US Patents 11,227,988, 11,532,778, and application 18/071,789. R.V. and J.M.P. are inventors on US Patent 10,903,139. Johns Hopkins University is the applicant on these patents. R.V. and J.M.P. do not declare any other financial or non-financial competing interests. The remaining authors J.B., M.H., S-J.J., V.R., R.U., J.S., M.K., and J.L. declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Rama Venkatasubramanian.

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