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Electrically Tunable and Negative Schottky Barriers in Multi-layered Graphene/MoS_2 Heterostructured Transistors

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Dongri Qiu & Eun Kyu Kim

We fabricated multi-layered graphene/MoS_2 heterostructured devices by positioning mechanically exfoliated bulk graphite and single-crystalline 2H-MoS_2 onto Au metal pads on a SiO_2/Si substrate *via* a contamination-free dry transfer technique. We also studied the electrical transport properties of Au/MoS_2 junction devices for systematic comparison. A previous work has demonstrated the existence of a positive Schottky barrier height (SBH) in the metal/MoS_2 system. However, analysis of the SBH indicates that the contacts of the multi-layered graphene/MoS_2 have tunable negative barriers in the range of 300 to −46 meV as a function of gate voltage. It is hypothesized that this tunable SBH is responsible for the modulation of the work function of the thick graphene in these devices. Despite the large number of graphene layers, it is possible to form ohmic contacts, which will provide new opportunities for the engineering of highly efficient contacts in flexible electronics and photonics.

Introduction

Among layered 2-dimensional (2D) materials, molybdenum disulfide (MoS_2) is attracting attention as a semiconducting material in the transition metal dichalcogenide family[1,2]. Because of quantum mechanical confinement, MoS_2 possesses several remarkable properties, such as an absence of dangling bonds[3], a lack of inversion symmetry[4], valley degrees of freedom[5], and other fascinating physical properties; as a result, it shows promise as a novel candidate material for high-performance and low-power electronics applications[6]. Moreover, the individual layers, which interact through the van der Waals force, can be readily exfoliated into atomically thin layers[7], and when this method is applied to combine MoS_2 with other 2D materials, novel heterostructured devices can be constructed[8]. Examples of these types of structures that have been reported in the literature include vertical tunneling transistors[9,10], hybrid graphene/MoS_2 photoresponsive devices[11], and memory devices that incorporate hexagonal boron nitride[12]. Although multifunctional device architectures offer various promising functionalities, various aspects of the performance-degradation effect have not been fully explored. In particular, previous studies have shown that the metal/MoS_2 and gate dielectric/MoS_2 interfaces significantly affect device performance[13–15]. In the case of the metal/MoS_2 interface, there is a scalable Schottky barrier height (SBH) that restricts carrier injection when a very low-work-function metal, such as scandium, is used[13]. Several previous works on contact optimization using single-layer graphene have been affected by the same difficulties[16–17]. However, very recently, Yu, L. *et al.*[18] and Liu, Y. *et al.*[19] have observed a barrier-free contact by using single-layer graphene as the back interconnection. Nevertheless, ohmic contact has been rarely achieved with relatively thick graphene (or graphite), and few detailed studies on the back-gate tunability of negative barrier heights have been conducted.

In this study, we present heterostructured MoS_2 field-effect transistors (FETs) that contain approximately 20 layers of graphene (denoted below as MGr) to form bottom-up interconnections for source

Quantum-Function Research Laboratory and Department of Physics, Hanyang University, Seoul 133-791, South Korea. Correspondence and requests for materials should be addressed to E.K.K. (email: ek-kim@hanyang.ac.kr)

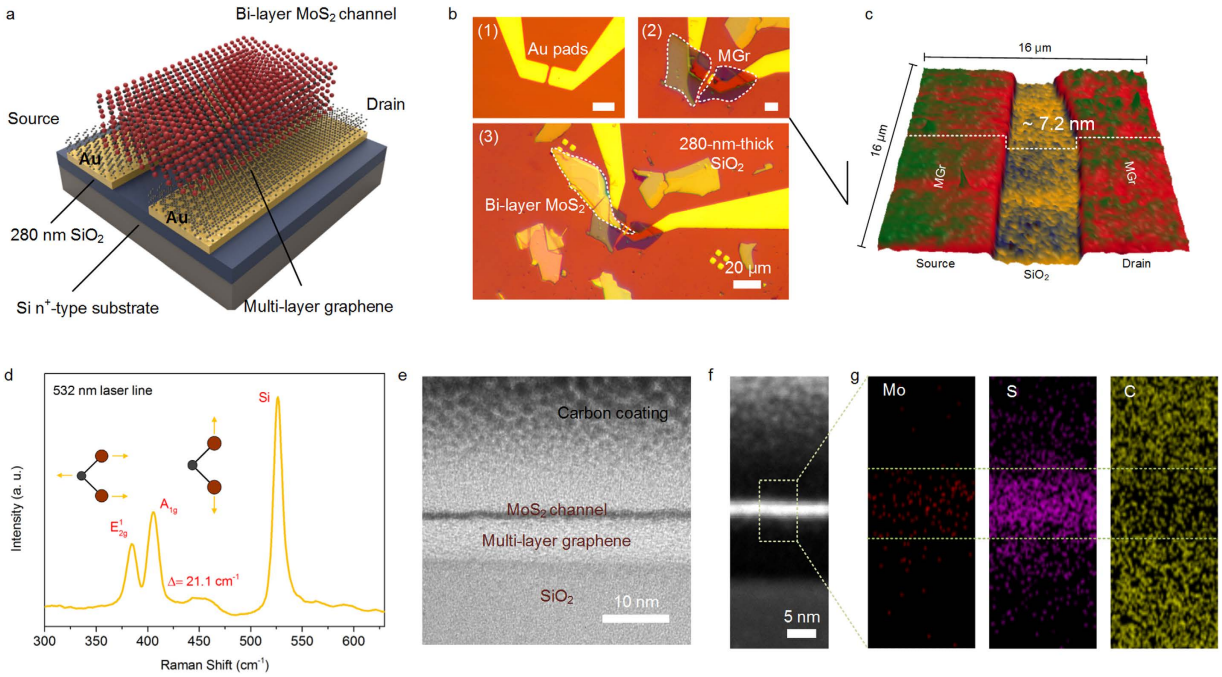

Figure 1. Fabrication process and schematic illustration of an MGr/MoS_2 device. (**a**) A 3D schematic image of our back-gated MoS_2 FET. (**b**) An optical image of pre-patterned Au pads (1), MGr flakes deposited on top of the Au electrodes (2), and the separation distance between them, which is defined as the channel length (L ~ 3.5 μm), as well as an optical image of the transfer of MoS_2 flakes onto the top surface of the MGr/Au stack to form a semiconducting channel with a width of W ~5.2 μm (3). (**c**) 3D AFM topographic image of MGr source/drain electrodes deposited on a 280-nm-thick SiO_2/Si substrate. (**d**) The Raman signal collected from the deposited MoS_2 channel in the MGr/MoS_2 FET and compared with that of MoS_2 flakes, as shown in Figure S2. (**e**) Cross-sectional HRTEM image of the heterostructured FET. (**f**) STEM image showing the interface between the MGr and the few-layered MoS_2 as well as the top of the carbon-Pt coating. (**g**) EDX mapping of the selected area for the Mo, S, and C elements.

and drain electrodes. Here, an alternative approach was engineered by inserting a thick graphene layer instead of single-layer graphene. To compare the characteristics of the devices, reference samples without MGr contacts were also fabricated. The heterostructured FETs exhibited a dramatic reduction in SBH based on the framework of the thermionic emission theory. It appeared that the observed negative SBH gave rise to true ohmic contact.

Results

Fabrication of the devices. A 3-dimensional (3D) schematic representation of our heterostructured device architecture is depicted in Fig. 1a. To investigate the electronic properties of the back-gated MGr/MoS_2 heterostructured devices, we deposited mechanically exfoliated graphite and single-crystalline 2H-MoS_2 onto a SiO_2/Si substrate on which Au metal pads (110 nm thick) had been pre-patterned, as described in the Methods section. The dry transfer technique used for both 2D materials began with the introduction of an intermediate polydimethylsiloxane (PDMS) layer, which acted as a contamination-free viscoelastic material to avoid wet chemistry (more information can be found in the Supplementary Information, Figure S1). Two multi-layered graphene samples were transferred from the PDMS layer to serve as the source and drain, as shown in Fig. 1b. Subsequently, a MoS_2 flake was directly transferred on top of the graphene flakes, overlapping both graphene contacts, to form a semiconducting channel using the same method (see (3) in Fig. 1b). For comparison, we also fabricated un-encapsulated bi- to quad-layer MoS_2 FETs (denoted below as Au/MoS_2) without inserting an MGr layer; for these devices, the transfer procedure was reduced to only one step. The MoS_2 channel was verified using Raman spectroscopy and atomic force microscopy (AFM) to confirm the thickness of the MoS_2 flakes (see Fig. 1d and the Supplementary Information, Figures S2 and S3). The frequency difference of 21.1 cm^{-1} between the in-plane mode (E^1_{2g}) and the out-of-plane mode (A_{1g}) corresponds to the signal of bi-layer MoS_2, which is consistent with our MoS_2 reference sample (Figure S2) and other reports[20]. Optical microscopy and AFM were used to determine the MGr thicknesses, which were 7.1 and 7.3 nm for the source and drain, respectively, as shown in Fig. 1c. The average height of the graphene flakes was further characterized using statistical studies and was found to be ~7 nm (Figure S4). Cross-sectional high-resolution

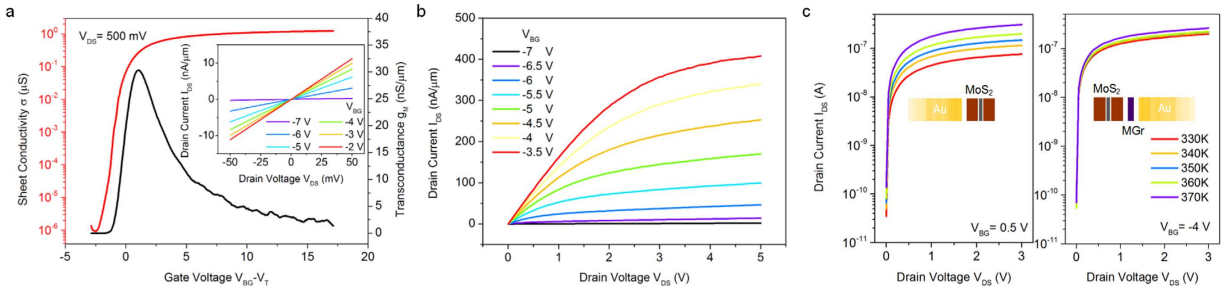

Figure 2. Electrical performance of the transistors. (**a**) Normalized I-V transfer characteristics of a typical back-gated MGr/MoS_2 device at a fixed drain voltage. Inset: I_{DS}-V_{DS} curve at a low drain bias ($V = \pm 50$ mV). The linearity was maintained under various gate voltages. (**b**) Output characteristics at various gate voltages. (**c**) Left: Temperature-dependent (from 330 to 370 K in 10-K increments) I_{DS}-V_{DS} characteristics for an Au/MoS_2 FET (left) and an MGr/MoS_2 FET (right). The inset shows the corresponding device configurations.

transmission electron microscope (HRTEM) analysis was used to study the overlapped MGr/MoS_2 stack. An HRTEM image of a clear and compact interface, without other impurities or significant gaps between the MoS_2 and MGr, is shown in Fig. 1e. Figure 1f displays a scanning TEM (STEM) image of the MGr/MoS_2 heterostructure, and the corresponding energy-dispersive X-ray spectroscopy (EDX) mapping is shown in Fig. 1g and S5.

Characterization of the devices. To investigate the presence of the intermediate MGr layer in our MGr/MoS_2 devices and its influence on the Schottky barrier, the devices were electrically characterized at room temperature. Figure 2a shows the typical I_{DS}-V_{BG} transfer characteristics of the back-gated heterostructured FETs, which are presented as a normalized sheet conductivity (defined as $\sigma = I_{DS}/V_{DS}(L/W)$) as a function of V_{BG}-V_T, where V_{BG} is the gate voltage and V_T is the threshold voltage. The devices displayed obvious n-type behavior and produced a high on/off ratio (~10^6) with a maximum normalized transconductance g_M/W of approximately 30.4 nS/μm at $V_{DS} = 500$ mV. I-V hysteresis behavior is also shown in Figure S6. After *in situ* thermal heating, the devices exhibited nearly "hysteresis-free" behavior, indicating that the amount of adsorbates was negligible[21]. By contrast, the devices without an MGr layer demonstrated a transconductance of 0.35 nS/μm at $V_{DS} = 500$ mV, which is 2 orders of magnitude lower than that of the MGr/MoS_2 FETs, as shown in Figure S7. The field-effect mobility, μ_{FE}, was estimated from the maximum value of the transconductance using the expression $\mu_{FE} = g_M L/WC_{OX}V_{DS}$. Here, $C_{OX} = \varepsilon_r\varepsilon_0/d_{OX} \sim 1.23 \times 10^{-8}$ F/cm^2 ($\varepsilon_0 = 8.854 \times 10^{14}$ F/m, $d_{OX} = 280$ nm), which is the back-gate capacitance per unit area, and $g_M = dI_{DS}/dV_{BG}$ is the transconductance. Thus, the field-effect mobility for our bi-layer MGr/MoS_2 device appeared to be approximately 17.9 cm^2/Vs in the bi-layer MoS_2 channel, as presented in Figure S8. This measured mobility is comparable to those of mono- or bi-layer MoS_2 in high-κ gate dielectric capping devices[22,23]. The reference sample (thick bi-layer MoS_2) with an Au metal contact had a mobility of 0.2 cm^2/Vs, which is consistent with other reports[3,24,25]. Such a low mobility may be originated from the presence of a sizable Schottky barrier at the Au-MoS_2 interface that hinders efficient carrier injection. To extract an accurate gate capacitance for the mobility calculation, a 100-kHz capacitance-voltage (C-V) profile was obtained by measuring between the source and back-gate electrodes (see Figure S9). The floor value of the capacitance (the minimum capacitance in the inversion regime) represented the actual electrode capacitance[26], and the measured gate capacitance (~1.24×10^{-8} F/cm^2) was very close to the value of 1.23×10^{-8} F/cm^2 obtained in the above calculation for a 4.52-mm^2 contact area.

Extraction of the Schottky barrier height. Figure 2b displays the I_{DS}-V_{DS} output characteristics of the MGr/MoS_2 devices at various gate voltages. The saturation current could be reached at high drain voltages under certain gate biases, opening a wide drain voltage window. Moreover, the drain current, I_{DS}, exhibited symmetrical and linear behavior (inset of Fig. 2a) under a small source-drain bias sweep (± 50 mV). Previous studies have claimed that the linear relationship in the range of low V_{DS} bias suggests ohmic contact at the metal-to-semiconductor junction[27]. However, the present experimental findings imply the existence of a sizable energy barrier at the two back Schottky diodes based on detailed variable-temperature measurements. Remarkably, the I_{DS}-V_{DS} characteristics at a fixed gate bias, on the right-hand side of Fig. 2c, manifested an extremely weak temperature dependence in the temperature range from 330 to 370 K compared with the Au/MoS_2 sample (left-hand side of Fig. 2c). This weak temperature dependence implies a reduction in the barrier height for thermal emission due to the modification of the barrier at the MGr/MoS_2 interface.

To better understand how the carriers travel in the presence of a Schottky barrier, we employed a well-known model, *i.e.,* the 3D thermionic-emission theory, to describe our observations. Generally, the two carrier transport mechanisms are thermionic emission and quantum-mechanical tunneling under

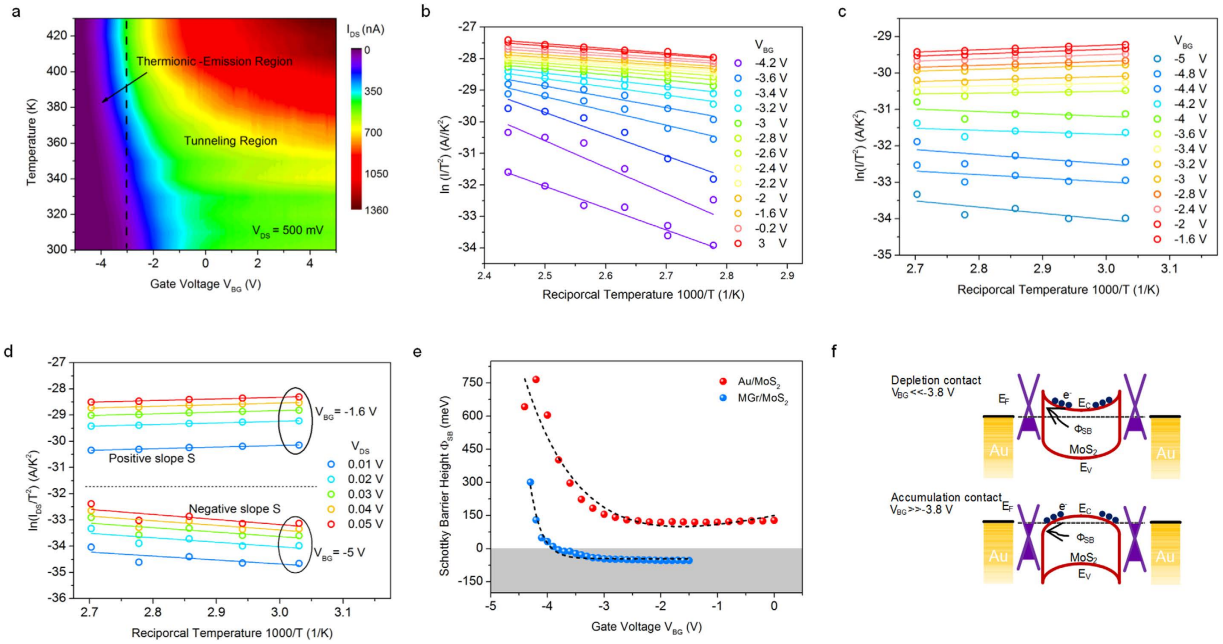

Figure 3. Temperature dependence of electrical transport and the extraction of the Schottky barrier height. (**a**) Color map of the temperature-dependent transfer characteristics at $V_{DS} = 500$ mV. (**b,c**) Arrhenius plots of $\ln(I_{DS}/T^2)$ *vs.* 1000/T at various gate voltages for an Au/MoS_2 FET (**b**) and an MGr/MoS_2 FET (**c**,**d**) Arrhenius plot for $V_{BG} = -1.6$ V and -5 V at various drain voltages from 10 to 50 mV. (**d**) Gate bias dependence of the variations in the Schottky barrier height. (**e**) Top: Schematic band diagram for a depletion-type contact. Bottom: Illustration of an accumulation contact.

gate bias modulations, as shown in Fig. 3a. The former current mechanism is associated with the emission of majority carriers over the interfacial barrier, and the tunneling mechanism involves carriers crossing the barrier in a highly accumulated MoS_2 channel. Under the assumption that the current is predominantly governed by the thermionic emission theory, the current I_{DS} is given by the expression[28] $I_{DS} = AA^*T^2\exp(-e\Phi_{SB}/k_BT)[\exp(eV_{DS}/k_BT) - 1]$, where A^*, A, e, V_{DS}, and k_B are the Richardson constant, the area of the contact, the elemental charge, the drain voltage, and the Boltzmann constant, respectively. Temperature-dependent I-V data were collected in the high-temperature regime (above room temperature) to avoid weak conductivity variations (see the Supporting Information, Figure S10). Such variations occur because at low temperature in the off state, the carriers do not have sufficient energy to pass through the barrier, and thermionic emission theory fails to explain this behavior (a detailed discussion can be found in ref. 29). To determine the SBH, the reciprocal temperature dependence of the $\ln(I_{DS}/T^2)$ fit curve was plotted for various gate voltages at the Au/MoS_2 (Fig. 3b) and MGr/MoS_2 (Fig. 3c) interfaces. The slope, S, was extracted from the different V_{BG} values of the Arrhenius plot, and the intercept, S_{INT}, yielded the Schottky barrier height, Φ_{SB}, as a function of the gate voltage, V_{BG}, using the expression $S_{INT} = -e\Phi_{SB}/1000\,k_B$ (see the Supporting Information, Figure S11). For the MGr/MoS_2 devices, the slope of the linear fit curve in the Arrhenius plot is negative near the off state (low V_{BG}; -5 V) and becomes more positive with the formation of a highly conductive MoS_2 channel at $V_{BG} = -1.6$ V, as depicted in Fig. 3d. The resulting features imply that the SBH dramatically decreases from 300 to 0 meV, becomes negative, and finally saturates near -45.5 meV, as shown in Fig. 3e. This finding represents the first observation of negative SBH behavior at an MGr/MoS_2 contact and is contrary to the results of several studies that have investigated this phenomenon in the 0–300 meV range[16–19]. Similar findings have been reported in conventional semiconductors and novel 2D materials, *e.g.*, MoS_2 with ferromagnetic permalloy contacts[29], p-type MoS_2 with MoO_X[30], and silicon (001) with metal Ti[31]. By contrast, for the Au/MoS_2 contact considered in this study, under a negative gate bias, the current through the Schottky barrier *via* thermionic emission resulted in a linearly decreasing trend (from 765.9 to 118.8 meV) as the gate bias became forward directed.

Negative Schottky barrier behavior. Generally, the semiconductor surface states and the work functions of the metal play a decisive role in the determination of the SBH, but the details of Schottky barrier formation in metal/semiconductor systems are not well understood. Various previous studies on metal/MoS_2 contacts have demonstrated an independence of the metal work functions due to the presence of interfacial states, D_{IT}, that cause Fermi-level pinning[13,14,32,33]. By combining the experimental

data presented in Figure S12 of the Supporting Information, we estimated D_{IT} using the expression[28] $D_{IT} \approx 1.1 \times 10^{13}(1 - S_0)/S_0 \approx 7.9 \times 10^{13}$ states/eV cm^2, where the slope is $S_0 = d\Phi_{SB}/d\Phi_M \approx 0.12$ and Φ_M is the metal work function. However, when MGr and MoS_2 are brought into contact, the Schottky-Mott model does not hold, because $D_{IT} \neq 0$. A modified model can be written as follows[34]:

$$\Phi_{SB} = S_0(\Phi_{MGr} - e\chi) + (1 - S_0)(E_G - \Phi_N) \quad (1)$$

where $\Phi_{MGr} = 4.5$ eV and $\chi = 4.0$ eV are the work function of the graphene and the electron affinity of the MoS_2[35,36], respectively; $E_G = 1.6$ eV is the band gap of the bi-layer MoS_2; and $\Phi_N = 1.53$ eV is the neutral level of the interface states. In practice, the Fermi level is pinned at a certain energy, and then, a depletion contact with a positive Schottky barrier is created at the MGr/MoS_2 interface. Considering this behavior, the first term of equation (1) will change to a negative value under the influence of the gate voltage, forming an accumulation contact (with a negative barrier height), at which the preferred ohmic contact can be formed (as shown in Fig. 3f). Because Φ_{MGR} depends on the back-gate electric field, the carrier density in the MGr shifts the Fermi level by $\Delta E_{F,MGr} = \hbar\nu_F\sqrt{\nu r|C_{OX}/e(V_{BG} - V_T)|}$), where ν_F is the Fermi velocity. The tunability of the work function of graphene has been demonstrated by Yu, Y.-J. *et al.*[37] only for the single- and bi-layer cases, not for thick layers such as those used in our experiments. Furthermore, if the work function of the multi-layered graphene, Φ_{MGr}, is less than that of the MoS_2, *i.e.,* $\Phi_B(V_{BG}) = \Phi_{MGr} - \Phi_{MoS2}(V_{BG})$, then it is possible for a negative contact potential, $\Phi_B(V_{BG})$, to arise as shown in Fig. 3f. As demonstrated by Li, Y. *et al.*[38], the electric-field-driven modulation of the work function of MoS_2 is estimated to be $\Phi_{MoS2}(V_{BG}) = e(\chi + \phi_S) - \hbar\pi(C_{OX}/e)(V_{BG} - V_T)/2m^*$, where ϕ_S, $\hbar$, and m^* are the surface potential, Planck's constant, and the effective mass of bi-layer MoS_2, respectively. For the values given in ref. 38, the Fermi-level variation, $\Delta E_{F,MoS2}$, of the bi-layer at the turning point voltage ($V_{BG} = -3.8$ V) is only approximately 31 meV, which is quite small. Therefore, we suggest that the tunable Schottky barrier is primarily responsible for the modulation of the work function of the thick graphene. Despite the large number of graphene layers, ohmic contacts can be formed, which will provide new opportunities for the engineering of highly efficient contacts in flexible electronics and photonics applications.

Discussion

In summary, we fabricated heterostructured MoS_2 FETs with multi-layered graphene contacts and systematically investigated their electronic properties at the MGr/MoS_2 interface. Negligible hysteresis was observed because of the optimized fabrication procedure. Upon the insertion of an intermediate tunnel layer, the devices displayed highly improved performance in terms of carrier mobility. An interesting negative Schottky barrier behavior was observed between the MoS_2 and the multi-layered graphene. We also qualitatively discussed the formation of ohmic contacts, which likely contributed to the controllability of the graphene work function by gate bias modulation. Thus, we were able to improve the carrier injection behavior and reduce the contact resistance, thereby developing a new possible approach for future electronics applications.

Methods

Multi-layered graphene was mechanically exfoliated from single-crystalline graphite (from Graphene Supermarket) using the standard Scotch-tape-based cleavage method. The thick graphene flakes were transferred onto bottom gold electrodes, which served as the source and drain, using techniques described previously[39]. In brief, this technique was based on the use of a viscoelastic PDMS layer that served as an acceptor surface in place of a silicon substrate. The 2D flakes were deposited on the PDMS layer and then aligned on top of the Au pads using optical microscopy. We then brought the 2D/PDMS stack into contact with the target substrate and slowly peeled it away from the PDMS.

Before the dry transfer was performed, the gold electrodes were pre-patterned on a degenerately doped Si substrate covered with a 280-nm layer of SiO_2. We intentionally chose two similar thicknesses of graphene flakes to perform the above techniques twice. Subsequently, MoS_2 (2D semiconductor) flakes were precisely deposited on top of the graphene contacts to serve as a channel material. The fabrication process described above avoids the use of any chemical solutions to minimize contamination. The devices were subsequently annealed at 399 K for 12 hours in a cryostat (ASK, 700 K) at a base pressure of ~2×10^{-2} Torr for the removal of adsorbates. Electrical measurements were performed using a semiconductor parameter analyzer (HP, 4156A) after *in situ* vacuum annealing. C-V measurements were performed using a Precision LCR meter (Agilent, E4980A) with the samples in the same chamber.

A focused ion beam (FEI, Quanta 3D FEG) was employed to prepare cross-sectional TEM samples after the deposition of a carbon/Pt coating. HRTEM imaging was performed using a spherical-aberration-corrected TEM (JEOL, JEM-2100F) operating at 200 kV. Chemical composition mapping was performed with an EDX apparatus attached to the TEM instrument.

The numbers of layers of graphene and MoS_2 were determined based on the color contrast in the optical microscope images and were further confirmed by AFM (Park Systems, XE-100). Raman spectroscopy (Jaco, NRS-3100) with laser excitation at $\lambda = 532$ nm was employed to analyze the spectra of the MoS_2 reference flakes and the FET channels.

References

1. Ganatra, R. & Zhang, Q. Few-Layer MoS_2: A Promising Layered Semiconductor. *ACS Nano* **8,** 4074–4099 (2014).
2. Hsu, A. *et al.* Large-Area 2-D Electronics: Materials, Technology, and Devices. *Proc. IEEE*, **101,** 1638–1652 (2013).
3. Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N. & Strano, M. S. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nat. Nanotechnol.* **7,** 699–712 (2012).
4. Wu, S. F. *et al.* Electrical tuning of valley magnetic moment through symmetry control in bilayer MoS_2. *Nat. Phys.* **9,** 149–153 (2013).
5. Mak, K. F., He, K., Shan, J. & Heinz, T. F. Control of valley polarization in monolayer MoS_2 by optical helicity. *Nat. Nanotechnol.* **7,** 494–498 (2012).
6. Radisavljevic, B. & Kis, A. Mobility engineering and a metal-insulator transition in monolayer MoS_2. *Nat. Mater.* **12,** 815–820 (2013).
7. Novoselov, K. S. *et al.* Two-dimensional atomic crystals. *Proc. Natl. Acad. Sci. USA.* **102,** 10451–10453 (2005).
8. Geim, A. K. & Grigorieva, I. V. Van der Waals heterostructures. *Nature* **499,** 419–425 (2013).
9. Georgiou, T. *et al.* Vertical field-effect transistor based on graphene-WS_2 heterostructures for flexible and transparent electronics. *Nat. Nanotechnol.* **8,** 100–103 (2013).
10. Yu, W. J. *et al.* Vertically stacked multi-heterostructures of layered materials for logic transistors and complementary inverters. *Nat. Mater.* **12,** 246–252 (2013).
11. Roy, K. *et al.* Graphene-MoS_2 hybrid structures for multifunctional photoresponsive memory devices. *Nat. Nanotechnol.* **8,** 826–830 (2013).
12. Choi, M. S. *et al.* Controlled charge trapping by molybdenum disulphide and graphene in ultrathin heterostructured memory devices. *Nat. Commun.* **4,** 1624 (2013).
13. Das, S., Chen, H. Y., Penumatcha, A. V. & Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **13,** 100–105 (2013).
14. Dankert, A., Langouche, L., Kamalakar, M. V. & Dash, S. P. High-Performance Molybdenum Disulfide Field-Effect Transistors with Spin Tunnel Contacts. *ACS Nano* **8,** 476–482 (2014).
15. Afanasev, V. V., Bassler, M., Pensl, G. & Schulz, M. Intrinsic SiC/SiO_2 Interface States. *physica status solidi (a)* **162,** 321–337, (1997).
16. Yoon, J. *et al.* Highly flexible and transparent multilayer MoS_2 transistors with graphene electrodes. *Small* **9,** 3295–3300 (2013).
17. Yuchen, D. *et al.* MoS_2 Field-effect Transistors with Graphene/Metal Heterocontacts. *Electron Device Letters, IEEE* **35,** 599–601 (2014).
18. Yu, L. *et al.* Graphene-MoS_2 Hybrid Technology for Large-Scale Two-Dimensional Electronics. *Nano Lett.* **14,** 3055–3063 (2014).
19. Liu, Y. *et al.* Toward Barrier Free Contact to Molybdenum Disulfide Using Graphene Electrodes. *Nano Lett.* **15,** 3030–3034 (2015).
20. Li, H. *et al.* From Bulk to Monolayer MoS_2: Evolution of Raman Scattering. *Adv. Funct. Mater.* **22,** 1385–1390 (2012).
21. Late, D. J., Liu, B., Matte, H., Dravid, V. P. & Rao, C. N. R. Hysteresis in Single-Layer MoS_2 Field Effect Transistors. *ACS Nano* **6,** 5635–5641 (2012).
22. Lee, G.-H. *et al.* Flexible and transparent MoS_2 field-effect transistors on hexagonal boron nitride-graphene heterostructures. *ACS Nano* **7,** 7931–7936 (2013).
23. Chan, M. Y. *et al.* Suppression of thermally activated carrier transport in atomically thin MoS_2 on crystalline hexagonal boron nitride substrates. *Nanoscale* **5,** 9572–9576 (2013).
24. Jin, T., Kang, J., Su Kim, E., Lee, S. & Lee, C. Suspended single-layer MoS_2 devices. *J. Appl. Phys.* **114,** 164509, (2013).
25. Fuhrer, M. S. & Hone, J. Measurement of mobility in dual-gated MoS_2 transistors. *Nat. Nanotechnol.* **8,** 146–147 (2013).
26. Kim, S. *et al.* High-mobility and low-power thin-film transistors based on multilayer MoS_2 crystals. *Nat. Commun.* **3,** 1011 (2012).
27. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **6,** 147–150 (2011).
28. Sze, S. M. & Ng, K. K. *Physics of semiconductor devices*. 3rd edn, (John Wiley & Sons 2006).
29. Wang, W. *et al.* Controllable Schottky Barriers between MoS_2 and Permalloy. *Sci Rep* **4,** 6928 (2014).
30. Chuang, S. *et al.* MoS_2 P-type Transistors and Diodes Enabled by High Work Function MoO_x Contacts. *Nano Lett.* **14,** 1337–1342 (2014).
31. Tao, M., Udeshi, D., Agarwal, S., Maldonado, E. & Kirk, W. P. Negative Schottky barrier between titanium and n-type Si(001) for low-resistance ohmic contacts. *Solid-State Electron.* **48,** 335–338 (2004).
32. Chen, J. R. *et al.* Control of Schottky Barriers in Single Layer MoS_2 Transistors with Ferromagnetic Contacts. *Nano Lett.* **13,** 3106–3110 (2013).
33. Kaushik, N. *et al.* Schottky barrier heights for Au and Pd contacts to MoS_2. *Appl. Phys. Lett.* **105,** 113505 (2014).
34. Tung, R. T. Chemical Bonding and Fermi Level Pinning at Metal-Semiconductor Interfaces. *Phys. Rev. Lett.* **84,** 6078–6081 (2000).
35. Walia, S. *et al.* Characterization of metal contacts for two-dimensional MoS_2 nanoflakes. *Appl. Phys. Lett.* **103,** 232105 (2013).
36. Ochedowski, O. *et al.* Effect of contaminations and surface preparation on the work function of single layer MoS_2. *Beilstein J. nanotechnol.* **5,** 291–297 (2014).
37. Yu, Y.-J. *et al.* Tuning the Graphene Work Function by Electric Field Effect. *Nano Lett.* **9,** 3430–3434 (2009).
38. Li, Y., Xu, C. Y., Zhang, B. Y. & Zhen, L. Work function modulation of bilayer MoS_2 nanoflake by backgate electric field effect. *Appl. Phys. Lett.* **103,** 033122 (2013).
39. Choi, J.-Y. Graphene transfer: A stamp for all substrates. *Nat. Nanotechnol.* **8,** 311–312 (2013).

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Author Contributions

E.K.K. proposed the research and supervised the overall study. D.Q. designed the experiment and performed the device fabrication, characterization, and data analysis. D.Q. and E.K.K. analyzed the results and wrote the manuscript.

Additional Information

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