micromachines

Article

Compensating Circuit to Reduce the Impact of Wire Resistance in a Memristor Crossbar-Based Perceptron Neural Network

Son Ngoc Truong

Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City 70000, Vietnam; sontn@hcmute.edu.vn; Tel.: +84-931-085-929

Received: 8 September 2019; Accepted: 1 October 2019; Published: 2 October 2019

Abstract: Wire resistance in metal wire is one of the factors that degrade the performance of memristor crossbar circuits. In this paper, an analysis of the impact of wire resistance in a memristor crossbar is performed and a compensating circuit is proposed to reduce the impact of wire resistance in a memristor crossbar-based perceptron neural network. The goal of the analysis is to figure out how wire resistance influences the output voltage of a memristor crossbar. It emerges that the wire resistance on horizontal lines causes the neuron's output voltage to vary more than the wire resistance on vertical lines. More interesting, the voltage variation caused by wire resistance on horizontal lines increases proportionally to the length of metal wire. The first column has small voltage variation whereas the last column has large voltage variation. In addition, two adjacent columns have almost the same amount of voltage variation. Under these observations, a memristor crossbar-based perceptron neural network with compensating circuit is proposed. The neuron's outputs of two columns are put into a subtractor circuit to eliminate the voltage variation caused by the wire resistance. The proposed memristor crossbar-based perceptron neural network is trained to recognize the 26 characters. The proposed memristor crossbar shows better recognition rate compared to the previous work when wire resistance is taken into account. The proposed memristor crossbar circuit can maintain the recognition rate as high as 100% when wire resistance is as high as 2.5 Ω. By contrast, the recognition rate of the memristor crossbar without the compensating circuit decreases by 1%, 5%, and 19% when wire resistance is set to be 1.5, 2.0, and 2.5 Ω, respectively.

Keywords: memristor; crossbar array; wire resistance; synaptic weight; character recognition

1. Introduction

Neuromorphic computing, inspired from biological perception, was introduced by C. Mead in the late 1980s [1]. It has been expected to become an alternative architecture to overcome the bottleneck of von Neumann computer architectures [1,2]. Neuromorphic computing refers to a hardware implementation of a brain-inspired system, which has the capabilities of parallel processing like a human brain. For realizing neuromorphic computing systems, various research activities, based on CPUs (Central Processing Units), GPUs (Graphics Processing Units), FPGAs (Field-Programmable Gate Arrays), analog circuits, memory circuits, etc., have been proposed in the past two decades [3–8]. These architectures are based on CMOS (Complementary-Metal-Oxide-Semiconductor) technology, which is approaching the end of their capabilities because scaling CMOS down faces several fundamental limiting factors stemming from electron thermal energy and quantum-mechanical tunneling [9,10]. The memristor crossbar array has been one of the promising candidates for realizing neuromorphic computing systems because crossbar architecture can be made with high density and low cost [11]. Memristor was postulated by Leon O. Chua in 1971 as the fourth basic circuit element and experimentally demonstrated by HP Lab in 2008 [12,13]. A memristor is a resistor with modifiable resistance, which makes it ideal for mimicking the synaptic plasticity of biological neurons [14]. The early memristor-based synaptic circuits are composed of memristors and CMOS transistors [15–17]. However, pure memristor crossbar arrays without CMOS devices seem to be more efficient in terms of their integration and power consumption [18–23]. Miao Hu et al. proposed a crossbar synaptic array that is composed of a plus and minus crossbar array representing plus- and minus-polarity connection matrices for analog neuromorphic computing [20]. Such a pure memristor crossbar array is very effective in realizing the bio-inspired systems in term of power consumption and area occupation. To reduce area and power consumption, S. N. Truong proposed a new memristor crossbar array architecture which is composed of a single memristor array and a constant-term circuit [21].

In a memristor array, some amount of voltage drop can be caused by interconnect resistance, also known as wire resistance along the row and the column lines [19,24–27]. Wire resistance degrades the performance of the circuit more seriously when the array size increases [25]. To mitigate the impact of wire resistance, several interesting schemes were proposed [24–27]. These schemes are effective when they are applied to a memristor crossbar array, in which memristors are used as binary switches between two distinct high and low resistance states (HRS and LRS, respectively). However, the impact of wire resistance in an analog memristor crossbar array for realizing the synaptic weight matrix was not fully considered. In this work, we propose a memristor crossbar array with a compensating circuit for implementing the analog synaptic array of a perceptron neural network. The impact of wire resistance is mitigated by compensating the voltage variation of two adjacent columns.

In this work, the output voltages of columns are figured out with taking the existing of wire resistance into account. The mathematical analysis and the simulation result show that the output voltage of columns increase, which is caused by the amount of voltage lost from wire resistance. The column close to the first one has a small variation of voltage, compared to the one far from the first column. From these observations, we propose a compensating circuit to mitigate the voltage variation caused by the wire resistance in a memristor crossbar array.

2. Materials and Methods

Figure 1 shows an interesting memristor array circuit for implementing the synaptic weight matrix of a perceptron neural network [21]. A single memristor array and a constant-term circuit are used for realizing the negative and positive synaptic weights, instead of using two complementary crossbar arrays [20,21].

In Figure 1, $g_{j,k}$ is the memristor's conductance at the crossing point between the *j*th row and the kth column. $V_{IN,j}$ is the input voltage applied to the *j*th row. $V_{C,k}$ is the column-line voltage on the *k*th column. The column line, $V_{C,F}$, is added in Figure 1 instead of using another memristor array [21]. The column line, $V_{C,F}$, is connected to the inputs, from $V_{IN,1}$ to $V_{IN,m}$. In Figure 1, $V_{C,F}$ enters G_F that constitutes an inverting OP amp with the negative feedback resistor, R_{F1}. The output voltage of G_F is V_F that is connected to all the column lines from $V_{C,1}$ to $V_{C,n}$ via R_{F2}, as shown in Figure 1. By applying Kirchhoff current law to the column line, $V_{C,F}$, we can calculate V_F and $V_{O,k}$ with Equations (1) and (2).

$$V_F = -\sum_{j=1}^{m} \frac{R_{F1}}{R_B} V_{IN,j}. \tag{1}$$

$$V_{O,k} = -\left[\sum_{j=1}^{m}\left(R_0 \cdot g_{j,k} \cdot V_{IN,j}\right) + \frac{R_0}{R_{F2}} V_F\right]. \tag{2}$$

If we choose $R_{F1} = R_{F2}$ and combining Equation (1) with Equation (2), the following Equation (3) can be obtained [21].

$$\mathrm{V}_{\mathrm{O},k} = -\left[\sum_{j=1}^{\mathrm{m}}\left(\mathrm{R}_0 \cdot \mathrm{g}_{j,k} - \frac{\mathrm{R}_0}{\mathrm{R}_\mathrm{B}}\right)\mathrm{V}_{\mathrm{IN},j}\right]. \tag{3}$$

If $-\left(\mathrm{R}_0 \cdot \mathrm{g}_{j,k} - \frac{\mathrm{R}_0}{\mathrm{R}_\mathrm{B}}\right)$ is defined as a synaptic weight of the *j*th row and *k*th column, $\mathrm{w}_{j,k}$, we can rewrite Equation (3) with Equation (4).

$$\mathrm{V}_{\mathrm{O},k} = \sum_{j=1}^{\mathrm{m}} \mathrm{w}_{j,k}\mathrm{V}_{\mathrm{IN},j}, \tag{4}$$

where $\mathrm{w}_{j,k} = \mathrm{R}_0\left(\frac{1}{\mathrm{R}_\mathrm{B}} - \mathrm{g}_{j,k}\right) = \mathrm{R}_0\left(\frac{1}{\mathrm{R}_\mathrm{B}} - \frac{1}{\mathrm{M}_{j,k}}\right)$.

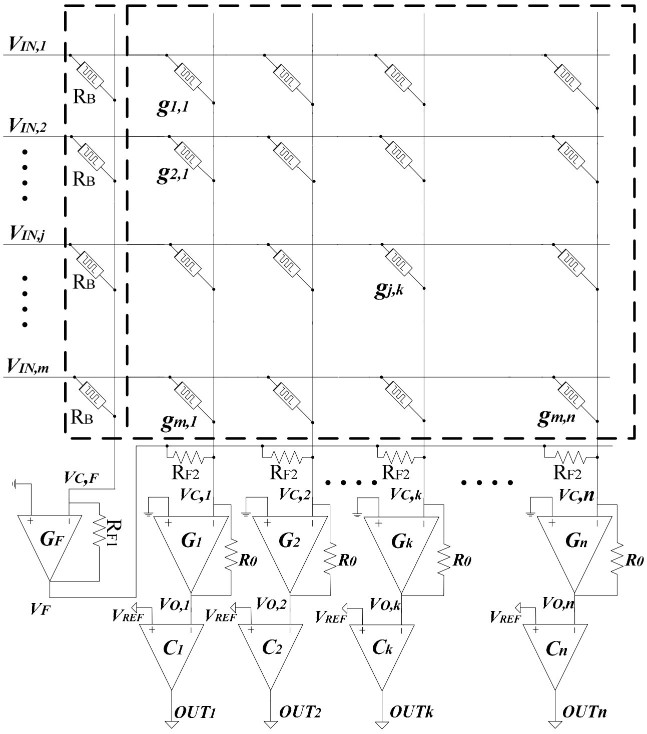


Figure 1. The memristor-based crossbar architecture with a single memristor array and a constant-term circuit for realizing the synaptic matrix of a perceptron neural network [21].

Equation (4) is used for calculating the output voltage of the *k*th column. The output of each column is a summation of the weighted inputs, hence each column works as a perceptron neuron. In Equation (4), $\mathrm{M}_{j,k}$ is the memristance value of the crossing point between the *j*th row and *k*th column. R_B is a constant. The synaptic weight, $\mathrm{w}_{j,k}$, can be decided to be either negative or positive by adjusting the memristance, $\mathrm{M}_{j,k}$. The output of the perceptron neuron is decided by a threshold function which produces 0 or 1. By adding the comparator to the output voltage, $\mathrm{V}_{\mathrm{O},k}$, we can decide if the neuron's output of the *k*th column, OUT_k, should be activated or not.

$$\mathrm{OUT}_k = \begin{cases} 1, \text{ if } \mathrm{V}_{\mathrm{O},k} \geq \mathrm{V}_{\mathrm{REF}} \\ 0, \text{ if } \mathrm{V}_{\mathrm{O},k} < \mathrm{V}_{\mathrm{REF}} \end{cases}. \tag{5}$$

In previous work, the impact of wire resistance is ignored. However, in the crossbar array, the voltage drop along column and row lines cannot be omitted [19,24–27]. It becomes more serious when the array size increases [24]. The wire resistance between two adjacent junctions is modeled by a small-value resistor, r, as shown in Figure 2.

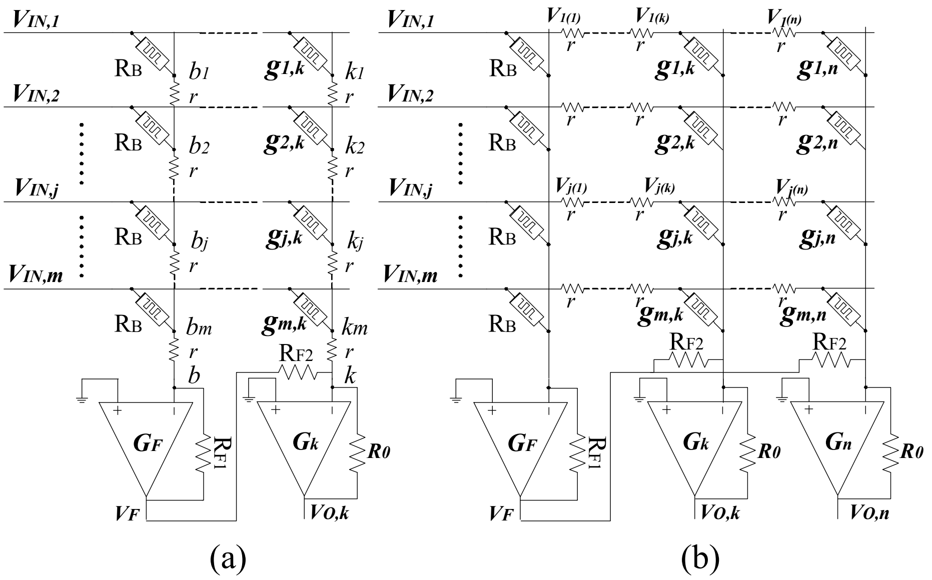


Figure 2. Wire resistance between two adjacent junctions is modeled by a small-value resistor, r, connecting between two crossing points. (**a**) Wire resistance on horizontal lines is omitted. (**b**) Wire resistance on vertical lines is omitted.

For the sake of simplicity, in this section we analyze the circuit separately with respect to the wire resistance on horizontal lines and the wire resistance on vertical lines, as shown in Figure 2a,b, respectively. We define $\mathrm{V_{b1}}$, $\mathrm{V_{b2}}$ as the voltages of node $\mathrm{b_1}$, $\mathrm{b_2}$, which are on the first column. Generally, $\mathrm{V}_{\mathrm{b}j}$ is the voltage of node b_j on the first column. Similarly, V_{kj} is the voltage of node k_j, which is on the jth column. Applying Kirchhoff current law for all nodes in Figure 2a, $\mathrm{V_F}$ and $\mathrm{V_{O,k}}$ can be estimated as follows:

$$\begin{aligned}\frac{-\mathrm{V_F}}{\mathrm{R_{F1}}} &= \frac{\mathrm{V_{IN,m}}-\mathrm{V_{bm}}}{\mathrm{R_B}} + \ldots + \frac{\mathrm{V}_{\mathrm{IN},j}-\mathrm{V}_{\mathrm{b}j}}{\mathrm{R_B}} + \ldots + \frac{\mathrm{V_{IN,1}}-\mathrm{V_{b1}}}{\mathrm{R_B}} \\ \mathrm{V_F} &= -\mathrm{R_{F1}}\left(\sum_{j=1}^{m}\frac{\mathrm{V}_{\mathrm{IN},j}}{\mathrm{R_B}} - \sum_{j=1}^{m}\frac{\mathrm{V}_{\mathrm{b}j}}{\mathrm{R_B}}\right).\end{aligned} \tag{6}$$

$$\begin{aligned}\frac{-\mathrm{V}_{\mathrm{O},k}}{\mathrm{R_0}} &= (\mathrm{V_{IN,m}} - \mathrm{V}_{k\mathrm{m}})\mathrm{g}_{\mathrm{m},k} + \ldots + \left(\mathrm{V}_{\mathrm{IN},j} - \mathrm{V}_{kj}\right)\mathrm{g}_{j,k} + \ldots + (\mathrm{V_{IN,1}} - \mathrm{V}_{k1})\mathrm{g}_{1,k} + \frac{\mathrm{V_F}}{\mathrm{R_{F2}}} \\ \mathrm{V}_{\mathrm{O},k} &= -\mathrm{R_0}\left(\sum_{j=1}^{m}\mathrm{V}_{\mathrm{IN},j}\mathrm{g}_{j,k} - \sum_{j=1}^{m}\mathrm{V}_{kj}\mathrm{g}_{j,k} + \frac{\mathrm{V_F}}{\mathrm{R_{F2}}}\right).\end{aligned} \tag{7}$$

If we assume that $\mathrm{R_{F1}} = \mathrm{R_{F2}}$, Equation (7) can be simplified as follow:

$$\mathrm{V}_{\mathrm{O},k} = -\left[\sum_{j=1}^{m}\left(\mathrm{R_0}\cdot \mathrm{g}_{j,k} - \frac{\mathrm{R_0}}{\mathrm{R_B}}\right)\mathrm{V}_{\mathrm{IN},j} - \sum_{j=1}^{m}\mathrm{R_0}\mathrm{V}_{kj}\mathrm{g}_{j,k} + \sum_{j=1}^{m}\mathrm{R_0}\frac{\mathrm{V}_{\mathrm{b}j}}{\mathrm{R_B}}\right]. \tag{8}$$

By comparing Equation (8) and Equation (4), we can derive the variation of voltage, ΔV, which is caused by wire resistance on the vertical lines.

$$\Delta\mathrm{V} = -\sum_{j=1}^{m}\mathrm{R_0}\frac{\mathrm{V}_{kj}}{\mathrm{M}_{j,k}} + \sum_{j=1}^{m}\mathrm{R_0}\frac{\mathrm{V}_{\mathrm{b}j}}{\mathrm{R_B}}. \tag{9}$$

Here $\mathrm{M}_{j,k}$ is the memristance of the crossing point between the jth row and the kth column. $\mathrm{V}_{\mathrm{b}j}$ and V_{kj} are the voltage at nodes $\mathrm{b_j}$ and $\mathrm{k_j}$ of the first column and the kth column, respectively, as shown in Figure 2a. $\mathrm{M}_{j,k}$ is calculated using Equation (4). It is possible to infer that the variation of voltage presented in Equation (9) can be very small because there are a negative term and a positive term in the right side of Equation (9).

In Figure 2b, wire resistance on vertical lines is omitted whereas wire resistance on horizontal lines is taken into account. The voltages applied to the columns decrease because they are lost from wire resistance. If we define $V_{j(k)}$ as the amount of voltage drop on wire resistance, which is on the *j*th row and between the (*k* − 1)th and *k*th column, the voltage applied to the *j*th row of the *k*th column is calculated as Equation (10).

$$V_{IN,j(k)} = V_{IN,j} - \sum_{i=1}^{k} V_{j(i)}. \tag{10}$$

Here $V_{IN,j(k)}$ is the voltage applied to the *j*th row of the *k*th column. The column-line voltage on the *k*th column, $V_{O,k}$, can be calculated using Equation (11).

$$V_{O,k} = -\left[\sum_{j=1}^{m}\left(R_0 \cdot g_{j,k} V_{IN,j(k)} - \frac{R_0}{R_B} V_{IN,j}\right)\right]. \tag{11}$$

By comparing Equation (11) and Equation (3), we obtain the variation of voltage, ΔV_k, of the *k*th column as follows.

$$\Delta V_k = \sum_{j=1}^{m} R_0 g_{j,k} V_{IN,j} - \sum_{j=1}^{m} R_0 g_{j,k} V_{IN,j(k)}. \tag{12}$$

Calculating $V_{IN,j(k)}$ by using Equation (10), we obtain ΔV_k as presented in Equation (13).

$$\Delta V_k = \sum_{j=1}^{m}\left(R_0 g_{j,k} \sum_{i=1}^{k} V_{j(i)}\right). \tag{13}$$

Here $\sum_{i=1}^{k} V_{j(i)}$ is the sum of the voltage on k resistors on the *j*th row. Equation (13) indicates that the output voltage of the *k*th column increases because of wire resistance. It is possible to infer that the column close to the first column has small voltage variation and the column far from the first column has large voltage variation. In Equation (13), the voltage variation increases proportionally to the column's index, *k*. Hence, it is interesting that two adjacent columns can have almost the same amount of voltage variation. Due to this reason, we propose a memristor crossbar array with compensating circuit to mitigate the voltage variation caused by wire resistance. By putting two adjacent columns into a subtraction circuit, the voltage variation can be eliminated significantly. The proposed memristor crossbar is schematically shown in Figure 3.

In Figure 3, the memristor crossbar is composed of 27 columns for recognizing 26 character images. The first column is a constant-term circuit to generate a negative voltage, as mentioned in the previous section. The remaining 26 columns represent 26 perception neurons trained to recognize the 26 characters. The differential amplifies from $G_{s,2}$ to $G_{s,26}$ are inserted into the circuit. The gain of these amplifiers is 1, so they work as the subtractors. The output voltages from $V_{O,1}$ to $V_{O,n}$ are the neuron's output of columns from Col_1 to Col_n. $V_{O,1}$ enter the comparator C_1 to decide if the neuron's output of column Col_1 should be activated or not. $V_{O,2}$ and $V_{O,1}$ go into $G_{s,2}$ that produces $V_{Os,2}$. $V_{Os,2}$ enters the comparator C_2 to decide if the neuron's output of column Col_2 should be activated or not. In general, the output voltage of the column Col_{k-1} and the column Col_k enter the subtractor $G_{s,k}$ for generating the neuron's output, $V_{Os,k}$, of the column Col_k. Using superposition theorem, $V_{Os,k}$ can be calculated with the difference of $V_{O,k-1}$ and $V_{O,k}$.

$$V_{Os,k} = -V_{O,k-1}\left(\frac{R_4}{R_3}\right) + V_{O,k}\left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{R_3 + R_4}{R_3}\right). \tag{14}$$

If we assume that $R_3 = R_4 = R_5 = R_6$, we can obtain:

$$V_{Os,k} = V_{O,k} - V_{O,k-1}. \tag{15}$$

The differential amplifier is able to reject any signal common to both inputs. That means, if two adjacent columns have almost the same amount of voltage variation, the voltage variation is then mitigated at the output.

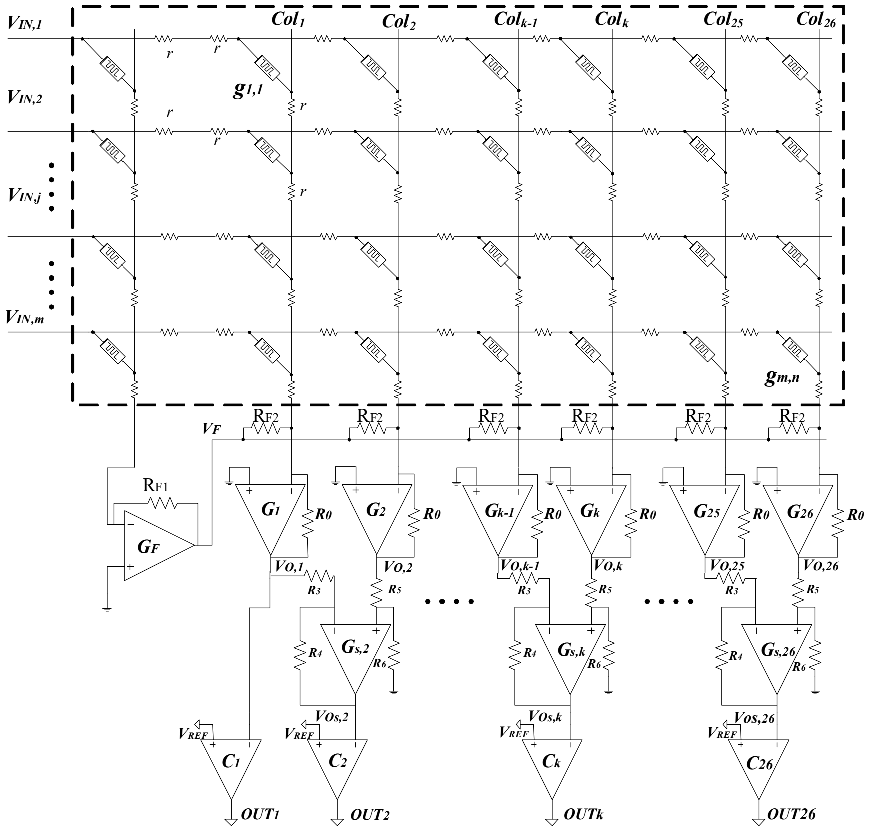


Figure 3. The proposed memristor crossbar with compensating circuit for implementing a perceptron neural network. The outputs of two adjacent columns are put into a differential amplifier working as a subtractor to eliminate the output voltage variation.

The concept of the proposed circuit is shown in Figure 4. The crossbar is trained to recognize the 26 characters from "A" to "Z". The 25th column is for recognizing the character "Y". The output of the 25th column is close to 1V when the input is "Y" and close to 0 when the other characters are applied to the input. Similarly, the neuron's output of the 26th column should be activated if the input is "Z", as indicated in Figure 4a. In Figure 4b, it is assumed that the wire resistance is present in the crossbar. The output voltage increases as reasoned in the previous section. The two last neurons recognize the input characters incorrectly, as demonstrated in Figure 4b. However, if we put the outputs of two last columns into a subtractor, the voltage variation can be mitigated significantly, as illustrated in Figure 4b. By doing this, we can maintain the recognition rate when wire resistance is present in the crossbar circuit.

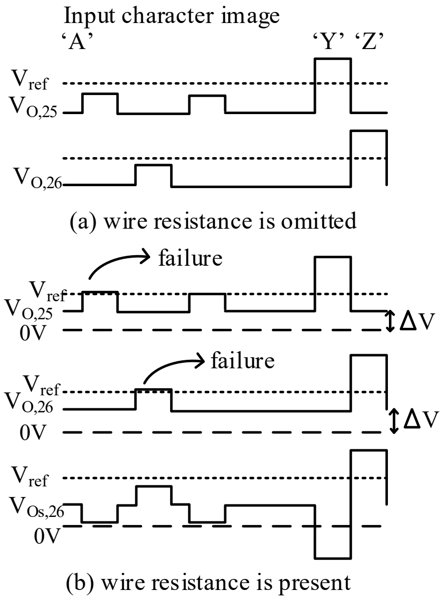
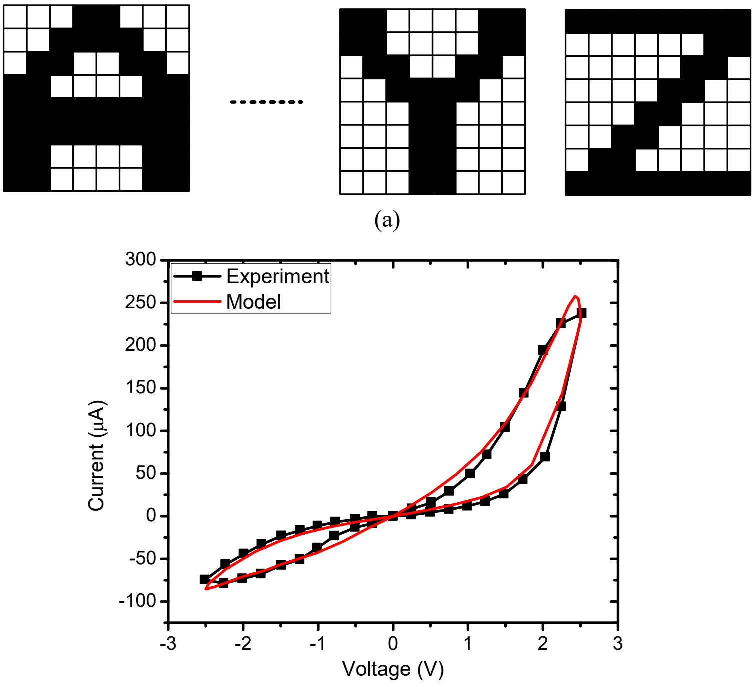


Figure 4. The concept of the proposed circuit for compensating the output voltage variation caused by wire resistance. (**a**) The ideal output of the 25th and 26th columns, which are trained to recognize character images of "Y" and "Z", respectively. (**b**) The output voltage of the 25th and 26th columns when the wire resistance is taken into account. $V_{Os,26}$ is the output of subtractor for the 26th column, as depicted in Figure 3.

3. Results

The proposed memristor crossbar circuit in Figure 3 is verified for the application of character recognition. Figure 5a shows eight × eight images of characters used in this simulation. Each character is composed of 64 black-and-white pixels. The proposed memristor crossbar is composed of 64 rows and 27 columns. The first column connects with all inputs through R_B to generate the negative voltage as mentioned in the previous section. The remaining 26 columns are for recognition of 26 characters from "A" to "Z". The 64 input voltages obtained from 64 pixels are applied to the inputs of 64 rows.

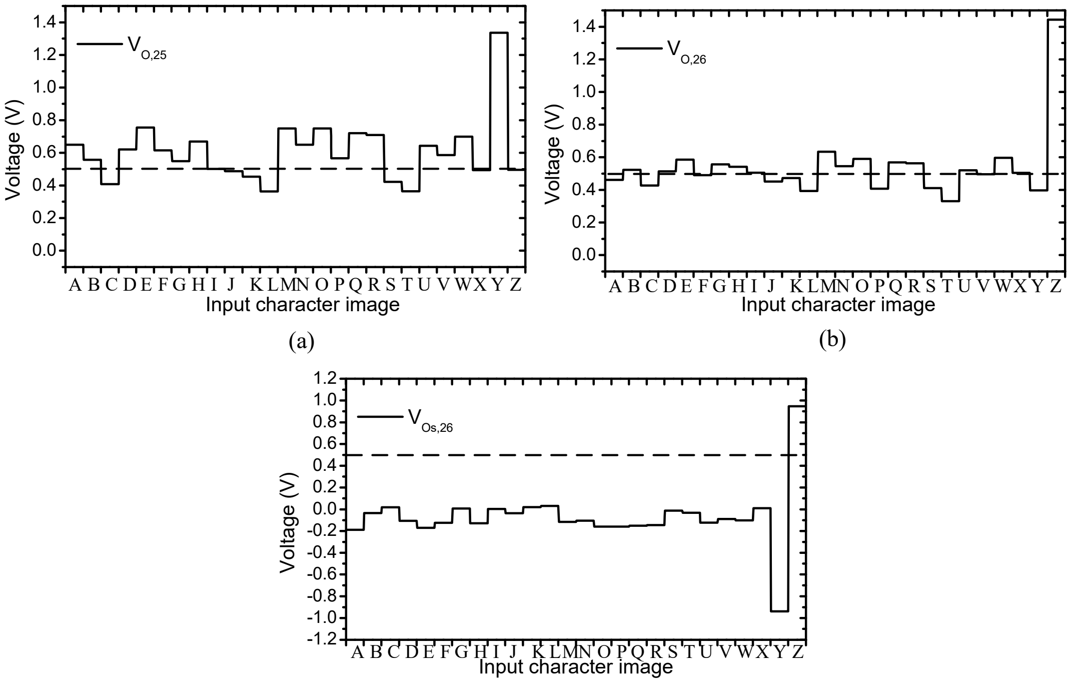
The red line in Figure 5b shows a hysteresis behavior of a real memristor based on the film structure of Pt/LaAlO$_3$/Nb-doped SrTiO$_3$ stacked layer [28]. The black line in Figure 5b represents the behavior model of the memristor used in this paper. This model can well describe various memristive behaviors that come from different kinds of memristors [29]. The circuit simulation is performed using the SPECTRE circuit simulation provided by Cadence Design Systems Inc. Memristors are modeled using Verilog-A and the CMOS technology is given by SAMSUNG 0.13 mm process technology [29,30]. The Verilog-A model parameters are presented in [28]. The wire resistance between two adjacent junctions is set to be 2.5 Ω for a 4F^2 cross-point structure [19,31]. Figure 6a shows the neuron's output of the 25th column, which is trained to be activated when character "Y" is applied to the input. Ideally, $V_{O,25}$ is close to 1V for character "Y", and close to 0V for others. However, the output voltage of the 25th column, $V_{O,25}$, is shifted up because of wire resistance, as reasoned in the previous section. Similarly, in Figure 6b, the neuron's output of the 26th column is shifted up as a result of the voltage drop along wire resistance. It can be realized that if we compare the column's output voltage, $V_{O,26}$, with the reference voltage, V_{REF}, the neuron's output of the 26th column can be activated for several input characters, which consequently degrades the recognition rate. The output voltage of the 25th column and the 26th column are put into a subtractor circuit to produce the neuron's output voltage of the 26th column, $V_{Os,26}$. By doing this, the voltage variation is mitigated significantly, as demonstrated in Figure 6c. When the character "Y" is applied to the inputs, $V_{Os,26}$ is negative, because $V_{O,25}$ is higher than $V_{O,26}$. For the character "Z", $V_{Os,26}$ is high, as indicated in Figure 6c. The simulation result shown in Figure 6c indicates that the neuron's output of the 26th column is only activated for the input character "Z", because the variation of voltage caused by wire resistance is mitigated remarkably by the subtractor circuit.



(a)

(b)

Figure 5. (**a**) The eight × eight pixels images of characters used to test the proposed memristor crossbar circuit. (**b**) The memristor's current–voltage characteristic measured from the real device and the memristor's behavior model [28,29].



(a)

(b)

(c)

Figure 6. The simulation result of the proposed memristor crossbar array depicted in Figure 4. (**a**) The neuron's output of the 25th column without compensating circuit. (**b**) The neuron's output of the 26th column without compensating circuit. (**d**) The neuron's output of the 26th column with compensating circuit. The wire resistance between two adjacent junctions is set to be 2.5 Ω [19,28].

The proposed circuit is tested with wire resistance that is varied from 0.5 to 2.5 Ω. This range of wire resistance is commonly used and obtained from the International Technology Roadmap for Semiconductors [24,25,31–34]. Figure 7 shows the comparison of the recognition rate between the memristor crossbar without compensating circuit and the proposed memristor crossbar with compensating circuit when the wire resistance is set to be 0.5, 1.0, 1.5, 2.0, and 2.5 Ω, respectively. The recognition rate of the memristor crossbar without compensating circuit declines dramatically when wire resistance increases. In particular, the recognition rate of the memristor crossbar without compensating circuit is 99%, 95%, and 81%, when the wire resistance is set to be 1.5, 2.0, and 2.5 Ω, respectively. By contrast, the proposed memristor crossbar with compensating circuit can maintain the recognition as high as 100% when wire resistance is as high as 2.5 Ω.

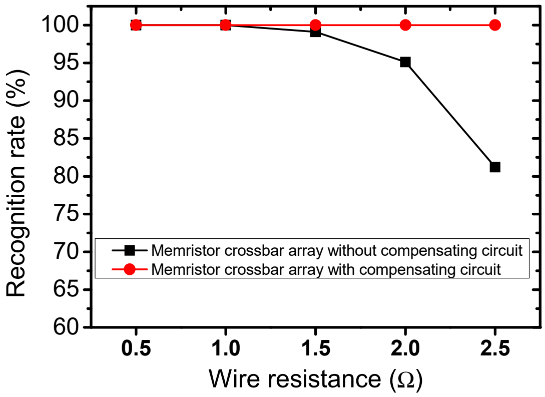


Figure 7. The comparison of the recognition rate between the memristor crossbar without compensating circuit and the proposed memristor crossbar with compensating circuit. The wire resistance is set to be 0.5, 1.0, 1.5, 2.0, and 2.5 Ω, respectively.

4. Discussion

Finally, we discuss the power and area overhead of the proposed memristor crossbar circuit. The proposed circuit uses the compensating circuit constituted by an Op-Amp and four resistors. The proposed circuit consumes more power and area, compared to the memristor crossbar without compensating circuit. However, the proposed memristor crossbar with compensating circuit shows better recognition rate by 19% than the previous memristor crossbar circuit, when wire resistance is set to be 2.5 Ω. Because wire resistance in the crossbar cannot be omitted, the proposed scheme makes the memristor crossbar-based perceptron neural network become more possible. The proposed circuit can be applied to memristor-based crossbar architectures which are used in resistive memory and artificial neural networks [34–36].

5. Conclusions

In this work, a memristor crossbar-based perceptron neural network with compensating circuit is proposed. The neuron's outputs of two columns are put into a subtractor circuit to eliminate the voltage variation caused by wire resistance. The memristor crossbar-based perceptron neural network is trained to recognize the 26 characters. The proposed memristor crossbar with compensating circuit shows better recognition rate, compared to the previous memristor crossbar without compensating circuit when wire resistance is taken into account. The simulation result shows that the proposed circuit can maintain the recognition rate as high as 100% when the wire resistance is set to be 2.5 Ω. By contrast, the recognition rate of the memristor crossbar without compensating circuit decreases by 19% when wire resistance is set to be 2.5 Ω.

Funding: This research received no external funding.

Conflicts of Interest: The author declares no conflicts of interest.

References

1. Mead, C. Neuromorphic electronic systems. *Proc. IEEE* **1990**, *78*, 1629–1636. [CrossRef]
2. Pacheco, P.S. *An Introduction to Parallel Programmin*; Elsevier: Amsterdam, The Netherlands, 2011.
3. Mirsa, J.; Saha, I. Artificial neural networks in hardware: A survey of two decades of progress. *Neurocomputing* **2010**, *74*, 239–255.
4. Himavathi, S.; Anitha, D.; Muthuramalingam, A. Feedforward neural network implementation in FPGA using layer multiplexing for effective resource utilization. *IEEE Trans. Neural Netw.* **2007**, *18*, 880–888. [CrossRef] [PubMed]
5. Du, Y.; Du, L.; Gu, X.; Du, J.; Wang, X.S.; Hu, B.; Jiang, M.; Chen, X.; Su, J.; Iye, S.S.; et al. An analog neural network computing engine using CMOS-compatible charge-trap-transistor (CTT). *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2018**, *38*, 1811–1819. [CrossRef]
6. Kawaguchia, M.; Ishiib, N.; Umeno, M. Analog neural circuit and hardware design of deep learning model. *Procedia Comput. Sci.* **2015**, *60*, 976–985. [CrossRef]
7. Wang, F.; Li, Y.X. Analog Circuit Design Automation Using Neural Network-Based Two-Level Genetic Programming. In Proceedings of the 2006 International Conference on Machine Learning and Cybernetics, Dalian, China, 13–16 August 2006.
8. Shima, T.; Kimura, T.; Kamatani, Y.; Itakura, T.; Fujita, Y.; Iida, T. Neuro chips with on-chip back-propagation and/or Hebbian learning. *IEEE J. Solid-State Circuits* **1992**, *27*, 1868–1875. [CrossRef]
9. Solomon, P.M. Device innovation and material challenges at the limit of CMOS technology. *Annu. Rev. Mater. Sci.* **2000**, *30*, 681–697. [CrossRef]
10. Brđanin, T.P.; Dokić, B. Strained silicon layer in CMOS technology. *Electronics* **2014**, *18*, 63–69.
11. Kügeler, C.; Meier, M.; Rosezin, R.; Gilles, S.; Waser, R. High density 3D memory architecture based on the resistive switching effect. *Solid State Electron.* **2009**, *53*, 1287–1292. [CrossRef]
12. Chua, L.O. Memristor—The missing circuit element. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519. [CrossRef]
13. Strukov, D.B.; Sinder, G.S.; Stewart, D.R.; Williams, R.S. The missing memristor found. *Nature* **2008**, *453*, 80–83. [CrossRef] [PubMed]
14. Jo, S.H.; Chang, T.; Ebong, I.; Bhadviya, B.B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Letters* **2010**, *10*, 1297–1301. [CrossRef] [PubMed]
15. Wang, H.; Li, H.; Pino, R.E. Memristor-based synapse design and training scheme for neuromorphic computing architecture. In Proceedings of the 2012 International Joint Conference on Neural Networks (IJCNN), Brisbane, Australia, 10–15 June 2012; pp. 1–5.
16. Kim, H.; Sad, M.P.; Yang, C.; Roska, T.; Chua, L.O. Neural synapse weighting with a pulse-based memristor circuit. *IEEE Trans. Circuit Syst.* **2012**, *59*, 148–158. [CrossRef]
17. Adhikari, S.P.; Yang, C.; Kim, H.; Chua, L.O. Memristor bridge synapse-based neural network and its learning. *IEEE Trans. Neural Netw. Learn. Syst.* **2012**, *23*, 1426–1435. [CrossRef] [PubMed]
18. Chen, Y.C.; Li, H.; Zhang, W.; Pino, R.E. The 3-D stacking bipolar RRAM for high density. *IEEE Trans. Nanotechnol.* **2012**, *11*, 948–956. [CrossRef]
19. Liang, J.; Wong, H.S.P. Cross-point memristor array without cell selector—Device characteristics and data storage pattern dependencies. *IEEE Trans. Electron. Device* **2010**, *57*, 2531–2538. [CrossRef]
20. Hu, M.; Li, H.; Wu, Q.; Rose, G.S.; Chen, Y. Memristor crossbar based hardware realization of BSB recall function. In Proceedings of the 2012 International Joint Conference on Neural Networks (IJCNN), Brisbane, Australia, 10–15 June 2012; pp. 1–7.
21. Truong, S.N.; Min, K.S. New memristor-based crossbar array architecture with 50-% area reduction and 48-% power saving for matrix-vector multiplication of analog neuromorphic computing. *J. Semicond. Technol. Sci.* **2014**, *14*, 356–363. [CrossRef]
22. Soudry, D.; Castro, D.D.; Gal, A.; Kolodny, A.; Kvatinsky, S. Memristor-Based Multilayer Neural Networks with Online Gradient Descent Training. *IEEE Trans. Neural Netw. Learn. Syst.* **2015**, *36*, 2048–2421. [CrossRef]
23. Wang, L.; Shen, Y.; Yin, Q.; Zhang, G. Adaptive synchronization of memristor-based neural networks with time-varying delays. *IEEE Trans. Neural Netw. Learn Syst.* **2014**, *26*, 2033–2042. [CrossRef]
24. Linn, E.; Rosezin, R.; Kügeler, C.; Waser, R. Complementary resistive switches for passive nanocrossbar memories. *Nature Mater.* **2010**, *9*, 403–406. [CrossRef]

25. Shin, S.H.; Byeon, S.D.; Song, J.S.; Truong, S.N.; Mo, H.S.; Kim, D.J.; Min, K.S. Dynamic reference scheme with improved read voltage margin for compensating cell-position and back ground-pattern dependencies in pure memristor array. *J. Semicond. Technol. Sci.* **2015**, *15*, 685–694. [CrossRef]
26. Levisse, A.; Royer, P.; Giraud, B.; Noel, J.P.; Moreau, M.; Portal, J.M. Architecture, design and technology guidelines for crosspoint memories. In Proceedings of the 2017 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), Newport, RI, USA, 25–26 July 2017.
27. Giraud, B.; Makosiej, A.; Boumchedda, R.; Gupta, N.; Levisse, A.; Vianello, E.; Noel, J.-P. Advanced memory solutions for emerging circuits and systems. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017.
28. Truong, S.N.; Pham, K.V.; Yang, W.; Shin, S.; Pedrotti, K.; Min, K.S. New pulse amplitude modulation for fine tuning of memristor synapses. *Mircoelectron. J.* **2016**, *55*, 162–168. [CrossRef]
29. Yakopcic, C.; Taha, T.M.; Subramanyam, G.; Pino, R.E.; Rogers, S. A memristor device model. *IEEE Electron Device Lett.* **2011**, *32*, 1436–1438. [CrossRef]
30. Spectre®Circuit Simulator User Guide. Available online: https://www.ee.columbia.edu/~{}harish/uploads/2/6/9/2/26925901/spectre_reference.pdf (accessed on 1 October 2019).
31. International Technology Roadmap for Semiconductors. 2007. Available online: https://www.semiconductors.org/wp-content/uploads/2018/08/2007Interconnect.pdf (accessed on 1 October 2019).
32. Kim, S.; Zhou, J.; Lu, W.D. Crossbar RRAM arrays: Selector device requirements during wire operation. *IEEE Trans. Electron. Devices* **2014**, *61*, 2820–2826.
33. Schindler, G.; Steinlesberger, G.; Engelhardt, M.; Steinhögl, W. Electrical characterization of copper interconnects with end-of-roadmap feature sizes. *Solid State Electron.* **2003**, *47*, 1233–1236. [CrossRef]
34. Kohonen, T. Self-organization and Associative Memory. In *Information Sciences*; Springer: Berlin/Heidelberg, Germany, 1989.
35. Li, C.; Belkin, D.; Li, Y.; Yan, P.; Hu, M.; Ge, N.; Jiang, H.; Montgomery, E.; Lin, P.; Wang, Z.; et al. Efficient and self-adaptive in-situ learning in multilayer memristor neural networks. *Nat. Commun.* **2018**, *9*, 2385. [CrossRef]
36. Caravelli, F.; Carbajal, J.P. Memristors for the curious outsider. *Technologies* **2018**, *6*, 118. [CrossRef]

© 2019 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).