Journal of Inorganic and General Chemistry
ZAAC
Zeitschrift für anorganische und allgemeine Chemie

DOI: 10.1002/zaac.201700270

REVIEW

Power Electronic Semiconductor Materials for Automotive and Energy Saving Applications – SiC, GaN, Ga_2O_3, and Diamond

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Dedicated to Professor Wolfgang Schnick on the Occasion of his 60th Birthday

Abstract. Power electronics belongs to the future key technologies in order to increase system efficiency as well as performance in automotive and energy saving applications. Silicon is the major material for electronic switches since decades. Advanced fabrication processes and sophisticated electronic device designs have optimized the silicon electronic device performance almost to their theoretical limit. Therefore, to increase the system performance, new materials that exhibit physical and chemical properties beyond silicon need to be explored. A number of wide bandgap semiconductors like silicon carbide, gallium nitride, gallium oxide, and diamond exhibit outstanding characteristics that may pave the way to new performance levels. The review will introduce these materials by (i) highlighting their properties, (ii) introducing the challenges in materials growth, and (iii) outlining limits that need innovation steps in materials processing to outperform current technologies.

1 Introduction

Automotive and energy saving applications include a number of electronic switching systems capable to distribute electrical power between energy supply, storage, and consumption devices. The performance level may range from (i) low power (10 W to 1 kW) and low voltage (< 400 V) applications like power supplies for consumer electronics and low performance mechatronic systems, via (ii) mid power (1 kW to 100 kW) and mid voltage (400 V to 1.2 kV) applications like electric motor controls, photovoltaic inverters, electric vehicle drives, and universal power supplies to (iii) high power (MW to GW) and high voltage (mainly 1.7 kV to 6.5 kV, but certain devices at higher voltages) applications like rail transport, ships, wind mills, and smart power grid. Basically in all cases the control and transformation of electrical currents (AC → AC, AC → DC, DC → AC, and DC → DC) stand in the foreground.

For high power devices and systems, reliability is the most important issue. Therefore novel materials with extraordinary properties may be used. Opposite, in the low power case, manufacturing costs dominate by far and established mass production processing technologies using standard materials stand in the foreground. In the mid power range, reliability and costs have to be balanced. New technologies are needed but they need to be based on large area, high throughput processing routes.

In power electronics semiconductor diodes and transistors that are able to operate at high voltages, currents, and power densities as well as increasingly higher switching frequencies of several hundred kilohertz are necessary. From a materials perspective the prerequisites may be broken down to three physical properties: (i) a high break down field E_B enables electronic devices to withstand high voltages during operation and provides a great robustness against unintentional operation failure, (ii) a large heat-conductivity λ improves the dissipation of heat loss and lowers the device operation temperature, and (iii) a great charge carrier saturation velocity vs. supports high frequency operation for more efficient electric power con-

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Peter Wellmann is a professor for materials science at the Friedrich-Alexander Universität Erlangen-Nürnberg (Germany). His research focuses on fundamentals as well as applied technology of crystal growth and epitaxy of wide bandgap semiconductors with a special emphasis on silicon carbide. To his specialties belong in-situ visualization of the growth process using modern X-ray visualization in 2D and 3D and advanced doping. Another activity is devoted to processing and characterization of the thin film solar cell material $CuIn_xGa_{1-x}Se_yS_{1-y}$. From 1996 to 1998 Peter Wellmann spent two years for postdoctoral research at the Materials Department of the University of California in Santa Barbara (USA). In addition he accepted invited professorships at the Institut National Polytechnique Grenoble (France) in 2004 and at the Université Montpellier 2 (France) in 2006.

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Table 1. Physical properties (room temperature values) of wide bandgap semiconductors for power electronic applications in comparison to the classic materials (data from references[1,2,78]).

	SiC	GaN	Ga_2O_3	C	Si	GaAs
E_G /eV	2.3…3.3	3.44	4.8	5.0	1.1	1.4
E_B /10^5 V·cm^{-1}	40	60	80	100	4	5
λ /W·cm^{-1}·K^{-1}	3…5	1.3	0.23	20	1.5	0.5
vs. [10^7 cm·s^{-1}	2.5	2.5	2	2.7	1	2
Lattice parameter						
a /Å	3.08 (hex)	3.19	12.23	3.57	5.43	5.65
b /Å			3.04			
c /Å			5.80			
β /°			103.7			
T_S /°C	2830	2500	1940	3900	1420	1250

verters. Interestingly, those wide bandgap (E_G) semiconductors that predominantly exhibit covalent chemical bonds (low *ionicity*) fulfil these requirements much better than classic semiconductors like Si and GaAs. Table 1 summarizes the key physical properties of the wide bandgap semiconductors SiC, GaN, Ga_2O_3 and C (= diamond) in comparison to their classic counterparts Si and GaAs.

Typically, the wide bandgap semiconductors summarized in Table 1 exhibit a small lattice parameter and a high melting or dissociation temperature T_S. In reciprocal space (*k*-space) this leads to an energy dispersion E(k) of the valence and conduction bands represented by a large effective electron (hole) mass and, hence, a low intrinsic charge carrier mobility. Irrespective of this, due to the great charge carrier saturation velocities $v_s > 2\times10^7$ cm·s^{-1} as well as due to the break down field values $E_B > 40\times10^5$ V·cm^{-1}, these wide bandgap materials meet the requirements for high frequency electronic device operation.

Related to the short bond lengths in the crystal structures as well as related to the strong chemical bonds, all wide bandgap materials in Table 1 exhibit elevated dissociation temperatures. While Ga_2O_3 may be grown from a stoichiometric melt, all other semiconductors, i.e. SiC, GaN, and C (diamond) need special vapor growth techniques or other high pressures processes under harsh environments as described in the forthcoming sections.

Another typical feature of the wide bandgap materials in Table 1 is the occurrence of various stable crystal polytypes.

(i) The most prominent example is silicon carbide that exhibits a large number of different stacking sequences of the Si–C double layers. In these structures, each Si is surrounded by four C atoms and vice versa. Physically mainly the electronic bandgap as well as the charge carrier mobility μ varies (Table 2), although the cubic 3C-SiC polytype also exhibits a slightly lower breakdown field (Table 2).

Table 2. Physical properties (room temperature values) of various SiC polytypes (data from references[1,2]).

	4H-SiC	6H-SiC	3C-SiC	15R-SiC
E_G /eV	3.23	3.98	2.36	2.96
E_B /10^5 V·cm^{-1}	40		25	
μ_n /cm^2·V^{-1}·s^{-1}	400	300	900	800

(ii) In the case of gallium nitride two polytypes are observed: The technological relevant hexagonal, chemically stable 2H-GaN as well as the metastable 3C-GaN counterpart.

(iii) Although electronically quite different, diamond (sp^3 carbon) and graphite (sp^2 carbon) may also called a polytypic variation of crystalline carbon.

(iv) In the case of gallium oxide the monoclinic, so called β-Ga_2O_3, is the most important crystal structure with respect to electronic applications.

In the following review, each materials section on SiC, GaN, Ga_2O_3, and Diamond starts with historic remarks that conduct its discovery or materials development. A brief description of the phase diagram of the material is followed by an introduction into the growth methods applied for the processing of single crystalline boules. Finally, special materials issues and applications are highlighted. Materials-wise, the section on SiC significantly includes own research results of the author with special emphasis on large area growth of SiC as well as in-situ process visualization of the growth process. In the case of the sections on GaN, Ga_2O_3, and Diamond the review is mainly based on literature data.

2 Silicon Carbide

In terms of novel semiconductor materials beyond silicon for power electronic devices, silicon carbide exhibits the most mature technology with fast growth market share. High performance device operation is limited by the provision of semiconductor wafers with low defect densities. Both, improvement of the crystal growth technology as well as deepening of the fundamental understanding of the crystal growth process are mandatory to make full use of the extraordinary physical properties of SiC as listed in Section 1.

2.1 Phase Diagram and Growth Methods of Silicon Carbide

Figure 1 shows the phase diagram of silicon carbide with its peritectic decomposition of the stoichiometric SiC phase at ca. 2830 °C.[3]

Hereby SiC decomposes into carbon and a silicon rich solution of up to 13 at% of carbon. In crystal growth technology SiC boules are mainly grown from the vapor by the so called physical vapor transport (PVT) method (Figure 2). Sublimation of stoichiometric SiC source material (usually SiC powder) is carried out at elevated temperatures above 2000 °C in an inductively heated closed graphite crucible surrounded by graphite foam or felt as isolating material. Crystallization is

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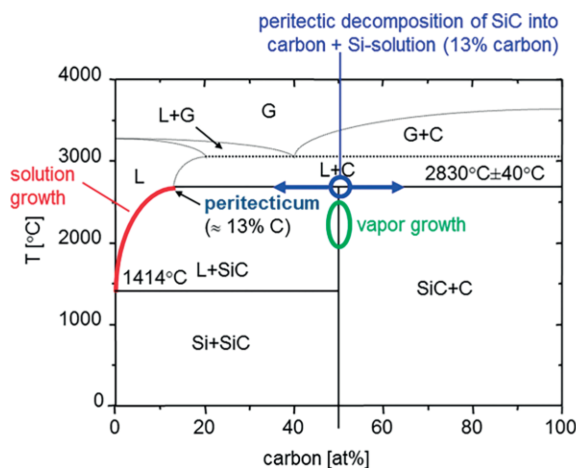

Figure 1. Phase diagram of SiC and routes of crystal growth using sublimation or solution growth.

conducted at slightly lower temperatures (e.g. ΔT = 50 °C) on a mainly (0001) oriented seed crystal. Today, this technology may be called mature, although crystal size enlargement from currently 100 mm to 150 mm and even 200 mm as well as reduction of the defect density and strain related wafer bow are challenging issues. The development of the PVT technique may be traced back to the fundamental works of *Lely*,[3] *Tairov*, and *Tsvetkov*,[4] as well as *Ziegler* et al.[5] In order to establish the SiC mass transport from the bottom of the crucible (SiC powder source) to its top (crystal growth interface), an axial temperature gradient is mandatory. Since the mass transport is initiated by a temperature gradient, the growing crystal by default will be exposed to thermally induced stress in axial as well as radial direction. The reduction of defect density needs to account for this intrinsic boundary condition.

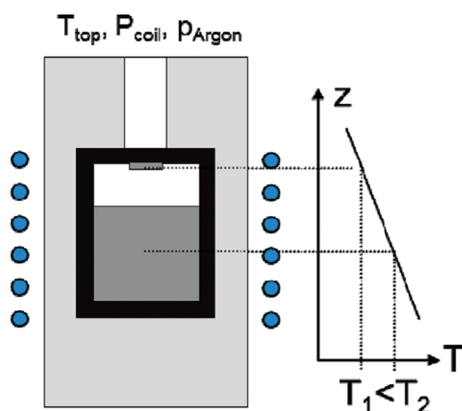

Figure 2. Schematic sketch of a growth cell for the processing of SiC using the physical vapor transport method.

The applied graphite parts usually exhibit a porosity of at least a few percent and therefore feature a permeable behavior for inert gases like argon and nitrogen. Therefore, n-type doping using the donor nitrogen in SiC may be carried out simply by the supply of nitrogen gas into the growth chamber. In the case of p-type doping using the acceptor boron or aluminum solid sources that are sublimed as addition to the SiC powder source or from an external dopant reservoir[6,7] are applied. While n-type doping using nitrogen gas is well controlled, in particular p-type doping using aluminum is quite challenging. Due to its much higher partial pressure than SiC at growth temperature, feeding of the dopant through an extra pipe into the growth cell is necessary.[7]

At temperatures between 2000 °C and 2400 °C the gas phase of the subliming SiC powder is composed of mainly Si, Si_2C, and SiC_2 but hardly of SiC molecules.[8] By the application of the inert gas argon (pressure = 10 mbar to 50 mbar) the growth process may be conducted in diffusion limited mode. Typical growth rates lie between ca. 200 $\mu m \cdot h^{-1}$ and 300 $\mu m \cdot h^{-1}$ and may be as much as 500 $\mu m \cdot h^{-1}$ to 1000 $\mu m \cdot h^{-1}$ but with increasingly challenge with increasing growth rate to obtain uniform material. A critical issue is the minimization of the radial temperature gradient in order to keep the residual sheer stress in the growing crystal as low as possible. The control of the temperature and the partially related gas species concentration fields are the main objectives during growth process optimization.[9–14] For a review it is related to reference[15].

Related to the PVT process a high temperature chemical vapor deposition (HT-CVD) technique has been developed[16,17] that also operates above 2000 °C. Instead of SiC as source material, HT-CVD makes use of gaseous precursors like silane (SiH_4) and ethylene (C_2H_4) that decompose at elevated temperature to form SiC clusters that act as sublimation source for the growth of the SiC boule. The technologic strength to apply HT-CVD lies in the advanced p-type doping capability using aluminum precursors like tri-methyl-aluminum (TMA) as well as in the fabrication of high purity SiC boules. Challenges features are achieving continuous growth at high growth rates as well as suppressing unintentional secondary deposits. Compared to PVT, the handling of toxic gases causes higher operation costs during operation of HT-CVD.

The other SiC growth route is based on crystallization from a Si-rich Si-C solution. The addition of further elements to enhance the carbon solubility may be applied. Within the last two decades significant progress in solution growth has been achieved. Initial studies of growth on 2 inch SiC seeds were done by *Hofmann* and *Müller*[18] and refined by *Epelbaum* et al.[19] The control of the carbon concentration in the Si-based melt and the transport of carbon to the growth interface require special attention during solution growth. Often graphite crucibles are applied, which are intentionally partially dissolved by the silicon solvent. Noteworthy is that the wetting behavior of silicon based solutions strongly depends on the graphite micromorphology. Despite all experimental obstacles, an increasing number of research reports in recent years (see, for example[20,21]) demonstrate how the fundamental understanding the SiC solution growth process significantly improved.

Most reports on solution growth follow the top seeded solution growth (TSSG) approach at temperatures below 2000 °C that use metal additives like Cr, Ti, and Al to increase the carbon solubility in the Si melt. At these temperatures the lower Si partial pressure enables a growth configuration based on a classic Czochralski setup. Using Si-Cr and Si-Ti solution

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at a growth temperature of 1940 °C, *Kusunoki* et al.[21] reported for a crystal diameter of 75 mm a growth rate of 200 μm·h^{-1}. In the case of smaller crystal diameters, growth rates above 1 mm·h^{-1} were reached. In general, during solution growth of SiC, metal additives are incorporated up to their solubility limit into the SiC crystal, which may alter the electronic properties of the semiconductor substrate. Recently it was reported from the author's team that the vertical Bridgman / vertical gradient freeze method can be applied at temperatures as high as 2300 °C using a metal free silicon-carbon solution of very high purity to perform SiC solution growth.[22] This growth configuration could solve the current challenge of unintentional doping of the SiC crystal by the metal additives during solution growth based on the Czochralski-like process.

The growth from the melt is carried out close to thermodynamic equilibrium and therefore usually leads to a lower dislocation density than other methods like PVT. Using solution growth a high structural quality of SiC[23] and the possibility to close micropipes was demonstrated.[19,24] Whether the application of solution growth will eventually lead to the fabrication of large area 4H-SiC boules for power electronic applications cannot be foreseen today. In the author's opinion, key points for the commercial success of solution growth of SiC crystals are the realization of long term stable growth conditions for the growth of long crystal boules as well as the cost reduction by an efficient re-usage of the crucible materials and the solvent Si.

2.2 In-situ X-ray Visualization of the Growth Process

The closed graphite crucible exhibits a rather limited growth process control. Temperature measurements using optical pyrometers at the top as well as at the bottom of the crucible and numerical simulation of the temperature field are used to derive the conditions inside the growth cell. The reliability of these data, however, strongly depends on the knowledge of the thermal and electrical properties of the graphite components and the SiC source material. A real drawback compared to the Czochralski growth process of Si is the lack of an optical access to the crystal growth context. In this context, the development of in-situ 2D and 3D X-ray based monitoring[25,26,15] has significantly improved the control of the growth process. Besides the crystal growth interface, major insight into the sublimation-recrystallization and related materials densification of the SiC source material has been achieved. In its most advanced stage, in-situ 3D X-ray computed tomography is applied (Figure 3).[15]

The growth cell is rotated continuously or in a number of single steps during the in-situ visualization, while simultaneously acquiring 2D X-ray projection images (Figure 3). Applied to a PVT growth machine for the growth of 3 inch SiC crystals, a tungsten X-ray source (DC voltage = 125 kV peak, maximum cw current = 350 μA, spot size = 70 μm,) and a flat panel X-ray detector [PaxScan 2520D/CL, Varian Medical Systems, CsI scintillator layer, active matrix of 1496 × 1874 pixels, pitch size = 127 μm^2 (3.94 lp·mm^{-1})] are used for high throughput image acquisition. With a frame rate of up to 30

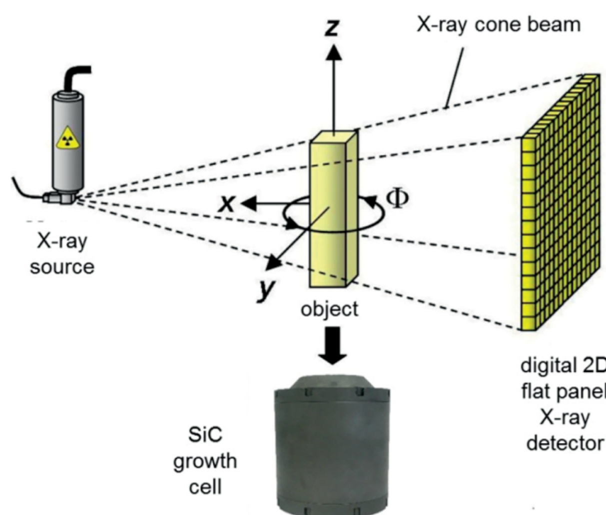

Figure 3. Sketch of the setup to visualize the PVT growth process using in-situ X-ray computed tomography.

fps in a 2 × 2 binning mode (10 fps without binning) the so called fly-by-measurements were carried out where the growth setup is continuously rotated during data acquisition. In the standard mode 2D X-ray images are collected in a stop-and-go-mode. The 3D image processing is conducted using a series of 200 to 400 2D X-ray projection images in conjunction with the classic so called filtered back-projection Feldkamp-algorithm.[27] The typical 3D image acquisition time lies between 3 min and 15 min. The special resolution of the setup is ca. 125 μm (voxel size). At typical crystal growth rates between 200 μm·h^{-1} and 500 μm·h^{-1} 3D the image acquisition is performed without further spatial resolution losses.

Figure 4 shows a series of in-situ 3D views into the hot crystal growth cell at ca. 2200 °C. Within this overview-projections the crystal growth process (enlargement of the crystal height) as well as the consumption of the SiC powder in the

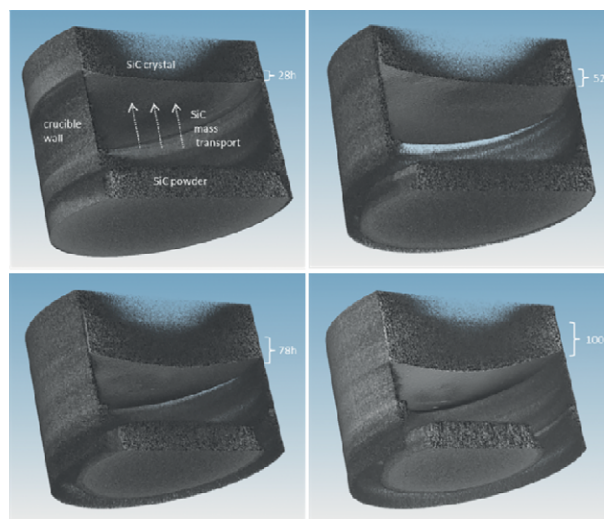

Figure 4. A series of live images of the PVT growth process at ca. 2200 °C acquired using in-situ X-ray computed tomography.

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periphery of the crucible is clearly observed after 28 h, 52 h, 78 h, and 100 h. For a further analysis 2D image cuts from the 3D computed tomography data set can be used (see, for example reference[15]). Detailed studies of the SiC powder consumption have been carried out recently as the source material consumption is the main limit for long growth periods.[28] While the advanced 3D X-ray computed tomography enables fundamental research studies, the less complex 2D X-ray visualization[25] may be applied during standard crystal growth in a production environment.

2.3 The Hexagonal 4H-SiC Polytype

Growth of 4H-SiC for power electronic applications is performed on (000–1) oriented carbon face seeds (Figure 5). In some cases, 2° or 4° off oriented seeds are applied. The 4H-SiC polytype stability is observed in a C-rich gas phase composition at higher supersaturation compared to the growth of 6H, i.e. higher axial temperature gradient compared to the average temperature.[29] In the case of diffusion limited growth using argon inert gas, no polytype stability dependence on the inert gas pressure has been reported so far.[29] Nitrogen doping stabilizes the growth of 4H-SiC boules.[30] Crystal defects in the SiC crystal that limit the electronic device operation include dislocations, stacking faults, carbon inclusions, and silicon droplets as well as macroscopic hollow core defects.[31] It has been reported that basal plane dislocations dramatically limit device stability of bipolar diodes. *Bergman* at al.[32] reported an electron-hole-pair-recombination driven enhancement of stacking fault generation, which strongly deteriorates the bipolar device performance. Unipolar devices like Schottky diodes are altered by threading screw dislocation densities.[33] Threading screw dislocations and in particular basal plane dislocations cause a device breakdown along the metal oxide / SiC interfaces.[34] Micropipes that mainly stem from threading screw dislocations[35,36] cause immediate device failure. From this list it follows that the reduction of the dislocation density is the main task during crystal growth. In this context tailoring of the temperature field in terms of low radial gradients throughout the complete process time as well as during cooling down of the crystal after growth are the main challenges. Numerical simulation of the steady state and transient temperature fields inside the growth cell are key issues. Experimentally the process control is carried out by the setting of the inductive heating power and the simultaneous monitoring of the temperature at the top and bottom of the growth cell. Process optimization is carried out in an iterative sequence of numerical simulation of the temperature field, step-by-step tailoring of the geometry of the growth cell and application of the adapted growth configuration to experiments. Figure 5 shows an optical image of an as grown 100 mm single crystal that has been oxidized to remove residual carbon from the crystal surface. The various colors are related to a thin SiO_2 surface layer.

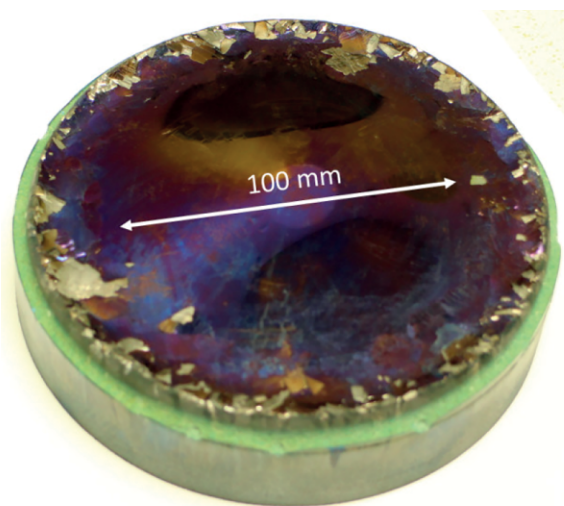

Figure 5. Optical image of an as grown 100 mm single crystalline 4H-SiC boule.

2.4 The Cubic 3C-SiC Polytype

Since the beginning of research and development of the semiconductor SiC, the cubic polytype 3C-SiC has been of particular interest due to its higher electron mobility compared to the hexagonal 4H-SiC (Table 2). In addition, due to lower bandgap of E_g(3C-SiC) = 2.3 eV versus of E_g(4H-SiC) = 3.2 eV, its metal SiO_2 semiconductor (MOS) interface exhibits a significantly lower defect density, which is beneficial for metal oxide semiconductor field-effect transistor (MOS-FET) applications.[37–39] Recent results have demonstrated a MOSFET channel mobility of 300 cm^2/Vs for 3C-SiC, which outperforms the 4H-SiC counterpart with a channel mobility below 100 $cm^2 \cdot cm^{-1}$. Compared to 4H-SiC, however, polytype stability during 3C-SiC bulk growth is much lower and therefore the crystal defect density much higher. Among others, proper growth parameters of 3C-SiC include a high supersaturation, a high temperature gradient and a silicon rich gas phase. So far basically no large area seeds are available. The difficulties to realize bulk 3C-SiC may be related to a challenging nucleation and preservation of the 3C-SiC polytype. Besides polytype changes, stacking faults (SFs), double positioning grain boundaries (DPBs) and antiphase boundaries (APBs) are the most prominent defects known in 3C-SiC. Due to all of the growth obstacles, it was considered from the beginning of 3C-SiC growth development on to perform heteroepitaxial bulk seeding either on (100) or (111) 3C-SiC epitaxial layers that were fabricated on (100) or (111) Si substrates or bulk seeding on hexagonal (0001) oriented 6H-SiC and 4H-SiC substrates.

Beside this, various approaches have been followed in recent years to grow bulk or at least bulk-like 3C-SiC (see, for example, references[40–52]). All these studies have established a broad knowledge for the successful growth of 3C-SiC bulk material. Together with great advances in growth reactor technology first large area, bulk-like 3C-SiC was demonstrated recently by the author's team. The PVT-like growth of (100) 3C-SiC is carried on (100) 3C-SiC-on-Si seeding layer fabricated by chemical vapor deposition (CVD). A critical step in this technology is the transfer of the thin 3C-SiC seeding layers

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(thickness ca. 12 µm to 50 µm) from the silicon wafer to a high temperature stable carrier. Figure 6 illustrates the transfer process that consists etching of the Si-wafer using a HNO_3 + HF solution, deposition of a carbon glue on top of the 3C-SiC layer and mechanical transfer to a poly-crystalline SiC carrier.[53,54] The resulting seeding stack was used in a subsequent PVT-like growth process to form quasi bulk 3C-SiC of an area of up to 10.5 cm^2 and a thickness of up to 0.9 mm (Figure 7).[53,54] The 3C-SiC was free of double position and antiphase boundaries and exhibited no polytype switches. The presented result is believed to be a major step towards real bulk 3C-SiC in the near future.

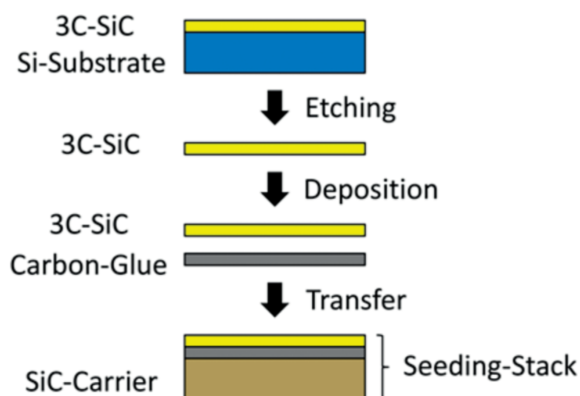

Figure 6. Seed preparation for 3C-SiC growth on 3C-SiC-on-Si CVD seeding layers.

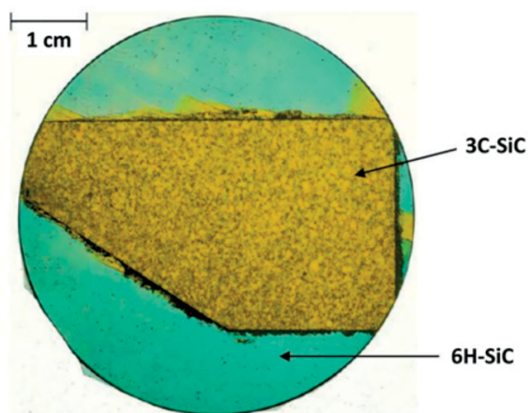

Figure 7. Optical image of an as grown yellow 3C-SiC bulk like crystal (area = 10.5 cm^2, thickness = ca. 0.5 mm) on its green 6H-SiC carrier.

2.5 The Rhombohedral 15R-SiC Polytype

Another high potential silicon carbide polytype is the rhombohedral 15R-SiC. This polytype exhibits an even greater electron mobility than cubic 3C-SiC (Table 2) and a lower bandgap than 4H-SiC. It may be grown in a quite narrow process window on the Si face of (0001) hexagonal SiC in a Si-rich gas phase environment.[55] Despite its great potential in power electronic application, this polytype is currently solely under fundamental academic investigation.

2.6 Novel Applications of SiC

Other than power electronic applications, the hexagonal and cubic SiC polytypes have recently shown new high potential applications.

Co-doping of 6H-SiC and 4H-SiC with nitrogen and boron as well as nitrogen and aluminum showed its great applicability as fluorescent SiC in white LED application.[56,57]

Cubic silicon carbide doped with the deep boron acceptor is a candidate for an intermediate band solar cell material with theoretical light conversion efficiencies above 50 %.[58,59]

Finally, p-type 3C-SiC doped with aluminum is currently studied for the application in solar driven water splitting.[60,61]

The success of SiC in these various high potential applications depends much on the progress in materials preparation. Recent advances in 3C-SiC may pave the way for a number of new applications of SiC beside the technology-driver of power electronics.

3 Gallium Nitride

3.1 Phase Diagram and Growth Methods of GaN

In the case of GaN the high partial pressure of nitrogen of ca. 4.5×10^3 MPa at the materials dissociation temperature of ca. 2500 °C is the characteristic feature that routes potential growth techniques. Although AlN has no obvious application in power electronic devices so far, it is worth summarizing its bulk growth capabilities with respect to a potential transfer to GaN. The dissociation temperature of crystalline AlN lies around 3200 °C, however, the nitrogen decomposition pressure of ca. 20 MPa is quite low compared to 4.5×10^3 MPa in case of GaN. Like in the case of SiC, AlN single crystals may be processed by the physical vapor transport method.[62–64] A significant number of current growth studies are carried out by teams that also investigated SiC bulk growth in the past. As crucible materials either tungsten or tantalum (tantalum carbide) are used. Special emphasis has to be put on the purity of the AlN powder source material. In particular the oxygen contamination needs to be lowered as much as possible. The applied crucible material impacts the gas phase chemistry. In the case of tungsten, growth is carried out on (0001) N-polar seeds. A significant crystal diameter reduction occurs during sublimation growth that causes the need to use foreign substrates like 6H-SiC wafers and hetero-epitaxial seeding with its drawback of initially high dislocation density in the AlN crystal boule. Growth in tantalum (or tantalum carbide) crucible may be carried out on (0001) Al-polar seeds that enables a radial extension of the single crystal diameter and may be favored for homo-epitaxial seeding on AlN wafers. A drawback of the tantalum based crucible system is the lower crystal purity, which causes strong optical below bandgap absorption in the ultraviolet light spectrum for the material.

As pointed out above, in the case of GaN the nitrogen component exhibits a much higher partial pressure at the dissociation temperature compared to AlN. In practice, classic physical vapor transport cannot be applied as bulk growth method

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for GaN above 2000 °C. In the past, PVT related growth has been proposed[65] but did not succeed so far on a large scale. The best single crystalline GaN boules have been prepare by the hydrogenated vapor phase epitaxial growth (HVPE)[66,67] and by the ammonothermal crystallization under ammonobasic conditions.[68,69]

While in particular power opto-electronic laser and light-emitting diodes benefit from bulk GaN seeding wafers, for power electronic applications another approach is favored (which is based on hetero-epitaxial growth of GaN on large silicon wafers). Due to the quite low heat conductivity of GaN that blocks heat dissipation during power electron device operation, the major application field of GaN lies in the lower voltage range between 200 V and 600 V, which basically bridges between the semiconductors Si (low voltage, 200 V to 400 V) and 4H-SiC (high voltage, 1200 V and above). This voltage range targets electronic devices for automotive and energy applications that face extreme cost pressure. In this context the hetero-epitaxial processing of GaN layers on large area Si wafers is coherent. It is noteworthy that the cubic 3C-SiC polytype semiconductor aims into the same 600 V device application. The material GaN, however, profits if high device switching frequencies are needed rather than if power comes to the fore.

3.2 Growth of GaN on Si-Seed-Wafers

A major breakthrough to process GaN epitaxial layers on (111) Si-wafers was developed by *Dadgar*, *Krost* et al.[70–72] Their development is based much on fundamental studies by *Watanabe*, *Amano*, *Akasaki* et al.[73,74] and *Hearne* et al.[75]

The (111) orientation of Si is applied as substrate to force the hetero-epitaxial nucleation of the hexagonal 2H-GaN polytype. Besides the lattice mismatch between Si and GaN of ca. 16 %, the difference in thermal expansion α is the more serious problem. As a consequence, optimization of the growth of GaN on Si is inherent with tailoring of residual layer GaN stress towards residual compressive strain that inhibits layer cracking.

GaN exhibits a larger α-value than Si; i.e. $\alpha(\text{GaN}) = 5.59 \times 10^{-6}\ \text{K}^{-1}$ (T = 300 K to 900 K)[76] vs. $\alpha(\text{Si}) = 3.77 \times 10^{-6}\ \text{K}^{-1}$ (T = 300 K to 900 K),[77] which causes tensile stress in the hetero-epitaxially grown GaN layer after cooling down to room temperature. As a consequence, GaN layer cracking is a severe problem. For comparison please note: The standard GaN substrate exhibits an α-value of $\alpha(\text{GaN}) = 7.5 \times 10^{-6}\ \text{K}^{-1}$,[76] which causes compressive strain in the epitaxial layer without cracking.

Watanabe, *Amano*, *Akasaki*, and their co-workers[73,74] introduced the application of low temperature grown, thin AlN interlayers (= LT-AlN) to compensate in grown stress in the GaN from tensile to compressive strain. *Dadgar*, *Krost*, and their co-worker[70,71] basically integrate two ca. 40 nm thin LT-AlN interlayers into three ca. 400 nm thick high temperature grown GaN layers (= HT-GaN) to achieve compressive strain and basically leading to no cracking in GaN material on Si.

Dadgar, *Krost*, and their co-workers[72] carried out an additional key development. Doping of GaN is usually carried out by Si through an addition of silane (SiH_4) to the epitaxial GaN growth process. In highly n-type doped GaN layers, however, this may lead again to tensile stress and cracking in the epitaxial film. Through the exchange of the dopant Si by Ge using germane (GeH_4) as doping gas the compressive GaN layer strain could be preserved and cracking was inhibited. In addition, greater layer conductivities could be realized through the usage of Ge as donor.

The combined tailoring of GaN epitaxial films grown on (111) Si through the addition of LT-AlN interlayers and through the replacement of Si n-type doping of GaN using Ge are key features for a technologic application of GaN films on Si-wafers.

4 Gallium Oxide

4.1 Phase Diagram of Growth Methods of Gallium Oxide

Like the standard semiconductor silicon, gallium oxide may be grown from the melt. The high melting point of T = 1940 °C makes great demands on the growth setup and in particular on temperature stability and chemical inertness of the melt carrying crucible material.

First reports on melt growth of Ga_2O_3 stem from *Chase* et al.[79] *Lorenz* et al.,[80] and *Harwig* et al.[81] who applied the quasi crucible free Verneuil process to fabricate crystals of up to 10 mm in diameter and 25 mm in length for fundamental studies of structural, electrical and optical materials properties.

Current studies follow either the crucible free floating zone process (see Section 4.2) or crucible based Czochralski method with its derivative, the edge defined film-fed growth (section 4.3).

4.2 Floating Zone (FZ) Growth of Ga_2O_3

In recent years, the crucible free floating zone (FZ) growth process has been applied by a number of research groups.[82–87] Like in the case of a number of oxide materials, intense light of halogen lamps and a focusing ellipsoidal mirror system is used for heating. As source material a rod of isostatically pressed Ga_2O_3 powder (typical purity: 4 N to 5 N) is applied. The largest Ga_2O_3 crystals exhibit a diameter of 25 mm and a length of 40 mm.[85] To reduce the concentration of oxygen vacancies that form intrinsic donors in Ga_2O_3, an annealing process in an oxygen-rich atmosphere may follow the growth process. To achieve larger crystal diameters of 100 mm or better 150 mm that meet the requirements for the processing of electronic devices, crucible based growth technologies (section 4.3) may be favorable for Ga_2O_3.

4.3 Czochralski (CZ) and Edge-Defined Film-Fed (EFG) Growth of Ga_2O_3

In the case of the crucible based Czochralski (CZ) process[88–90] and its related derivative the edge-defined film-fed

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(EFG) growth technique[91] iridium is applied to carry the Ga_2O_3 melt. To suppress oxygen evaporation from the melt as well as the decomposition of the crucible material, a gas mixture of argon and oxygen or argon and carbon dioxide is applied under ambient pressure. Related to the pronounced (100) and (001) cleavage planes of the monoclinic β-Ga_2O_3 lattice, growth is performed in the crystallographic [010] direction. To reduce thermal stress, cooling down the crystal to room temperature is usually carried out using an after-heater.

Using the Czochralski method[88,90] crystals of up to 100 mm in diameter[78] have been prepared. In the case of the EFG-process[91] flat (100) oriented 150 mm large quasi-wafers have been fabricated[78] that meet basic technological device processing requirements.

4.4 Outlook

The main obstacles to be solved for the growth of Ga_2O_3 single crystals for a broad technical application are related (i) to the control of oxygen partial pressure, and (ii) the presence of the pronounced (100) and (001) cleavage planes.

In the case of the oxygen partial pressure a suppression of oxygen evaporation from the Ga_2O_3 melt is necessary to inhibit a nonstoichiometric composition of it as well as the corrosion of the iridium crucible. Also an evaporation of oxygen from the Ga_2O_3 crystal surface during growth and during cooling down needs to be further suppressed in order reduce unintentional doping through intrinsic oxygen vacancies.

In the author's opinion, melt growth of Ga_2O_3 by the vertical Bridgman (VB) and Vertical Gradient Freeze (VGF) should be considered in the future. Low temperature gradients during growth could lower the probability of cleavage along (100) and (001) planes. In addition, the usage of a liquid encapsulation (to be developed) on top of the melt surface would minimize the oxygen vacancy generation in the crystal and the oxygen corrosion problem of the iridium crucible.

5 Diamond

5.1 Phase Diagram and Growth Methods of Diamond

The phase diagram of the existence range of the carbon crystal structures graphite and diamond as a function of temperature and pressure in Figure 8 exhibits a number of features relevant for selection of the growth process. Although quite stable under ambient conditions and temperatures up to ca. 1000 °C, diamond may be accounted as metastable phase of carbon with graphite as stable structure under ambient pressure. Graphite dissociates at ca. 3900 °C and a pressure of up to ca. 100 MPa directly into gaseous carbon with no intermediate liquid phase. Diamond itself exhibits an equilibrium transition into liquid carbon at ca. 4000 °C and a pressure of ca. 10^4 MPa. With increasing pressure to values above 5×10^3 MPa the melting point of diamond lowers to values below 2000 °C.

Based on the phase diagram in Figure 8 growth of crystalline diamond may be performed under equilibrium-near conditions from a carbon melt or solution at extreme pressures in the 5×10^3 MPa range that touch technological limits. In this context the high pressure high temperature solution growth (HPHT) has been developed.[92–94] Using for example carbon in an iron-nickel alloy as catalyst at 5.5×10^3 MPa and 1300 °C diamond of up to a few millimeters in size have been synthesized.[95] The crystal size is much limited by the dimension of the vessel interior that needs to withstand the extreme pressure of ca. 5×10^3 MPa.

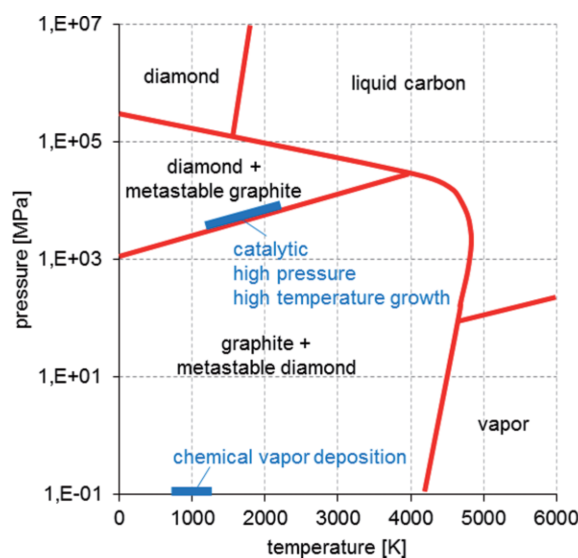

Figure 8. Sketch of the phase diagram of carbon as a function of temperature and pressure.

5.2 Gas Phase Deposition of Diamond

Another approach to grow crystalline diamond is based on off-equilibrium conditions during vapor growth.[92–94,96–99] In particular, chemical vapor deposition (CVD) that makes use of hydrocarbon precursors like methane (CH_4), ethane (C_2H_4), and propane (C_3H_8) is applied.

Stability criteria to perform chemical vapor deposition of diamond are given by the Bachmann triangle C-H-O composition diagram (Figure 9). In particular, the hydrocarbon route

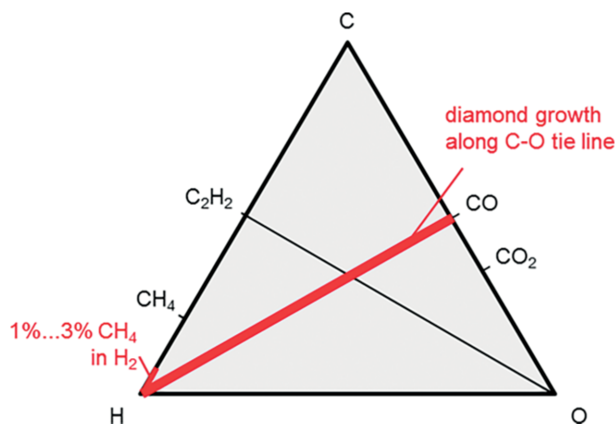

Figure 9. Sketch of the Bachmann triangle C–H–O composition diagram for stable diamond growth conditions. Red lines indicate areas of diamond deposition.

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C-H needs hydrogen rich conditions with at least 97 % of H_2 in the case of a CH_4 precursor diluted in H_2. The high hydrogen content inhibits that formation of graphite by predominantly etching of sp^2-bound carbon vs. sp^3-bound carbon in the diamond case.

Noteworthy is so called the CO tie line within the Bachmann triangle that offers additional technologic freedom in future development of diamond growth processes. In the hydrocarbon route, growth kinetic of diamond mainly depends on (i) the availability of atomic hydrogen (elemental H) and the methyl radical (CH_3), as well as on (ii) the provision of carbonized seeding interface. Technically, the dissociation of hydrogen gas (H_2) into hydrogen radicals (elemental H) and hydrocarbons (CH_4, C_2H_4, C_3H_8) into methyl radicals (CH_3) precursors is performed through a hot filament ($T \approx 2000$ °C) of tungsten (alternative: tantalum), by the provision of microwave heated plasma or by usage of a hot thermal plasma jet gas stream.

As seeds carbonized metal (e.g. Ir, Fe) and silicon surfaces or diamond platelets may be applied that are chemically stable in the harsh environment of the hydrogen and methyl radicals. Recently, *Mühle* et al.[100] demonstrated a diamond single crystal of ca. $7 \times 7 \times 1.5$ mm^3 in size that was grown on a $3 \times 3 \times 1.4$ mm^3 HPHT diamond seed using a 2.45 GHz microwave CVD reactor (substrate temperature of 1000 °C to 1200 °C, pressure ca. 200 mbar) at a growth rate of ca. 18 µm·h^{-1}.

5.3 Doping of Diamond

Like in the case of the group IV semiconductor silicon, the small boron atom may be applied as acceptor dopant. Due to the large hole binding energy of ca. $E_A \approx 400$ meV, the electrical activation at room temperature is rather low. Doping with donors, however, is an unsolved issue in diamond. Phosphorous and nitrogen that are quite successfully used as donors in silicon and silicon carbide, respectively, fail in diamond.

6 Summary

Among the presented wide bandgap semiconductors the hexagonal 4H-SiC already offers a mature bulk crystal growth and device processing technology. Its major application lies in the field of high power electronics where reliability plays a major role. Nevertheless, cubic 3C-SiC, which may benefit from the 300 mm silicon wafer technology could also have a significant contribution in the mid power range. In this application field GaN epitaxially grown on silicon is of particular interest. The GaN offers a higher break down field than 3C-SiC and a better high frequency performance. In addition, GaN epitaxy profits a lot from the LED activities. The Ga_2O_3 is a currently a hardly recognized wide bandgap semiconductor for power electronic application. It targets the mid to high power range. Its future development will much depend on the success in the realization of large crystal boules. Compared to SiC, the lower heat conductivity of Ga_2O_3 is a drawback. Diamond is the wide bandgap semiconductor with the best physical properties in almost every sense with respect to power electronics. Today, its application suffers from the lack of crystalline quality. However, in future high power applications that push all power densities and operation voltages to the upper limit, the semiconductor diamond is the best choice. In the author's opinion, ongoing efforts to eventually provide diamond crystals that could enable electronic device operation in the ultra-high power range should be continuously supported.

Acknowledgements

The author gratefully acknowledges the financial support of the Deutsche Forschungsgemeinschaft, the STAEDTLER-Stiftung, the Bundesministerium für Bildung und Forschung as well as the European Commission under the framework of Horizon 2020 that enabled his studies in the field of electronic materials and in particular on wide bandgap materials.

Keywords: Silicon carbide; Gallium nitride; Gallium oxide; Diamond; Energy applications

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Received: August 1, 2017
Published Online: October 20, 2017

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