materials

MDPI

Article

Use of Bilayer Gate Insulator in GaN-on-Si Vertical Trench MOSFETs: Impact on Performance and Reliability

Kalparupa Mukherjee [1,*], Carlo De Santi [1], Matteo Borga [2], Shuzhen You [2], Karen Geens [2], Benoit Bakeroot [3], Stefaan Decoutere [2], Gaudenzio Meneghesso [1], Enrico Zanoni [1] and Matteo Meneghini [1]

1 Department of Information Engineering, University of Padua, 35131 Padua, Italy; desantic@dei.unipd.it (C.D.S.); gauss@dei.unipd.it (G.M.); zanoni@dei.unipd.it (E.Z.); matteo.meneghini@unipd.it (M.M.)
2 IMEC, Kapeldreef 75, 3001 Leuven, Belgium; matteo.borga@imec.be (M.B.); shuzhen.you@imec.be (S.Y.); karen.geens@imec.be (K.G.); stefaan.decoutere@imec.be (S.D.)
3 CMST imec/UGent, 9052 Ghent, Belgium; benoit.bakeroot@imec.be
* Correspondence: mukherjee@dei.unipd.it

Received: 27 September 2020; Accepted: 21 October 2020; Published: 23 October 2020

Abstract: We propose to use a bilayer insulator (2.5 nm Al_2O_3 + 35 nm SiO2) as an alternative to a conventional uni-layer Al_2O_3 (35 nm), for improving the performance and the reliability of GaN-on-Si semi vertical trench MOSFETs. This analysis has been performed on a test vehicle structure for module development, which has a limited OFF-state performance. We demonstrate that devices with the bilayer dielectric present superior reliability characteristics than those with the uni-layer, including: (i) gate leakage two-orders of magnitude lower; (ii) 11 V higher off-state drain breakdown voltage; and (iii) 18 V higher gate-source breakdown voltage. From Weibull slope extractions, the uni-layer shows an extrinsic failure, while the bilayer presents a wear-out mechanism. Extended reliability tests investigate the degradation process, and hot-spots are identified through electroluminescence microscopy. TCAD simulations, in good agreement with measurements, reflect electric field distribution near breakdown for gate and drain stresses, demonstrating a higher electric field during positive gate stress. Furthermore, DC capability of the bilayer and unilayer insulators are found to be comparable for same bias points. Finally, comparison of trapping processes through double pulsed and V_{th} transient methods confirms that the V_{th} shifts are similar, despite the additional interface present in the bilayer devices.

Keywords: GaN; vertical GaN; trench MOS; gate dielectric; breakdown; trapping; reliability

1. Introduction

Vertical GaN technologies [1–10] are gaining popularity for power conversion applications [8,11], owing to the superior power handling capabilities compared to the lateral configuration [12–14], combined with the inherent material advantages of GaN. Among various vertical architectures, trench MOSFETs on Si substrates [3,4,8,10] have substantial economic advantages, in addition to promising performance metrics. However, development is still in the initial stages, and active research into the MOS framework is ongoing.

The choice and quality of the dielectric is an important factor in determining device stability and reliability. However, the performance and degradation issues related to the gate oxide of vertical GaN MOSFETs still have to be investigated in detail. Moreover, several papers (see for instance [15,16]) propose the use of a single dielectric (typically Al_2O_3) as a gate insulator; alternative solutions, such as

the use of bi-layered dielectrics, still have to be explored: bilayer dielectrics are used in silicon MOSFETs, and typically consist of a thin interface dielectric followed by a thicker insulator.

The aim of this work is to advance the understanding on the leakage, reliability, and trapping related to the gate stack of vertical GaN-on-Si MOSFETs. Specifically, (i) we investigate the degradation processes of the gate insulator subject to electrical stress at high field for devices with uni-layer dielectrics; (ii) we propose to use a bilayer dielectric stack (Al_2O_3 followed by SiO_2) with the aim of improving device stability and reliability; (iii) we demonstrate the net superiority of the bilayer dielectric scheme, compared to the uni-layer. The results described in this paper indicate that bilayer dielectrics are an advantageous alternative to uni-layer ones for the fabrication of vertical GaN MOSFETs, and provide general guidelines for device design.

It was chosen to keep a thin interfacial layer of Al_2O_3 on top of the AlGaN, since this allows for substantially improving the quality of the interface, compared to a SiO_2/GaN interface (see recent reports on the topic, such as, for instance, [17,18]). The SiO_2 layer was introduced in order to improve the breakdown strength of the devices, compared to the case in which Al_2O_3 alone is used. The article is structured as follows: in Section 2, the structural details of the studied semi-vertical devices, and of the simulated structure are described. Section 3 compares DC and breakdown tests, which show a reduction of gate leakage by two orders of magnitude with bilayer devices, while ensuring comparable drain currents in the on-state. Section 4 summarizes the observations and concludes the work. The bi-layer approach is found to enhance breakdown robustness, based on observations from step stress and constant voltage stress experiments. Finally, the comparison of V_{th} shifts under positive gate stress reveals that the use of the bilayer dielectric does not notably deteriorate trapping processes in the devices.

2. Materials and Methods

A semi-vertical device configuration is used as a test vehicle to investigate dielectric processing, in gate trench MOSFETs for vertical GaN devices, as described in the schematic in Figure 1. The devices were fabricated on a 200 mm silicon substrate.

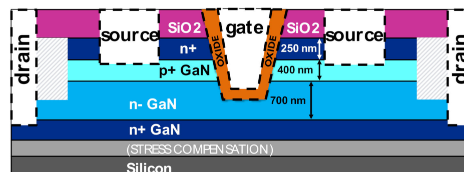

Figure 1. Structural schematic of the studied semi vertical trench MOSFETs.

The bottom of the gate trench is 4 µm in length. The width of each gate finger is 100 µm. The gate trench extends into the n-drift layer. The structure is semi-vertical, meaning that electrons flow from the source, vertically along the gate trench and n-drift region, and then laterally through the buried n+ layer to the drain via, which finally returns the current to the surface through the drain metal. Two wafers with varying gate dielectric from IMEC, Leuven, Belgium are compared: Wafer M with a 35 nm uni-layer aluminum oxide (Al_2O_3) and Wafer B with a bilayer composition: 2.5 nm Al_2O_3 and 35 nm silicon dioxide (SiO_2). In both wafers, the Al_2O_3 layer has been deposited, using atomic layer deposition (ALD) at 300 °C. For the SiO_2 in the bi-layer, a plasma enhanced chemical vapor deposition (PECVD) oxide was used with a deposition temperature of 400 °C.

The Sentaurus tool from Synopsys was used for the TCAD simulations in order to investigate the electric field distribution.

3. Results and Discussion

3.1. DC Parameters and Characterization

Figure 2a,b present typical examples of the gate-source and gate-drain leakage characteristics, respectively, for both wafers, for V_{GS} (with the drain terminal floating) and V_{GD} (with the source terminal floating) sweeps from −3 V to +8 V. Figure 3a,b summarize the leakage distribution at V_{GS} = 8 V and V_{GD} = 8 V, respectively, over several tested devices from each wafer.

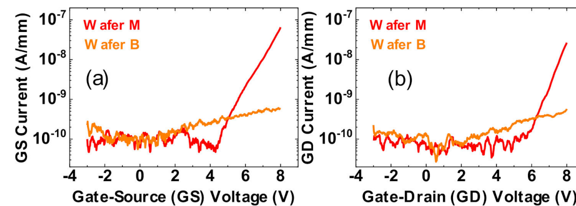

Figure 2. Comparison of diode leakage behavior between Wafer M (uni-layer oxide) and Wafer B (bilayer oxide). (**a**,**b**) are typical characteristics of the gate-source (GS) diode with drain floating (**a**) and the gate-drain (GD) diode with source floating (**b**).

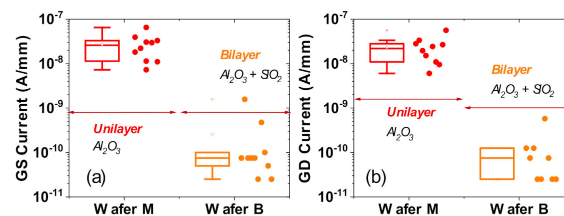

Figure 3. Comparison of diode leakage behavior between Wafer M (uni-layer oxide) and Wafer B (bilayer oxide). (**a**,**b**) show statistical results of the current level at V_{GS} = 8 V (**a**) and V_{GD} = 8 V (**b**).

With Wafer B (bilayer wafer), the gate leakage is clearly lower, by more than two orders of magnitude, compared to Wafer M (uni-layer wafer). This difference may be ascribed to the intrinsic properties of the material, like the critical breakdown field, which is lower in Al_2O_3, compared to SiO_2.

A second factor to take into account is that the use of the bilayer increases the barrier for thermionic electron leakage from the channel to the metal (as shown in Figure 4). By adding SiO_2 to the gate oxide stack, the effective barrier respective to the gate metal is increased.

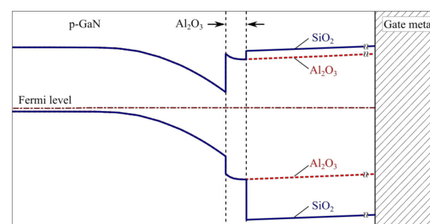

Figure 4. Schematic of the conduction band discontinuity at the Al_2O_3/SiO_2 interface within the bilayer dielectric stack, in comparison to the Al_2O_3 only uni-layer stack.

An additional conduction band discontinuity of 0.4 eV is present at the interface between Al_2O_3 and SiO_2 [19], which contributes to an effectively higher band offset with GaN, relative to the gate. Thus, an associated reduction of the leakage current is expected, which is especially relevant at high positive gate biases.

Figure 5a,b illustrates a typical I_D-V_{GS} characteristic from each wafer at V_{DS} = 10 V in log scale and linear scale, respectively. From measurements on several devices, the threshold voltage (V_{th}) is

extracted at 1µA/mm, and the associated distribution is presented in Figure 5c. The drain current distribution at V_{GS} = 8 V and V_{DS} = 10 V is compiled in Figure 5d for both wafers.

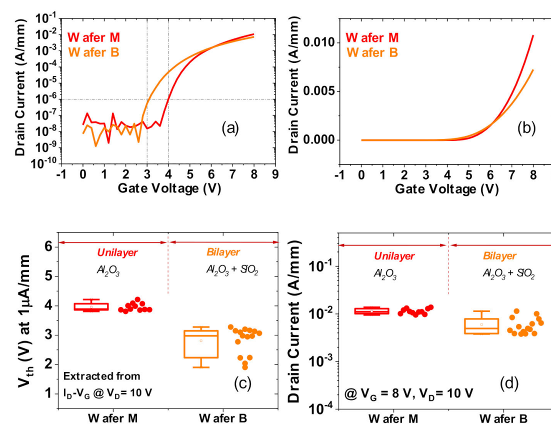

Figure 5. Comparison of transfer characteristics between Wafer M (uni-layer oxide) and Wafer B (bilayer oxide). Typical I_D-V_{GS} results at V_{DS} = 10 V in (**a**) log scale and (**b**) linear scale. (**c**,**d**) box charts with statistics of threshold voltage (V_{th}) (**c**) and I_{DS} current levels at V_{GS} = 8 V and V_{DS} = 10 V (**d**).

The mean threshold voltage is found to be ≈4 V for Wafer M and ≈3 V for Wafer B. Importantly, from the I_{DS} comparison, it can be observed that, for identical bias conditions, the drain current level is comparable between the two cases. Based on the results described within this section, we can conclude that the use of a bilayer passivation substantially improves the leakage performance of the devices, without deteriorating the DC on-state current.

3.2. Drain-Gate Step Stress Experiment

The results described above indicate that a bilayer insulator permits obtaining a substantial reduction in the gate leakage, for comparable DC performance of the transistors. In this section, we evaluate the robustness of devices with uni-layer and bilayer insulators. To this aim, 35 devices from each wafer were subjected to off-state drain step stress tests at V_{GS} = 0 V. The drain stress (V_{DS}) bias was incremented in steps of 3 V until breakdown with 120 s per step.

Figure 6a reports representative examples of the I_{DS} evolution during the step stress test, for each of the wafers. As can be noticed, drain leakage remains stable and low (around 100 nA) until a breakdown is observed. Failure consists of a sudden increase in leakage current, which is indicative of catastrophic breakdown in the insulating layer. I_{GS} evolution (not shown) is found to be similar in nature, indicating that leakage current is dominated by the gate–drain component.

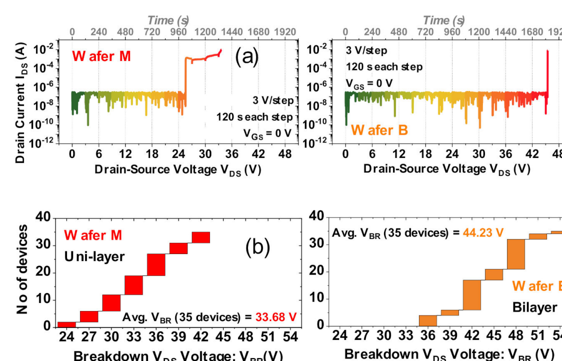

Figure 6. Off-state drain step stress comparison at V_{GS} = 0 V for Wafer M (uni-layer) and Wafer B (bilayer) devices. (**a**) drain-source current (I_{DS}) evolution during stress; (**b**) breakdown drain-source voltage (V_{BR}) distribution for 35 tested devices from each wafer.

Figure 6b reports the cumulative failure distributions for the two wafers; as can be noticed, the mean breakdown voltage for Wafer B (with an average = 44.2 V) is observed to be more than 10 V higher than Wafer M (with an average = 33.7 V).

This represents a relevant reliability advancement for the wafer with bilayer insulator, considering that the thickness of the dielectric is only 2.5 nm thicker than Wafer M. This difference can be ascribed to the different breakdown strengths of the two insulators. Silicon dioxide has a much lower dielectric constant (3.9, [20]) compared to aluminum oxide (9.1, [20]). It is known that the breakdown field decreases with increasing dielectric constant [21,22]. Therefore, silicon dioxide has a higher breakdown field, compared to aluminum oxide.

3.3. Reliability: Electroluminescence Tests

Step stress tests on the drain were also performed in conjunction with electroluminescence imaging to investigate the nature and location of the breakdown spot.

During a step–stress test, typically the samples are destroyed, due to a sudden increase in leakage current. However, catastrophic failure should be prevented, if one wants to use the samples for failure analysis. To this aim, we carried out the step–stress tests by using a current limiting circuit that was added to the microprobes. Once the device reaches breakdown, this circuit instantly decreases the voltage on the devices to avoid thermal runaway at the failure location. This allows for keeping the samples in good status, thus permitting post-stress electroluminescence characterization, to accurately identify the failure spot.

We tested a total of 31 devices. As displayed in Figure 7, stress voltage (V_{DS}) was set at 24 V, and increased by 3 V every 40 s, until failure was reached. A 40 s EL image was simultaneously acquired at each V_{DS}.

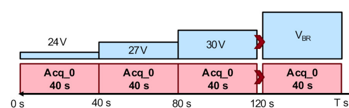

Figure 7. Electroluminescence imaging procedure coupled with step stress.

Once breakdown is achieved, a single post-breakdown stress (with an EL acquisition of 40 s) at the corresponding V_{BR} is performed to verify the location of the detected luminescence spots. The EL spot measured at V_{BR} reflects the region of breakdown in the devices. Figure 8a displays a typical EL device image obtained at V_{DS} = V_{BR}, marking the breakdown location. The rectangular mapping region for each wafer was obtained by considering both gate fingers (see Figure 8b) concurrently. In Figure 8c, the EL spot positions along the gate fingers were collated for each wafer, to acquire the spatial distribution of the breakdown occurrences per 10 µm of the mapped region, as illustrated in Figure 8d.

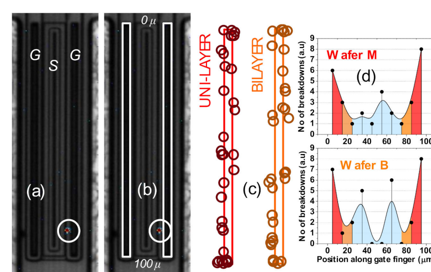

Figure 8. Breakdown spot mapping using V_{DS} step stress with electroluminescence imaging (**a**) example of a device image with an observed breakdown spot; (**b**) outline of the two 100 µm gate fingers which together represent the map area; (**c**) EL spot locations over both gate fingers superimposed onto the mapping region, for each wafer (**d**) number of breakdown occurrences distributed over 10 equal intervals along the width of the gate fingers.

From the distribution in Figure 8d, it can be inferred that the breakdown occurs preferentially near the corners of the gate fingers (top and bottom 10 µm regions within the 100 µm fingers). For both wafers, almost 50% of tested devices (8 + 6 out of 31 for Wafer M and 8 + 7 out of 31 for Wafer B) show breakdown spots at the gate edges. Hence, breakdown location is found to be independent of the dielectric composition.

3.4. Reliability: GS/GD Breakdown and TCAD Simulations

Multiple devices were subjected to forward gate step stress tests at V_{DS} = 1 V to evaluate the maximum voltage applicable to the gate of the devices, and to compare the gate-source breakdown characteristic for the wafers. The gate was biased in 3 V steps of 120 s each, until breakdown was reached.

Electrical measurements were coupled with electroluminescence studies, in order to obtain a detailed description of the degradation process. It is observed here as well that the failure is focused around the gate corners (not shown). The I_{GS} evolution for three representative devices from each wafer is presented in Figure 9a,b, respectively.

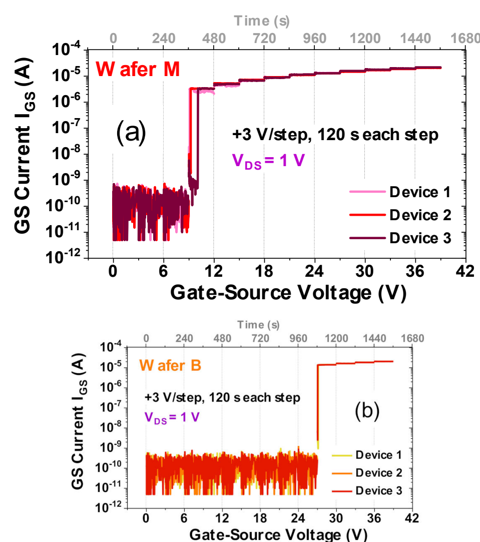

Figure 9. Forward gate-source step stress at V_{DS}= 1 V. (**a**,**b**) present typical stress current (I_{GS}) characteristics for three Wafer M (uni-layer) devices (**a**) and three Wafer B (bilayer) devices (**b**).

It is clear that the bilayer devices are consistently more robust than uni-layer devices, displaying an average gate breakdown voltage of 27 V, which is substantially higher than the gate breakdown around 9 V observed for the Wafer M devices. This represents an important improvement in gate reliability.

The gate-source step stress experiment probes the devices under on-state conditions, compared to the off state drain-source step stress results discussed above. Accordingly, breakdown voltages obtained for V_{GS} stress are correspondingly lower for both wafers. (44 V to 27 V for Wafer B, and 33 V to 9 V for Wafer M). TCAD simulations can be used to visualize the region near the gate under both of these conditions. The representative structure used to simulate the devices is presented in Figure 10.

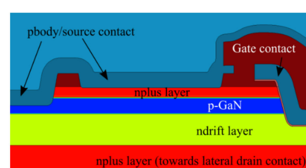

Figure 10. Simulated structure representing the GaN trench MOSFET devices.

Figure 11 displays the equipotential lines around the gate of the bilayer device structure: (a) for a gate-source voltage sweep at V_{GS} = 27 V and V_{DS} = 1 V and (b) for a drain-source voltage sweep under OFF-state conditions at V_{DS} = 44 V and V_{GS} = 0 V.

For a positive V_{DS} sweep under OFF-state, the channel is not formed, and the potential drops on both the oxide and the depleted drift region. From Figure 11b, we can observe the increase of the electric field below the trench within the n-drift layer. The associated depletion within the drift region absorbs part of the applied voltage. Hence, the critical electric field inside the gate dielectric is obtained at higher drain voltages compared to the ON-state.

Indeed, in the ON-state (forward gate bias), the channel is formed along the gate trench sidewalls. As such, as can be seen from Figure 11a, the applied gate voltage falls almost entirely across the oxide and the critical electric field in the gate dielectric is reached at lower gate bias voltages. Hence, the device breakdown voltage under forward gate stress provides a better representation of the critical electric field associated with a chosen dielectric.

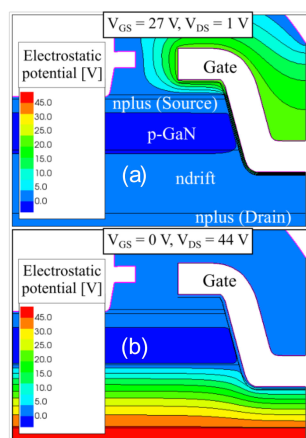

Figure 11. Simulations of breakdown conditions for the bilayer devices: (**a**) in the ON-state with V_{GS} = 27 V and V_{DS} = 1 V and (**b**) in the OFF-state with V_{GS} = 0 V and V_{DS} = 44 V.

Based on the results of the step–stress experiments, for Wafer M (uni-layer dielectric), a basic critical electric field value of 2.6 MV/cm (9 V/35 nm) can be calculated. For the potential of 27 V across the bilayer dielectric stack, the potential at the boundary between SiO_2 and Al_2O_3 can be calculated to be 0.80 V. This corresponds to an estimated electric field value of 7.5 MV/cm (26.2 V/35 nm) across the SiO_2 layer, and 3.2 MV/cm (0.80 V/2.5 nm) across the Al_2O_3 layer, in Wafer B devices.

Taking these values as reference electric fields for which breakdown can be assumed to occur, simulations were performed on vertical trench MOS structures with uni-layer and bi-layer dielectric configurations to assess expected breakdown voltages under ideal conditions.

Figure 12 presents the false color maps of the electric field near the gate trench edges; these simulations were done at the breakdown voltage values estimated for the two wafers by step–stress experiments.

Specifically, we used V_{GS} equal to 9 V at V_{DS} = 1 V for the uni-layer and (b) V_{GS} equal to 27 V at V_{DS} = 1 V for the bilayer device structures. There is electric field crowding near the trench edges for both the cases. In Figure 12a, we can see that the electric field value of 2.6 MV/cm estimated from the experiments approximately corresponds to the V_{GS}= 9 V condition in the uni-layer device. Similarly, from Figure 12b, at V_{GS} = 27 V in the bilayer device, we observe that the calculated field value of 7.5 MV/cm reasonably matches the simulated electric field peak in the SiO_2 layer near the gate trench edge. Thus, the simulated gate breakdown voltages closely approach the experimentally obtained gate voltage limits. This is indicative of a reliable dielectric deposition process used here on GaN.

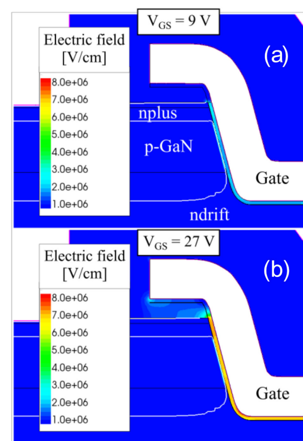

Figure 12. Simulations of the electric field under on-state V_{GS} biasing on Wafer M and Wafer B structures: for the uni-layer device at V_{GS} = 9 V and V_{DS} = 1 V (**a**), for the bilayer device at V_{GS} = 27 V and V_{DS} = 1 V (**b**).

3.5. Reliability: Constant Voltage Stress

Constant voltage stresses were performed on 12 devices for different V_{DS} values per wafer to assess the failure probabilities and derive lifetimes from Weibull analysis. For Wafer M, stress voltages were defined at V_{DS} = 28, 30 and 35 V (around the mean V_{BR} of 33.6 V) and for Wafer B at V_{DS} = 42, 45 and 50 V (around the mean V_{BR} of 44 V).

Based on the constant voltage test results, as displayed for the low voltage biases of 28 V (Wafer M) and 42 V (Wafer B) in Figure 13a, the time to failure (TTF) distribution is summarized in Figure 13b. The Weibull probability percentages are then calculated for both wafers at each voltage and presented in Figure 13c,d for Wafer M and Wafer B, respectively. The plot evaluates the Weibull cumulative probability to determine whether the time to failure under different voltages represents a Weibull distribution [23]. The slope of the Weibull plot (shape factor in Figure 13c,d) reflects the conformity of the obtained fit.

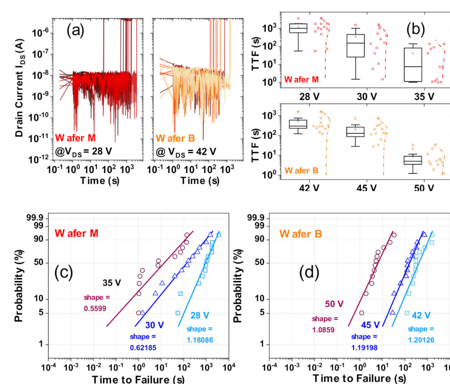

Figure 13. Constant voltage stress tests on Wafer M (uni-layer) and Wafer B (bilayer). (**a**) presents current plots for 12 tested devices at a V_{DS} bias of 28 V for Wafer M and 42 V for Wafer B; (**b**) Time to Failure (TTF) dependence on stress voltage V_{DS} for constant voltage stress tests on both wafers; (**c**,**d**) are probability distributions evaluated for Wafer M (**c**) and Wafer B (**d**) devices.

From Figure 13c,d, the constant voltage TTF data appear to reasonably agree with Weibull distribution fits, for both wafers, except for some outliers with very short failure times. The shape factor for Wafer M is below 1 for V_{DS} = 30 V and 35 V. This indicates that, at these higher voltages, early life or extrinsic device failures dominate.

Only at the lowest V_{DS} = 28 V, the shape factor is 1.18, indicating a shift to intrinsic failures, which could be linked to random events or wearout mechanisms. For the bilayer devices (Wafer B), the shape factors for all V_{DS} cases are all close to or above 1 (constant or increasing failure rate with time), which indicates that the device failures are probably due to wearout mechanisms. This confirms the superior stability of the bilayer dielectric, compared to the uni-layer case.

3.6. Trapping Performance: Threshold Voltage Shifts

In order to evaluate the impact of using a bilayer dielectric on trapping processes, we investigated the dynamic performance of the two wafers under positive gate stresses.

3.6.1. Double Pulsed Measurements

Fast double pulsed measurements [24,25] were performed on both wafers for positive gate quiescent voltages up to an overdrive V_{ov} (=V_{GS}-V_{th}) of 3 V and a quiescent V_{DS} = 0 V. The quiescent periods are interrupted by measurement periods to build an I_{DS}–V_{GS} characteristic specific to a particular $V_{GS,Stress}$ (yielding V_{th}). The t_Q and t_{meas} periods were 100 µs and 1 µs, respectively. The extracted V_{th} shifts at each stress voltage (V_{th} @ $V_{GS,Stress}$ -V_{th} @ 0 V) were averaged from several devices, and then compared in Figure 14a,b, for Wafer M and Wafer B, respectively.

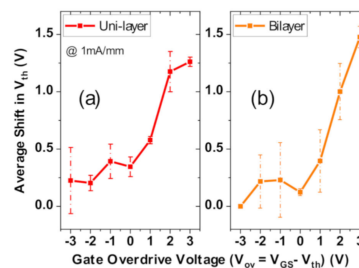

Figure 14. Average V_{th} shift comparison between Wafer M (uni-layer) and Wafer B (bilayer) from double pulsed measurements. (**a**,**b**) are V_{th} shifts for quiescent V_{GS} stress voltages up to gate overdrive = 3V (quiescent V_{DS} = 0 V), for Wafer M with V_{th} ≈ 4V and $V_{GS,Stress}$ = 0 to 7 V (**a**) and for Wafer B with V_{th} ≈ 3 V and $V_{GS,Stress}$ = 0 to 6 V).

It is observable that the V_{th} shifts for similar overdrive voltages are comparable between the wafers. These results indicate that most of the trapping occurs at interface and/or border traps at the GaN/Al_2O_3 interface [25–27], which is common to both dielectric configurations.

We notice that the bilayer devices have slightly larger shifts (≈0.2 V), at the highest overdrive of 3 V. This is reasonable to expect since the bilayer structure introduces an additional interface inside the gate dielectric, which could be a source of additional trapping sites.

3.6.2. V_{th} Transient Measurements

Finally, the V_{th} transient method [25,28,29] was used to accurately extract the V_{th} shifts for each wafer for V_{ov} up to 4 V for a stress time of 100 s. During each stress phase at a given $V_{GS,Stress}$, 22 fast (10 µs) I_{DS}-V_{GS} sweeps (V_{GS} = 0 to 7.5 V at V_{DS} = 12 V) were performed, over a total time duration of 100 s, to measure the gradual shifts in V_{th}. Figure 15a illustrates a typical I_{DS}–V_{GS} characteristic set at $V_{GS,Stress}$ = 6 V for Wafer B during the stress phase, and Figure 15b presents the extracted V_{th} shift (defined for a current intercept of 2 mA/mm). The V_{th} shifts after 100 s of each $V_{GS,Stress}$ were averaged over six devices from each wafer, and compared in Figure 15c for the same overdrive.

The maximum V_{th} shift is around 2 V for both wafers at the highest overdrive of 4 V. Wafer B has moderately higher V_{th} shifts than Wafer M.

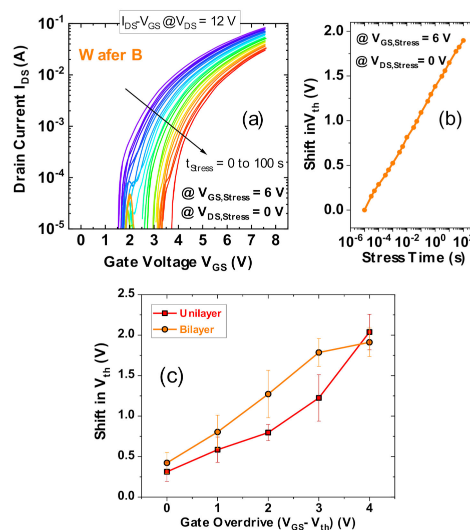

Figure 15. V_{th} shift comparison from V_{th} transient measurements between wafers for V_{GS} stress voltages up to 4 V of overdrive. (**a**) displays a typically obtained set of 22 I_D–V_{GS} curves during 100 s of stress at $V_{GS,Stress}$ = 6 V and $V_{DS,Stress}$ = 0 V on a Wafer B device; the associated V_{th} shift is plotted in (**b**). Averaged V_{th} shifts (at 100 s) for 6 devices each, are plotted in (**c**) for $V_{GS,Stress}$ = 0 to 7 V for Wafer B with $V_{th} \approx 3$ V and $V_{GS,Stress}$ = 0 to 8 V for Wafer M with $V_{th} \approx 4$ V.

4. Conclusions

In summary, we demonstrated that, by using a bilayer insulator, it is possible to improve substantially the performance and the reliability of GaN-based vertical MOSFETs. For almost the same insulator thickness, the devices with bilayer insulator have a gate leakage two orders of magnitude lower, a higher drain breakdown voltage (44.2 V vs. 33.7 V), a higher gate-source breakdown voltage (27 V vs. 9 V). From constant voltage stress tests, the uni-layer shows an extrinsic failure at 30 V (average V_{BR} − 3.7 V), while the bi-layer failures indicate wear out mechanisms even at 50 V (average V_{BR} + 5.8 V), which highlights its better robustness. Electroluminescence studies and simulations were employed to understand the electric field evolution with stress at different stages of the degradation process. In addition to having an improved breakdown robustness for the bilayer dielectric, the trapping effects in terms of V_{th} shifts in both wafers were found to be comparable, which renders the bilayer dielectric configuration highly favorable for use in vertical GaN trench MOS technologies.

Author Contributions: Conceptualization, K.M., C.D.S., M.B., S.Y., K.G., B.B., S.D., G.M., E.Z., M.M.; investigation, K.M., C.D.S., M.B., S.Y., K.G., B.B., S.D., G.M., E.Z., M.M.; data curation, K.M., C.D.S., B.B., S.Y., M.M.; writing—original draft preparation, K.M., C.D.S., M.M., K.G., S.Y., B.B.; writing—review and editing, K.M., C.D.S., M.M., K.G., S.Y., B.B.; supervision, G.M., E.Z., M.M., S.D.; funding acquisition, M.M. All authors have read and agreed to the published version of the manuscript.

Funding: This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No. 826392. The JU receives support from the European Union's Horizon 2020 research and innovation program and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, and Switzerland. This research activity was partly funded by project "Novel vertical GaN-devices for next generation power conversion", NoveGaN (University of Padova), through the STARS CoG Grants call. Part of this work was supported by MIUR (Italian Minister for Education) under the initiative "Departments of Excellence" (Law 232/2016).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Li, W.; Nomoto, K.; Lee, K.; Islam, S.M.; Hu, Z.; Zhu, M.; Gao, X.; Pilla, M.; Jena, D.; Xing, H.G. Development of GaN vertical trench-MOSFET with MBE regrown channel. *IEEE Trans. Electron Devices* **2018**, *65*, 2558–2564. [CrossRef]

2. Hu, J.; Zhang, Y.; Sun, M.; Piedra, D.; Chowdhury, N.; Palacios, T. Materials and processing issues in vertical GaN power electronics. *Mater. Sci. Semicond. Process.* **2018**, *78*, 75–84. [CrossRef]
3. Liu, C.; Khadar, R.A.; Matioli, E. GaN-on-Si quasi-vertical power MOSFETs. *IEEE Electron. Device Lett.* **2017**, *39*, 71–74. [CrossRef]
4. Khadar, R.M.A.; Liu, C.; Soleimanzadeh, R.; Matioli, E. Fully vertical GaN-on-Si power MOSFETs. *IEEE Electron Device Lett.* **2019**, *40*, 443–446. [CrossRef]
5. Otake, H.; Chikamatsu, K.; Yamaguchi, A.; Fujishima, T.; Ohta, H. Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates. *Appl. Phys. Express* **2008**, *1*, 011105. [CrossRef]
6. Gupta, C.; Chan, S.H.; Lund, C.; Agarwal, A.; Koksaldi, O.S.; Liu, J.; Enatsu, Y.; Keller, S.; Mishra, U.K. Comparing electrical performance of GaN trench-gate MOSFETs with a-plane and m-plane sidewall channels. *Appl. Phys. Express* **2016**, *9*, 121001. [CrossRef]
7. Khadar, R.A.; Liu, C.; Zhang, L.; Xiang, P.; Cheng, K.; Matioli, E. 820-V GaN-on-Si quasi-vertical pin diodes with BFOM of 2.0 GW/cm2. *IEEE Electron Device Lett.* **2018**, *39*, 401–404. [CrossRef]
8. Flack, T.J.; Pushpakaran, B.N.; Bayne, S.B. GaN technology for power electronic applications: A review. *J. Electron. Mater.* **2016**, *45*, 2673–2682. [CrossRef]
9. Zhang, Y.; Dadgar, A.; Palacios, T. Gallium nitride vertical power devices on foreign substrates: A review and outlook. *J. Phys. D Appl. Phys.* **2018**, *51*, 273001. [CrossRef]
10. Liu, C.; Khadar, R.A.; Matioli, E. 645 V quasi-vertical GaN power transistors on silicon substrates. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 240–243.
11. Ma, C.T.; Gu, Z.H. Review of GaN HEMT applications in power converters over 500 W. *Electronics* **2019**, *8*, 1401. [CrossRef]
12. De Santi, C.; Meneghini, M.; Meneghesso, G.; Zanoni, E. Review of dynamic effects and reliability of depletion and enhancement GaN HEMTs for power switching applications. *IET Power Electron.* **2017**, *11*, 668–674. [CrossRef]
13. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R.; et al. The 2018 GaN power electronics roadmap. *J. Phys. D Appl. Phys.* **2018**, *51*, 163001. [CrossRef]
14. Ibbetson, J.P.; Fini, P.T.; Ness, K.D.; DenBaars, S.P.; Speck, J.S.; Mishra, U.K. Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors. *Appl. Phys. Lett.* **2000**, *77*, 250–252. [CrossRef]
15. Ruzzarin, M.; Meneghini, M.; Bisi, D.; Sun, M.; Palacios, T.; Meneghesso, G.; Zanoni, E. Instability of Dynamic-R_{ON} and Threshold Voltage in GaN-on-GaN Vertical Field-Effect Transistors. *IEEE Trans. Electron Devices* **2017**, *64*, 3126–3131. [CrossRef]
16. Ruzzarin, M.; Meneghini, M.; De Santi, C.; Meneghesso, G.; Zanoni, E.; Sun, M.; Palacios, T. Degradation of Vertical GaN FETs under Gate and Drain Stress. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 4B.1-1–4B.1-5.
17. Gao, J.; Hao, M.; Li, W.; Xu, Z.; Mandal, S.; Nemanich, R.; Chowdhury, S. Al2O3 Insertion Layer for Improved PEALD SiO2/(Al) GaN Interfaces. *Phys. Status Solidi A* **2018**, *215*, 1700498. [CrossRef]
18. Posthuma, N.E.; You, S.; Stoffels, S.; Liang, H.; Zhao, M.; Decoutere, S. Gate Architecture Design for Enhancement Mode p-GaN Gate HEMTs for 200 and 650V Applications. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 188–191. [CrossRef]
19. Robertson, J.; Falabretti, B. Band offsets of high K gate oxides on III-V semiconductors. *J. Appl. Phys.* **2016**, *100*, 014111. [CrossRef]
20. Robertson, J. High dielectric constant oxides. *Eur. Phys. J. Appl. Phys.* **2004**, *28*, 265–291. [CrossRef]
21. Jain, P.; Rymaszewski, E.J. Embedded thin film capacitors-theoretical limits. *IEEE Trans. Adv. Packag.* **2002**, *25*, 454–458. [CrossRef]
22. Klee, M.; De Esch, M.; Keur, W.; Kumar, B.; van Leuken-Peters, L.; Liu, J.; Mauczok, R.; Neumann, K.; Reimann, K.; Renders, C.; et al. Ferroelectric thin-film capacitors and piezoelectric switches for mobile communication applications. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2009**, *56*, 1505–1512. [CrossRef]
23. Nelson, W. Accelerated life testing-step-stress models and data analyses. *IEEE Trans. Reliab.* **1980**, *29*, 103–108. [CrossRef]

24. Bisi, D.; Stocco, A.; Meneghini, M.; Rampazzo, F.; Cester, A.; Meneghesso, G.; Zanoni, E. High-voltage double-pulsed measurement system for GaN-based power HEMTs. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; pp. CD.11.1–CD.11.4.
25. Mukherjee, K.; Borga, M.; Ruzzarin, M.; De Santi, C.; Stoffels, S.; You, S.; Geens, K.; Liang, H.; Decoutere, S.; Meneghesso, G.; et al. Analysis of threshold voltage instabilities in semi-vertical GaN-on-Si FETs. *Appl. Phys. Express* **2020**, *13*, 024004. [CrossRef]
26. Ren, B.; Sumiya, M.; Liao, M.; Koide, Y.; Liu, X.; Shen, Y.; Sang, L. Interface trap characterization of Al2O3/GaN vertical-type MOS capacitors on GaN substrate with surface treatments. *J. Alloys Compd.* **2018**, *767*, 600–605. [CrossRef]
27. Kaneki, S.; Ohira, J.; Toiya, S.; Yatabe, Z.; Asubar, J.T.; Hashizume, T. Highly-stable and low-state-density Al2O3/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates. *Appl. Phys. Lett.* **2016**, *109*, 162104. [CrossRef]
28. Lagger, P.; Reiner, M.; Pogany, D.; Ostermaier, C. Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in GaN based MIS-HEMTs by stress/recovery experiments. *IEEE Trans. Electron Devices* **2014**, *61*, 1022–1030. [CrossRef]
29. Stockman, A.; Canato, E.; Tajalli, A.; Meneghini, M.; Meneghesso, G.; Zanoni, E.; Moens, P.; Bakeroot, B. On the origin of the leakage current in p-gate AlGaN/GaN HEMTs. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 4B.5-1–4B.5-4.

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).