

Review

Nanosystems, Edge Computing, and the Next Generation Computing Systems

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Received: 30 July 2019; Accepted: 16 September 2019; Published: 19 September 2019



Abstract: It is widely recognized that nanoscience and nanotechnology and their subfields, such as nanophotonics, nanoelectronics, and nanomechanics, have had a tremendous impact on recent advances in sensing, imaging, and communication, with notable developments, including novel transistors and processor architectures. For example, in addition to being supremely fast, optical and photonic components and devices are capable of operating across multiple orders of magnitude length, power, and spectral scales, encompassing the range from macroscopic device sizes and kW energies to atomic domains and single-photon energies. The extreme versatility of the associated electromagnetic phenomena and applications, both classical and quantum, are therefore highly appealing to the rapidly evolving computing and communication realms, where innovations in both hardware and software are necessary to meet the growing speed and memory requirements. Development of all-optical components, photonic chips, interconnects, and processors will bring the speed of light, photon coherence properties, field confinement and enhancement, information-carrying capacity, and the broad spectrum of light into the high-performance computing, the internet of things, and industries related to cloud, fog, and recently edge computing. Conversely, owing to their extraordinary properties, 0D, 1D, and 2D materials are being explored as a physical basis for the next generation of logic components and processors. Carbon nanotubes, for example, have been recently used to create a new processor beyond proof of principle. These developments, in conjunction with neuromorphic and quantum computing, are envisioned to maintain the growth of computing power beyond the projected plateau for silicon technology. We survey the qualitative figures of merit of technologies of current interest for the next generation computing with an emphasis on edge computing.

Keywords: edge computing; the internet-of-things; carbon nanotubes; processors; nanoscience; quantum computing; neuromorphic computing; plasmonics; photonics; information technology

1. Introduction

Capturing and isolating single atoms or molecules and controlling their quantum states to achieve the desired function is undoubtedly a fantastic milestone for toolmaking and information processing, the two pillars of human endeavors. Stimulated by successful demonstrations, such as trapping a single atom or imaging single atomic sites and bonds within a molecule, there have been visions to reach beyond nanotechnology for continuing at thousand times smaller into the pico-technology [1], and at a million times smaller into the femto-technology [2], the realm of neutrons, protons, electrons, and other nuclear particles. Amazingly, pico- and femto-technologies are already being contemplated for addressing technology bottlenecks, such as a better electronic on-off switching speed to improve communication bandwidths beyond ~50 GHz [3]. In the earlier stages of nanotechnology, in “Technical boundless optimism”, D. Jones, reviewing “Nano! Remaking the World Atom by Atom”, raised certain

skepticism with respect to the promises and potentials of nanotechnology [4]. However, demonstrations, such as resolving the atoms that make up the benzene rings within a molecule (pentacene) adsorbed on a copper or a sodium chloride surface [5], uphold the noted optimism. Resolving the atomic structure of graphite, monitoring the formation of fullerene C₆₀ molecules [6], and discerning the various carbon-carbon bonds within the molecules [7] are other examples of boundless success. In “Bonding more atoms together for a single molecule computer”, C. Joachim discussed how the future of computing would depart from solid-state integrated electronics and enter the realm of molecular transistors [8]. Such claims are already being supported by works on single molecules, for example, controlling cis-trans transition in Azobenzene molecule, leading to the molecules being “switched” with spatial selectivity, has been demonstrated [9]. Taming individual atoms towards quantum computing, atom-by-atom assemblers to arrange several trapped neutral atoms in one-dimension [10], in arbitrary two-dimensional patterns [11], and in three-dimensional arrays [12] with controllable single atom capability, have been demonstrated. To scale up the “fabrication” of such atomic and molecular switches, novel concepts are being reported, including the demonstration of monolayer surface patterning at 3.5 nm on a gold surface via self-assembly, offering a potential path to large-area patterning [13].

Assessing the joint impact of nanosystems that function as sensors, actuators, processors, memory, and communication links is nontrivial. For example, the importance of electronic computers in investigations of molecular quantum mechanics was recognized as early as 1956 [14]. However, the notion of molecules themselves being used as computers, or quantum effects being employed to compute and communicate, have only emerged recently. Astonishingly, DNA computing [15], molecular machines [16], biological microprocessors [17], bio-electronic computers [18], etc. have been already reported, albeit largely exploratory.

Nevertheless, aided by nanosystems, information is being created at rapidly increasing rates. Reciprocally, the explosive growth of data [19] and its profitable global market [20] is rapidly advancing the exploration and discovery of new nanosystems that can statically and dynamically accommodate information [21]. The generation and fate of information and its fascinating dynamic relationship with information technological devices warrant scrutiny [22–27]. Morphing into a countless number of sensors [28–30], data collectors are generating mindboggling amounts of data [31], soon to reach $\sim 10^{21}$ bytes (or zettabytes, ZB) [32]. A 2012 industrial study reported an estimated 1 ZB of data generated worldwide with a predicted 40 ZB by the year 2020 [33]. In year 2011, Hilbert and López, estimating the world’s technological capacity to store, communicate, and compute information, concluded that in the year 2007, the world had stored ~ 0.29 ZB (compressed bytes), communicated ~ 2 ZB, and carried out 6.4 exaflops ($= 6.4 \times 10^{18}$ flops or floating-point operations/s) [19]. For comparison, Hilbert and López noted that the exaflop rate roughly equals the maximum number of nerve impulses/s executed by one human brain, and the ZB stored data is approaching the roughly 100 ZB stored in the DNA of a human adult [19].

With computing operation rates at the exaflop in the horizon [34], the high-performance computing (HPC) has to possess the capability to handle exabyte ($\sim 10^{18}$ bytes) massive quantities of data in addition to improved flops. The processing, communication, and storage of the large volumes of data by transistor circuits, interconnects, and networks, invented to make use of the digitally represented information, are pervasive. However, these operations are growing increasingly challenging due to data traffic, memory, and computing capacities. To combat the challenges associated with the need to transfer and communicate large amounts of data generated in one location to an HPC data center in a different location, the concept of edge computing (EC) [35] is being intensively investigated [36–39].

The intent of this article was a survey of the general state of the EC and the pertinent nanoscience subfields, including nanophotonics [40–45] and nanomaterial-based components [46,47]. Noting the cross-disciplinary nature of the solutions needed to overcome existing challenges in EC, we discussed how the relevant research areas and technologies could be mutually beneficial towards serving the needs of the internet of things (IoT) and HPC in the exascale regime. A growing number of

exploratory work of potential for the next generation computing is being reported, e.g., creating and controlling Majorana quasiparticles for use in quantum computing [48], or use of metamaterials in optical computing of integral equations [49]. However, while several exciting venues have opened up towards achieving stable information carriers for quantum computing or biologically inspired massive processing, we here emphasize developments that have been recognized to be closer to scalable implementation. Skyrmions, for example, are spatially highly localized (~nm) excitations or quasiparticles in a magnetic material. They exhibit a level of stability, mobility, and localization that render them highly suitable for information encoding. These magnetic spin configurations are protected by the specific topology of the underlying material domain (e.g., a ferromagnet-heavy metal bilayer [50]). Thus, they can be transported and manipulated to convey information, leading to the notion of Skyrmionics, which has been proposed for stochastic or probabilistic computing [51]. However, probabilistic computing (compared to binary-encoded computation) is itself under active exploration to potentially provide an alternative computing platform for embedded systems at lower area and power, and better error resilience, and high computational density, all of which are ideal attributes for constrained environments, such as EC devices (sensor nodes and mobile devices) [51–53]. Skyrmionics, however, is not considered sufficiently developed to compete with existing silicon electronics. Figure 1 displays some elementary statistics related to EC, emphasizing the recent rapid growth and the diversity of EC research profile. We noted that the key discussion of the article, that is, the use of nanotechnology in the development of EC, pertains more generally to the next generation computing systems rather than specifically to EC.

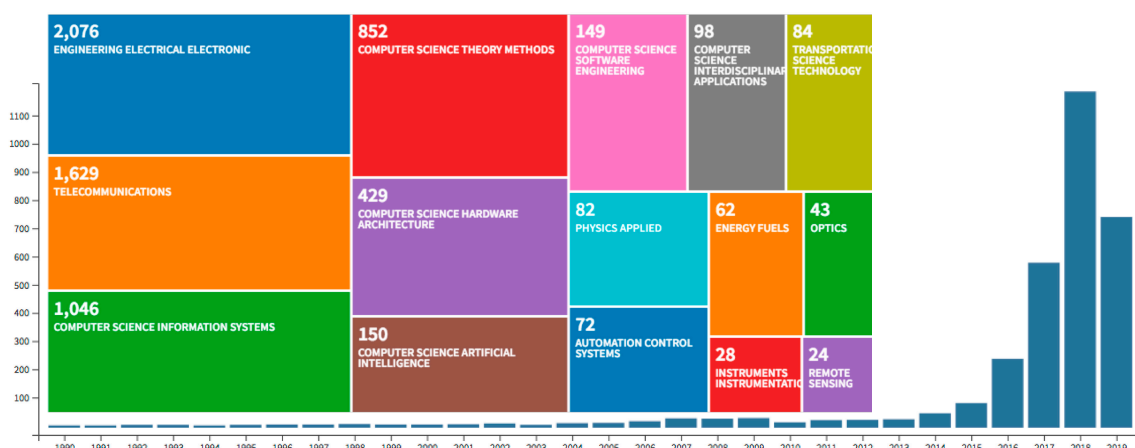


Figure 1. Article statistics showing the histogram of edge computing over publication years, a compilation from [54]. Inset: distribution by discipline [54]. Notable are the intensified research, the multidisciplinary character of the field, and the largest contributing disciplines. The number of other contributing disciplines (not shown) is also increasing rapidly.

2. Edge Computing

Edge computing may be regarded as a product of the evolution of electronics and communication. In “How we created edge computing” [35], M. Satyanarayanan discussed how the realization of the limitations of cloud-based processing led to the proposal of the concept of EC via the introduction of cloudlets [55–57]. While sharing similarities, clear distinctions exist between cloud, cloudlet, fog, and edge [37–39]. Satyanarayanan et al. subsequently showed that reductions of 51% and 42% in latency and power use, respectively, could be achieved in a mobile device when using cloudlets (in this case, a virtual machine on Dell Optiplex 9010) instead of the cloud (Amazon EC2). In “Working on the edge”, further definition of EC was provided by V. Bahl, who also discussed the future of EC, and how it would help the cloudification of the telecom network and become an integral component of it. Interestingly, Bahl further characterized the EC as a “marriage” between the telecom and the IT

industries [58]. While the definition of EC may be subject to slight variation and remains largely broad, for the sake of our presentation, we showed the common ingredients in Figure 2.

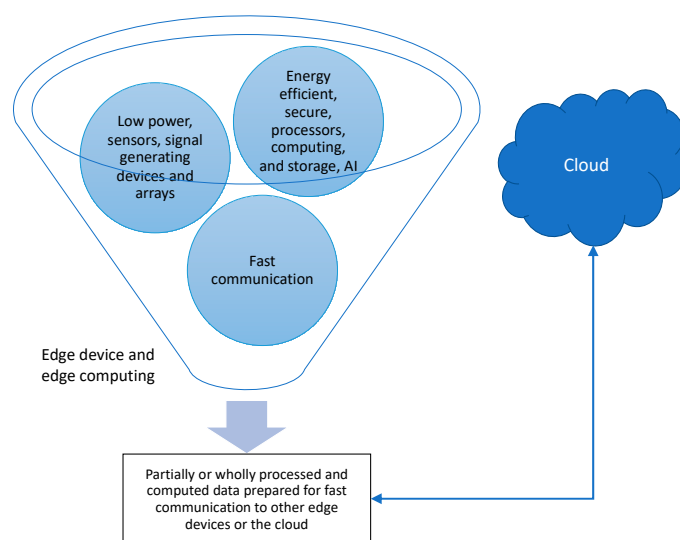


Figure 2. Some basic elements of a device in the edge computing paradigm. The edge device does not necessarily require a connection with a centralized cloud. Many challenges lie ahead regarding energy efficiency, data quality and reliability, data and device security, computing performance level, etc., stimulating exploration for novel nanosystems and processor architectures, rapid communication, and related components.

Examining the rapidly growing number of investigations reported (see Figure 1), the following recurring definition takes the center stage: EC is an emerging data processing paradigm toward countering the current and projected bottlenecks of cloud-based computing. Thus, EC strives to complement the cloud. An EC device processes data on local computing and communication infrastructure and only, if necessary, prepares data and establishes a communication link to a data center or other EC devices. Therefore, EC is envisioned to overcome both latency and memory bottlenecks of the current centralized cloud-based paradigm. However, despite recent related surveys [37–39], exactly how an EC device should be defined has not been rigidly formulated due to the infancy of the EC field and the high degree of diversity of IoT. Nevertheless, we may recognize that to constitute an EC device, innovations in both hardware and software are necessary to meet the growing speed and memory requirements.

EC devices take on the task of carrying out preliminary data processing instead of transmitting raw data to data centers for processing. Aiding the cloud by greatly reducing the upload bandwidth and computation complexity, the EC nodes are envisioned to perform tasks, such as real-time signal and image processing, combinatorial optimization, agent-based modeling, big data analysis, etc. Such tasks are performed to provide secured services, effective control, and seamless decision-making while achieving energy efficiency. Therefore, HPC is essential to EC networks [59]. In recognition of the importance of the EC field, in a recent, editorial “Take it to the edge” [60], it was named the 2019 technology of the year.

A central objective of cloud, fog, mist [61], and recently EC, has been to achieve enhanced performance locally using a non-centralized distribution of computer memory and computing power (see). The advantage of offloading computational tasks to fog or cloud servers is a time reduction for task processing. Thus, physically, servers are deployed at the near edge or the extreme edge of the network (closer proximity to the data sources) instead of the data centers [62]. Specifically, EC is addressing the challenges facing the computing of data for which speed and scale are not only ideal but necessary. Despite the power of the cloud computing and storage solutions (e.g., platforms, such as Amazon elastic compute cloud [63] and Google cloud platform [64]), the increasing number, type,

and spatial distribution of devices, generating extremely large amounts and types of data, require continuous innovation. Therefore, the infrastructure is evolving from its core, i.e., the data centers to its edges. The diversity in the IoT applications implies that data processing may require different levels of intelligence, efficiency, and security. As the technologies could generate predictions about personal behaviors and private lives, measures must be considered to guard against the associated pervasive analytics. An important issue of EC is dealing with data protection, as discussed in “Data protection in the age of big data” [65]. Recently, in “Multi-tier computing networks for intelligent IoT”, as depicted in Figure 3, Y. Yang defined the roles of cloud, fog, and edge computing technologies; delineated their hierarchies; and described how integration among them might be necessary for optimum IoT services [66].

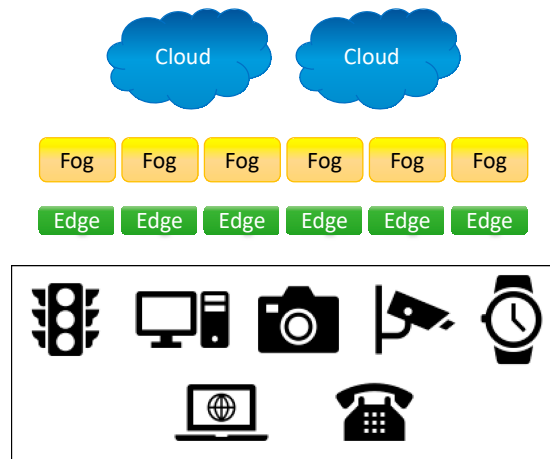


Figure 3. Multi-tier computing networks. The integration of various technologies to achieve intelligent applications and services.

Increasingly advanced sensors with sophisticated data acquisition (software and hardware) are being employed globally. In sensing, a simple use case is that of a single sensor or a network of complex integrated sensors [67] reporting a single or arrays of parameters, e.g., extracted from a terrestrial or an extraterrestrial environment. As an example, consider a sensor for the detection of environmental methane, mercury, fungi, or bacteria. As depicted in Figure 4, a raw signal is produced by the sensor, which within some calibration is representative of or proportional to the presence of the sought chemical or biological species. To create useful information and decision-making, the raw signal is either (I) communicated directly to the cloud via a network for processing and storage, or (II) is first somewhat processed locally and then communicated to the cloud.

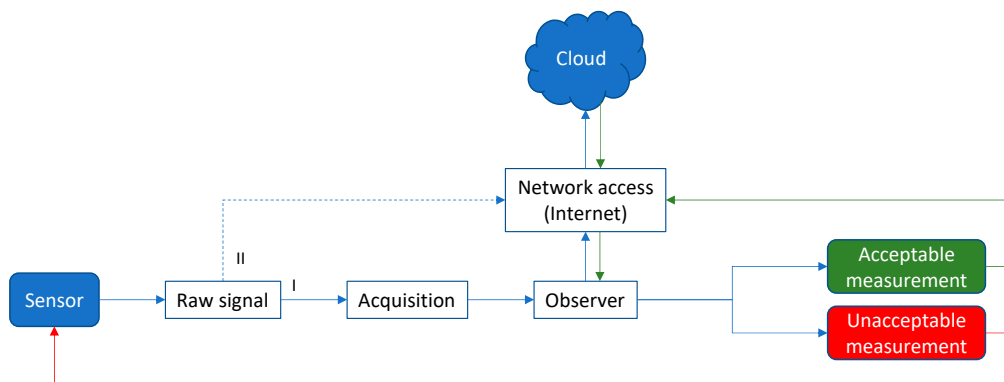


Figure 4. Example of a current paradigm based on cloud computing. Sensors generate raw signals, which are submitted to the cloud directly (route II) or are acquired and observed and then either communicated to the cloud or are evaluated and submitted to the cloud.

Within the IoT, the number of sensors is exploding, and thus feeding or uploading such raw or insufficiently processed varying sized signals is readily seen to lead to bandwidth, latency, and storage problems [68]. For example, smart cities [69], homes, and cars will generate a heretofore unimaginable amount of data and communication loads. EC is envisioned to alleviate such predicted/expected problems. By incorporating a local high-performance processor with built-in artificial intelligence (AI), local decision-making can be carried out and only if necessary, communicated with the cloud. This is depicted in Figure 5, where the raw data is locally processed in an embedded processor with sufficiently provided AI (e.g., Fuzzy logic, Bayesian network) to generate high-level information and confident decisions. The output information, instead of the raw data, may then be communicated to the cloud for further processing (HPC, storage, etc.).

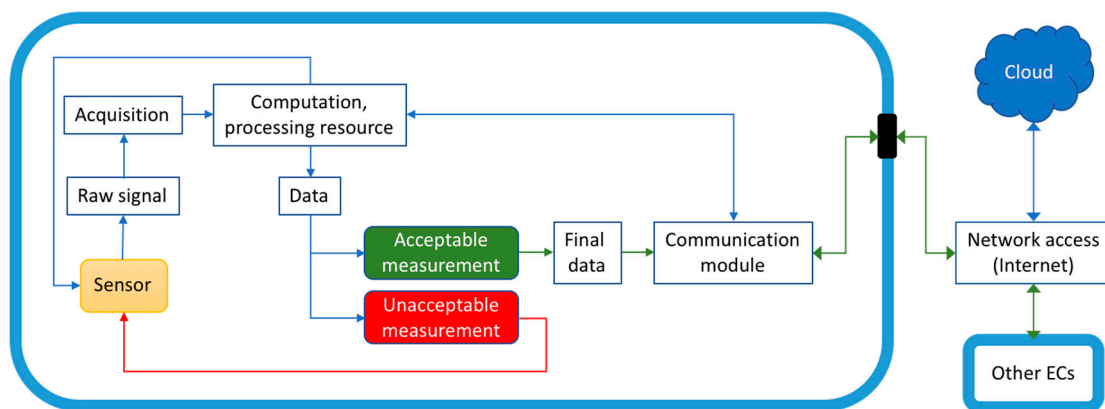


Figure 5. A simplified edge computing approach. A sensor generates raw data, which is locally processed and evaluated. If the outcome meets certain criteria, the data is then communicated to the cloud for further processing/computing and storage.

Distributed sensing, such as used in the oil and gas industry, is expected to be a major beneficiary of EC. For instance, spatially distributed, fiber optic sensors, capitalizing on Brillouin and Raman scattering [70], interact and detect pressure, vibrations, gas species (leaks and contamination), temperature, and other harsh-environment parameters for fossil energy research [71]. Due to its distributed nature, EC encompasses many of the same aspects of signals, processing, computing, and data storage. As a result, within the IoT, including IIoT (industrial IoT [72]) and IoMT (internet of medical things [73,74]), the EC devices are extremely diverse, and the volume of data they are generating and processing is rapidly increasing. Data formats include time and frequency space signals, complex images, sound and voice, and a plethora of protected health [74–76], personal, and sensitive data. Due to the variety of EC devices, data types, and algorithms [77], many AI-based or smart offloading and transmission strategies are being proposed, such as employing machine and deep learning methods [75,78], or mimicking human brain networks [79]. Similarly, knowledge-sharing strategies to take advantage of self-taught knowledge between EC devices, such as pertaining to home IoT, have been considered [80]. Undoubtedly, EC-specialized or related optimization problems formulation and solution will be valuable [72,81–83], as discussed in the case of optimization consideration for platooning for automatic driving [84], evolutionary game theoretical proposals for mobile devices and security [85,86], better estimation of interference in EC devices [87], cost-effective placement of EC servers [88], computational power allocation for blockchains [89], and incorporation of computer vision [90].

While security strategies are being developed [61,91,92], the emerging era of EC offers tremendous opportunities for research and development in nanosystems, such as optical sensors, optical communication, and photonic processors [40–42,44,93,94], all of which are to be seamlessly integrated in one or more part of the secure network, from the edge to the core.

The increased computational loads on end EC-based devices, in conjunction with IoT operating system, is to consider balanced process management for the interplay between the processing and communication tasks [95] or resource and energy consumption [96]. In an empirical study using IoT sensor devices, tests were carried out with different levels of computational load and various priority schemes to show that an increased load results in cross-effects between the processing and communication tasks, significantly affecting their performance [95].

The decentralized decision-making of the EC paradigm toward generating accurate data must be energy efficient. For example, the continuous readings to provide high-resolution location can be energy inefficient in mobile devices prompting proposals to develop on-device cognitive-inspired control for power-aware human mobility analysis in IoT devices [97]. In addition to energy efficiency, the emerging EC, aiming to provide faster IoT operation and mobile devices, seeks to conserve and optimize memory, cache, server placement, size, weight, etc., calling for new studies and proposals. Recently, to realize a potentially scalable and intelligent caching scheme that aims to reduce cache redundancy, a progressive popularity-aware caching scheme was proposed [98]. To avoid wasting cache space when the content is not popular enough, the proposed method first caches initial “chunks” of the content at the edge node and then progressively continues caching subsequent chunks at upstream according to the content popularity and each content node position [98]. Also, the cost-effective placement of edge servers has been proposed for metropolitan area network [88].

The universality of EC applications and the accumulative impact they will impart can be readily appreciated from the long list of applications that are rapidly growing into various hierarchies of service. For example, for more reliable service, solar cells/panels and related devices need to become smart with AI for IoT in an EC domain. Spectral variation, combined with an array of environmental sensors to monitor, pressure, temperature, humidity, wind speed, cloud movements, etc., can be utilized to optimize the performance of solar cells, leading to potentially significant economic benefits. Similarly, traffic lights augmented with hyperspectral imaging and chem-bio sensors can be made locally smart when combined with weather sensors and the unique local population and infrastructure signatures. More concrete EC applications include scalable framework for early fire detection [99], disaster management services [100], accelerometers for structural health monitoring [101], micro-seismic monitoring platform for hydraulic fracture [102], a framework for searchable personal health records [75,76,103], smart health monitoring [76,104] and healthcare framework [105], improved multimedia traffic [106], a field-programmable gate array (FPGA)-based system for cyber-physical systems [107] and for space applications [108], biomedical wearables for IoMT [73,76,109], air pollution monitoring systems [110], precision agriculture [111,112], diabetes [74] and ECG [109] devices, and marine sensor networks [113].

Acute needs of edge devices are readily identified within the customs and border protection (CBP), where agents controlling illicit drugs and contraband can immediately make decisions instead of communicating with other data centers. With the opioid crisis, the number of sensors will inevitably increase, and EC devices with sufficient computing power and rapid communication rate can provide critical decision-making.

Since the EC devices, such as IoT sensor nodes, will be ubiquitous, embedded computing paradigms for EC devices will have to use energy-efficient microprocessors to process the data. Furthermore, supplying real-time on-demand energy for EC devices will have to be investigated, in particular, since the energy consumption rate changes dynamically at different nodes prompting new charging scheduling schemes [114].

For chemical and biological sensors, real-time data acquisition, rapid processing, and computing are necessary. If the sensor output can be processed locally, instead of being sent to a different location, better mitigation and remediation can be achieved. A closely related EC-use case is the need for intelligent surveillance cameras. With the tremendous need for chem-bio standoff detection, the ability to collect molecular spectral data in addition to visual information would revolutionize the surveillance technologies. Aided with AI, EC surveillance cameras will be capable of processing the

local streaming and only communicate specific detection results rather than continuous submission of the data. Upon reception, the cloud could then send the EC device new instructions, including programming to different functionalities.

Increasingly more complex services are expected to be provided by the continuously improving energy efficiency of system-on-chip (SoC), furnishing sensors and devices (edge, mist, fog, and IoT end devices) with significant computing power. This allows a self-contained module in which edge sensors and actuators generate data that can be processed on-site. In addition to software, SoCs, containing components, such as processors, graphics processing unit GPU), network-on-chip (NoC) [115], and memory and data storage, essentially function as a server. Attractive/desired attributes of SoCs include their SWaP (size, weight, and power).

Given the staggering number of future EC devices, it may be prudent to treat certain dynamic aspects of the EC within the realm of coupled oscillator systems and self-similar geometries, as graphically depicted in Figure 6. One may then ask the question of specific distributions of EC devices corresponding to holistic and emergent information phenomena.

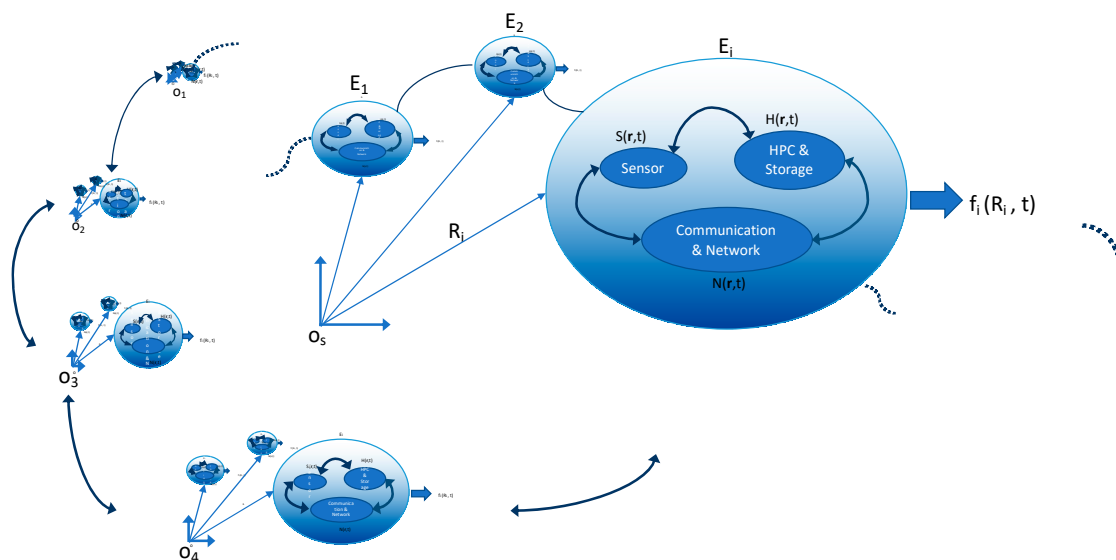


Figure 6. Envisioning a potential variation of the interconnectivity of edge sensors. The nested growth of edge devices may form a system of a coupled dynamical system with fractal self-similarity. The sensor output S can be processed to H and communicated as N with a final output of f for node i located at R_i relative to data center O_5 .

Although there is an increasing number of EC-related optimization work being reported, obtaining quantitative data on the figure of merit of EC is less prevalent in the current state of affairs. Such quantitative data would provide energy consumption merits or other advantages of EC. For example, in a fog versus cloud computing experiment, in which 25% of the applications needed real-time services, around 40% reduction in energy expenditure was reported for the fog [37]. Similar reports are emerging, where also EC advantages are being specifically compared to cloud computing. For example, an edge micro-seismic monitoring system was shown to perform at higher efficiency with less transmitted data when compared to a method lacking edge capability [102]. EC-specific quantitative metrics is currently highly needed. Unlike cloud computing simulation frameworks (including the cloud-based EdgeCloudSim simulator [116]), simulators that could be specifically used for modeling the design and behavior of an EC device are not quite available yet [36].

Given the very broad scope of computing, our review encompassed a brief account on the emerging nanomaterials and nanosystems of potential use in computing. Discussions pertaining to the many types of processors: central processing unit (CPU), GPU, FPGA, etc., architectures (multi-core,

heterogeneous core processors, neuromorphic, etc.), and related hardware and software are presented marginally [117–119].

3. Edge Computing Processor Architectures

Although currently, supercomputers, such as Summit and Sierra (ranking No. 1 and No. 2, respectively on the Top500 list) are not practical for EC, it is envisioned that smart supercomputers will eventually enter the EC domain, unleashing new capabilities. Summit [120], for example, a US Dep. of Energy machine at Oak Ridge National Laboratory, links more than 27,000 GPUs and 9000 CPUs to provide 200 petaflops ($=2 \times 10^{17}$ operations/s) HPC at a power consumption of 13 MW, which is not practical yet for EC devices.

The projection that the number of IoT devices will continue to grow rapidly ($\sim 50 \times 10^9$ by 2020 [37]) places increasing demand on-chip performance. The power efficiency of EC devices is thus of paramount importance despite the development of better energy storage and power transport technologies. Designers, developers, and manufacturers compete to achieve smaller, lighter, lower cost, but faster, higher performance, and more energy-efficient processors for EC applications. Thus, as the EC-use cases are being more systematically characterized, the design of EC-optimized processors is expected to intensify.

Processor design begins by considering a specific instruction set architecture (ISA), which provides the needed information to write machine language programs and implement different processors. The ISAs, having varying degrees of complexity [121], can lead to processors that may be more suitable for EC and edge-native applications. For example, an ISA that retains specialized instructions, including those that may be used less frequently in practical programs, is the complex instruction set computer (CISC), which was the basis for Intel's 80×86 chip. CISC, however, has not been seen as competitive for EC, which focuses more on specific performance and functionality criteria. A lighter version of ISA, the reduced instruction set computer (RISC), prioritizing the frequently used instructions while implementing the less frequently used instructions as subroutines, offers a more efficient approach for EC and edge-assisted applications. The use of RISC processors has come to dominate many embedded applications markets making up 99% of microprocessor volume in 2017 [122]. A comparison of chips based on various architectures is shown in Figure 7, where the RISC chips, such as advanced RISC machine (ARM) and MIPS (microprocessor without interlocked pipelined stages), are seen to dominate the market in comparison with Intel's 80×86 , which in the year 2011 reached its peak at 0.365 billion [122]. Since RISC processors carry out fewer computer instructions, they operate faster, which is of specific importance in many EC devices where the real-time or simultaneous response is desired. By excluding instructions that are not needed, RISC processors, employing a reduced number of transistors, use a fraction of the power required by CISC processors. RISC processors can also be more suitable for miniaturized EC devices since the size of the semiconducting material (die size) needed for the integrated circuit is proportional to the transistor count, which leads to smaller processors.

As discussed by D. Patterson in "Reduced Instruction Set Computers Then and Now" [122], RISC grew out of an attempt to execute more instructions in a single short cycle. With the rapidly advancing IoT applications, placing increasing demands on EC, new and innovative ISAs, such as the open-source RISC five (RISC-V) [121,123], is paving the way for new architectures, allowing hardware designers to implement powerful processor for both EC and the cloud [124]. With frozen base instructions (while supporting custom instructions for designing specialty functions), software written for RISC-V will indefinitely run on other similar RISC-V cores.

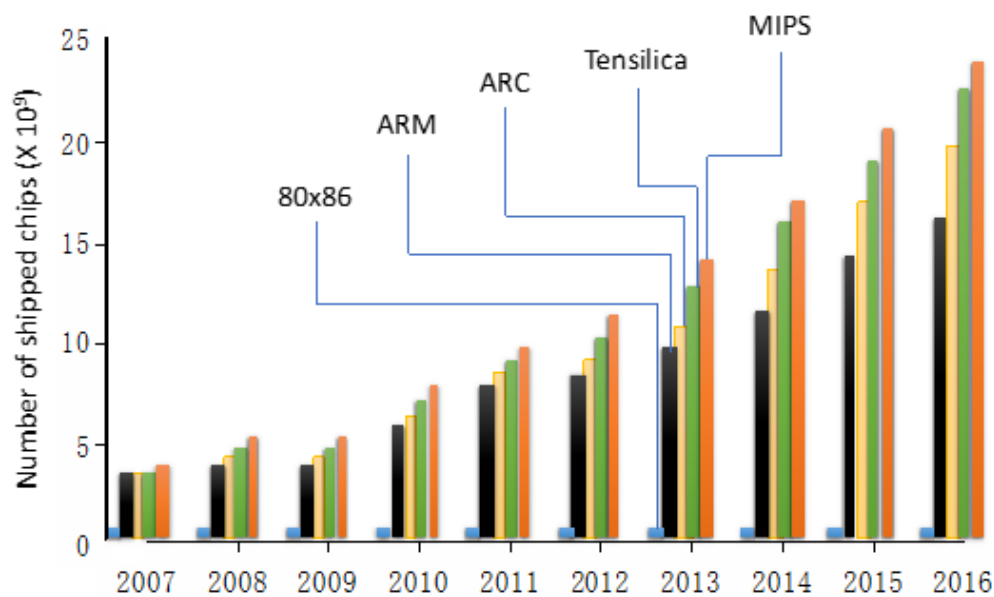


Figure 7. Comparison of the number of RISC chips (ARM, ARC, Tensilica, or MIPS ISAs) versus CISC architecture (Intel's 80×86). RISC, reduced instruction set computer; CISC, complex instruction set computer; ISA, instruction set architecture; ARM, advanced RISC machine.

Examples of new commercial processors for EC applications include chips from the Advanced RISC Machine (ARM) [125]. In addition to products such as the Cortex families [126], the recently announced Neoverse solutions are explicitly advertised for EC-use cases [127]. The main characteristics that advertise these new chips within the EC domain include low latency, low power consumption, and smaller size. Others offering or competing to supply EC hardware, capabilities, and services include NVIDIA EGX platform [128], APC's Edge Computing Solutions [129], Open Edge Computing Initiative [130], and others.

Classically, achieving optimum control is recognized as the hardest part of computer design [121]. However, the impact of novel ISAs stretches beyond classical computing. Interestingly, similar RISC-inspired considerations have also been proposed in quantum computing, to offset any disadvantages that are imposed by the inaccessibility to specific quantum bits (qubits) (e.g., individual trapped ion [131] or individual neutral atom sites [132] in optical lattices) towards implementing control [133]. It may, therefore, be envisioned that similar reduced ISA advantages may prove useful to consider in exploratory nanoscience work on novel processor designs.

4. Nanosystems and Nanoscience: From Edge Sensing to Edge Computing

Computing has successfully capitalized on the electronic properties of silicon and silicon-based electronics. The success builds primarily upon the scalability of silicon transistors, such as a field-effect transistor (FET), which is the basic component of present computer circuitry. To surpass sub-20 nm nodes, that is, the semiconductor manufacturing process that generates transistors with a size smaller than 20 nm, the conventional scaling has reached major limitations. Currently, silicon FETs are fabricated at the 14-nm node (and at sub-14-nm node using FinFET technology) and have an overall lateral footprint of ~ 90 – 100 nm. Innovative approaches and extreme ultraviolet lithography to print the features are being explored towards 5 nm node design. Thus, nanoscale phenomena are expected to be manifested more strongly in the increasingly nanosized domains. In nanosystems, because the electronic and optical response of bulk materials are altered by size, shape, and surface, confinement effects can be pronounced and thus provide new functionalities. The increased surface-to-volume ratio and subwavelength or mean-free-path proportional characteristic length scales and domains are behind many of the observed phenomenal nanoscale effects. For example, a semiconductor material engineered by spatial confinement, creating subbands and thus intersubband transitions, can lead to

the generation of radiation (e.g., quantum cascade lasers). In all-dielectric stacks [134,135], similar to semiconductor heterostructures [136], the alternating layers of specific dielectric functions (e.g., small imaginary part, high and low real part dielectrics) create useful photonic band structures [137] or giant ($\sim 10^4$) surface [137] or bulk field enhancement [135].

In the general case of a composite nanostructured material domain, such as a quantum well [138] of a given morphology or a gap-plasmonic structure [139,140], the ensuing quantum confinement furnishes a variety of enabling mechanisms [141–143] via tunneling, modification of local density of states, frustrated total internal reflection, mode coupling, etc. It is envisioned that the opportunities offered by fields, such as advanced nanophotonics [40,42,144,145], nanomaterials [47], and smart sensors, will be capitalized by EC to advance IoT and other network-based applications [113]. Nanosystems, such as nanophotonic crystal cavities, quantum dots, carbon nanotubes (CNT), and nanomaterials, and their composites allow information processing. Owing to the unique properties of nanomaterials and nanostructures, future processors [146] and integrated circuits [147,148] will exploit these nanosystems not only for computing and conveying information but also for storage of information [46,149,150].

To address the material challenges associated with the down-scaling of chips, new conductor materials, e.g., graphene nanoribbons [151] to create alternative interconnect [152,153] to replace copper and tungsten are needed [154]. In particular, obtaining new materials, physical basis, and mechanisms of potential to achieve improved processors, circuits, devices, and networks constitute one of the most impactful scientific challenges [155–165]. Searching for novel materials of potential use in HPC, several candidate materials have been proposed, including CNTs [166–169] and topological material design [170–176]. Extensive material characterization involving scanning probe microscopy and spectroscopy, and an array of surface probes and other analytical techniques are being employed to acquire a better understanding of nanomaterials. For example, many nanoscale transport properties of interest in transistor or chip design, e.g., plasmon transport in a nanowire or an electron or a phonon transport in a CNT or a semiconducting quantum dot, the mean-free-path (for scattering from impurity or other potentials) can be large leading to the electron or phonon motion being ballistic. Owing to unique light-matter interactions, electronic, mechanical, and thermal properties of nanosystems and innovative approaches to creating superior processors are evolving rapidly [41,46,146,177].

Since the invention of the point-contact transistor [178], transistors have evolved into the semiconducting building blocks of circuits built onto chips that make up the processor. CMOS (complementary metal-oxide-semiconductor) has been the workhorse of modern digital systems. While the CMOS technology enabled the creation of HPC, new functionalities and types of nanomaterials will enable the evolution of HPC [179,180]. The higher density of information-processing materials that also exhibit superior performance metrics of lower propagation delay and total power dissipation is envisioned to emerge from new nanomaterials, as depicted in the process loop in Figure 8.

For EC devices, minimizing power dissipation, which is related to the switching mechanisms in various transistor configurations, is critical. For example, switching in tunnel FET (TFET) occurs when barrier tunneling is modulated, whereas, in standard MOSFET (metal-oxide-semiconductor field-effect transistor), one modulates the thermionic emission across the barrier. The MOSFET operates in the subthreshold region when the gate voltage is below the threshold voltage. The subthreshold swing (related to MOSFET's I-V characteristic) of 60 mV/decade (a decade corresponds to a 10-times increase of the drain current), that is, if the gate voltage is increased by 60 mV, the drain current will increase by a factor of 10. The subthreshold swing 63 mV/decade of drain current at 300 K is a limit imposed by the charge carriers obeying the thermal Maxwell-Boltzmann distribution. Lower supply voltage transistors lead to the lower power consumption of the device. However, in FETs, the thermionic limit (~ 60 mV/decade) restricts the voltage. Using a graphene source with a CNT channel, a lower voltage of 40 mV/decade has been demonstrated [181]. Similarly, the lower voltage has been achieved in vertical gate-all-around nanowire GaSb/InAs (gallium antimonide/indium arsenide) TFETs, where a subthreshold swing of 40 mV/decade and a current of ~ 40 μ A/wire have been reported [182], or in the band, structure engineered GeSn (Germanium-Tin) TFET [183].

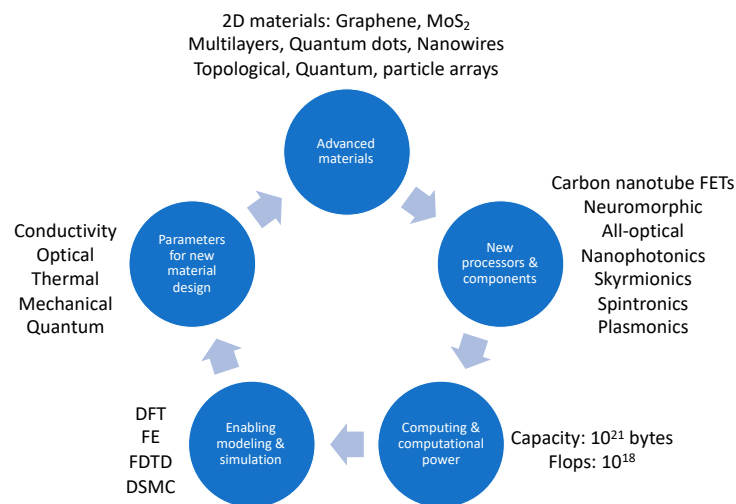


Figure 8. The process loop for the development of new processors. Examples of computational approaches including DFT (density functional theory), finite elements (FE), finite difference time domain (FDTD), and direct simulation Monte Carlo (DSMC) are given only generically.

The prime example of 1D and 2D nanomaterials of current interest within the enormous application space, comprising next-generation computing systems and circuit elements, includes CNTs and graphene, MoS₂, transition metal dichalcogenides, black phosphorus [139,184,185], etc. Building processors based on carbon nanomaterial FETs (MOSFET, CMOS, and the multi-gate transistors FinFET [186,187]) have been already demonstrated as in the case of CNT FET. Advanced FETs, such as CNT-based FinFETs [188,189] are being explored as a power-efficient node-scaled platform towards a chip with reduced transistor dimensions and thus increased density. Use of other nanomaterials of relevance includes fabrication and testing via self-assembly of block copolymers to achieve 7 nm node FinFETs [187], and Si, Ge, and SiGe nanowire FinFETs [190]. Block copolymers, belonging to the class of linear copolymers in which the different types of monomers cluster together to form blocks of repeating units, can controllably self-assemble at the nanoscale to form an important class of nanocomposites [185,191]. The resulting functional nanoscale objects can be conductive and semiconductive and, therefore, important to the electronics industry.

Other uses of polymeric nanomaterials include shape memory functionality, explored by IBM (international business machines) corporation through the “millipede” system aimed at developing ultrahigh density storage devices with terabit capacity, small form factor, and high data rate [192,193]. The thermomechanical data storage [193], based on the nanoscale heat-induced deformation in polymers to record and erase information to create novel high-density storage [192], has been explored using the capabilities of scanning probe microscopy (SPM), more specifically AFM (atomic force microscope). In addition to having been employed in the characterization of a plethora of solid-state electronics and photonics systems at the nanoscale, AFM is critically used in exploring the emerging high-density storage technologies beyond hard disk drives and flash memory [194]. Another instance, in which a probe-based approach is indispensable, is the use of ferroelectrics as a memory medium. In ferroelectric memory (capacitor type), the spontaneous polarization state of the crystal domains can be used to store bits of information, which can be changed via an external field [194]. For high-density data storage and rewritable data recording, the thin (few crystal lattice parameters) domain walls in ferroelectrics is a potential advantage since polarization changes occur over short distances.

The evolution of computer technologies, enabling increased computing power and improved SWaP, has taken the switching speed or clock frequency of the processors from 750 kHz (Intel 4004) to 8.6 GHz (AMD’s FX) [154]. As the processor merits (e.g., the loosely adopted trend of doubling of transistor number on a chip per two years, i.e., Moore’s law) is approaching its current limits,

novel processor architectures based on CNTs [149,195–199], or other nanomaterials [146,177] are being explored with tremendous prospects for the next generation computation and communication systems.

SWaP of processor units and related devices are expected to improve by employing the next generation of processors and on-chip integrated electronics [200] based on CNT [47,188,198,199,201–203], plasmonics [41,93,145,204–207], nano-optics, quantum computing [45,131,208], silicon photonics [144,145,209–211], optical interconnects (as opposed to metal interconnects) [212], and switches. In cases where the losses in plasmonic systems [213–215] may be an issue, all-dielectric resonances are emerging as an alternative approach [137].

Table 1. Novel nanomaterials and nanostructures of importance in the research and development of the next-generation computing systems.

Nanosystem	Typical Excitation	Application	References
Carbon nanotubes	Electron-hole transport	Transistor channel, cooling, vias, connectors	[216–221]
Nanowires and nanoantenna	Plasmons	Interconnect, connector, qubit	[146,207,222–227]
Quantum dots (doped, undoped Si, GaAs, etc.)	Excitons	Qubit	[226,228–235]
Silicon photonics components	Donor, electron, hole charge and spin states	Transistor material, qubits, quantum computing	[176,210,211]
Nanophotonics components	Photons, polaritons, plasmons	Transistor material, qubits, quantum computing	[204,216,231,233]
Organic compounds	Charge	Transistor material	[147]
Nitrogen vacancy	Spin states	Qubits, quantum computing	[205,236,237]
Trapped ions		Qubits, quantum computing	[131,238]
Nano- and micro-electromechanical systems (NEMS and MEMS)	Phonons	Readout	[193]
Superconductors	Electron	Qubits, quantum computing	[222,226]
Metamaterials and metasurfaces	Photons, phonons, plasmons	Transistor material, frequency conversion	[94,239–241]
Topological materials	Photons, phonons, plasmons, electrons	Interconnect, connector, qubit, transistor material	[170–174,176,222,242]
Metal-oxide-semiconductor and -metal tunnel junctions	Electron, plasmon, photon	Transistor material	[232,234]
Multilayers	Bloch surface waves	Interconnect	[94,135]

In exploring new mechanisms and systems for information encoding and transport toward technology alternatives for processors, FPGAs [107], interconnects [115], etc., use of nanotubes [47,149], nanowires [146,223,227,243], ferroelectric capacitors and FETs (FeFETs), and other nanosystems continue to be reported. While some candidate materials of potential use in nanoelectronics and for transferring information, such as CNTs [149,217], plasmonic nanowires [223], and all-dielectric stack optical nanofibers [244], have been discussed above, a more compact presentation of the nanosystems

of potential for the development of the next-generation processor and related components is given in Table 1.

Throughout this work, the central theme is how EC could take advantage of nanoscience and the related applications and thus enable the next superior technology. The applications cited seem to be in support of this theme. Our motivation here stems from the natural need for edge devices characterized by mobility and agile computing power at low energy consumption. However, a level of skepticism remains regarding the real progress and impact of EC across this very large range of fields that will be discussed next. Further research is thus warranted to establish the state of EC.

4.1. Carbon Nanotube CPU and Edge Device

A nanosystem of particular interest in nanoelectronics and thus of impact for EC is the carbon nanotube. Further reduction in the size of a large number of transistors fabricated on silicon wafers in the current state of chip manufacturing lead to impractical energy dissipation and transistor failure and thus loss of information. Silicon-based transistors, developed to be increasingly smaller, experience conductivity losses, leading to energy loss by generating heat. Replacing silicon-based elements with CNTs, owing to their more efficient electron transport properties, can lead to less energy requirements. In “How we made the carbon nanotube transistor” [166], C. Dekker provided a brief account on the creation of room-temperature transistors based on a single CNT as the channel material instead of bulk silicon [217,245].

CNTs are large aspect-ratio quantum wires [196,216,246,247] with promising electronic, plasmonic [145], thermal, and mechanical properties [188,248], and can be arranged and integrated compactly [47,198,200,249–252] towards new computer systems [217,253–267]. CNTs, as single carbon-atom thick cylindrical current carriers, have micrometers long electronic coherence lengths with electron mobility ~ 70 times higher than silicon and $\sim 25\%$ higher than other semiconductor materials. With the increasing number of bits of information that has to be processed via charge transport through the transistors, the superior mobility of the CNTs is significant. Following the creation of the first CNT transistor in 1998, logic gates [219] and, eventually, central processors have been demonstrated [268].

CNTs have a set of demonstrated advantageous properties, such as thermal, optical, and electronic properties. For example, mixed CNTs, containing both multi- and single-walled carbon nanotubes (MWCNTs and SWCNTs), have been also proposed as an interconnect for VLSI (very-large-scale integration) circuits [269]. Interestingly, CNT-polymer mixtures have been employed as the dynamical substrate in reservoir computing [270], a recurrent neural networks framework suited for dynamic (temporal) data processing [271]. The measurement of transport properties of individual CNTs [220] has identified both metallic [218,272] and semiconducting [245] characteristics. Similarly, both ballistic and diffusive phonon transport [221] of CNTs have been investigated at room temperature [273,274]. The determination of the electronic scattering mechanisms and quantized energy spectra [275] help exploiting these novel nanomaterials. Further characterization of CNTs, single and bundled (e.g., for allowing larger and faster transport than copper interconnects), as a function of CNT length, contact geometry, wrapping or chirality, and diameter (~ 0.4 nm–2 nm) will aid the future design [276–278].

Single-walled CNTs are cylindrically rolled-up graphene layers with useful electronic band structure and transport properties [279,280]. Many CNTs exhibit direct bandgap. CNTs' semiconducting bandgap approximately scales inversely with their diameter. With typical energy values of 1 eV for a 1 nm diameter CNTs, they are also of potential use as a quantum light source [216,279]. The general light emission properties of CNTs are via incandescence, electroluminescence, and photoluminescence. The intensity of the emitted light from the excitonic states can be controlled by current modulation (\sim GHz) and be enhanced via coupling to a cavity [281]. By engineering the photonic density of states via plasmonic or photonic environmental design, e.g., by use of a nanophotonic crystal cavity, it is possible to achieve proper modal volumes, optical quality factors, and Purcell enhancement, and thus a controllable optimum CNT-based on-chip light source [281].

Naturally, CNTs are p-type semiconductors, but n-type CNTs can also be achieved, for example, via electron doping (surface charge transfer from an electron donor) [282]. While efforts to incorporate CNTs as the transistor channel or as interconnect materials are ongoing, field-effect transistors (FET) and related development based on CNTs have been demonstrated [188,195,197–199,217,246,250,268,283–291], including results from IBM [167,292,293]. Very recently, using the CNT FETs, hyperdimensional computing has been experimentally demonstrated [47,149].

Various transport properties of CNTs (electrons or phonons in quantized and ballistic conductance) [221,294] may be exploited in a CNT-based transistor [217,268] or device, which is envisioned to outperform (same scale) silicon-based transistors. The appeal of higher speed and lower voltage operation of the CNT-based FETs derives fabrication and experimental efforts to achieve smaller system with recent reports of 5 nm gate length transistors conducting a larger current at 0.4 V than that achieved from the best silicon CMOS transistor (Intel's 14- and 22-nm Si CMOS FETs [295]) at 0.7 V [296].

Statistical estimates suggest that about 33% of fabricated CNTs exhibit metallic [218,272] rather than semiconducting properties [245,297]. With the current target purity of 0.0001%, various innovative approaches have been proposed to “filter” CNTs. Practical issues related to sorting between metallic and nonmetallic CNTs [298–300] for purity in response, nondestructive alignment on a chip [169,291,301], and overcoming CNT-metal junction barrier that limits transistor conductance [302], are being addressed. With improved implementation, multiple CNTs can be used to channel sufficient current in a transistor. To achieve sufficient current per transistor, >125 CNTs/ μm has been targeted [297]. Thus, the superior semiconducting properties of CNTs can be exploited in practical devices for faster switching ($\sim 10^{15}$ s) and thus better chip-making materials.

With a density of states of zero at the Fermi energy, graphene behaves as a zero-gap semiconductor or a metal, which can be inherited by the CNTs. With carbon atom each covalently bonded to the three neighboring carbons via their sp^2 states in a hexagonal lattice, the electronic band structure of the CNTs has been studied when investigating its transport properties [278,303].

The International Technology Roadmap for Semiconductors (ITRS) [304] is calling for “miniaturization of logic transistors by the progress of technology “nodes,” with smaller numbers indicating newer technologies for smaller and faster devices.” The prediction of ITRS for the device gate length is a reduction to 10 nm, with the contact critical dimension reduced to 11 nm, and 4-nm spacer width, to achieve an overall device footprint of 40 nm in the 3-nm technology node. These specifications have recently been met in a CNT transistor scaled to a 40-nanometer footprint [305]. Thus, CNTs will continue to play a major role in the next-generation processors, as well as in many sensors, both of which will enable powerful EC devices.

4.2. The Topological Edge States to Aid Edge Computing

In the ongoing efforts to increase the computing power while achieving an optimum SWaP that meets the demands of EC, work on 2D materials are gaining considerable momentum [306]. The effort is focused on achieving superior electronic transport properties in 2D materials when compared to silicon. With such superior materials, nanoelectronic devices (e.g., FETs) are envisioned to exhibit superior electrostatic control over their transport properties. Recent proposals on developing FETs based on 2D topological insulator ribbons are promising [307]. The transistor switching in topological FETs can be controlled via modulation of scattering since in topological materials [308] electrons can be protected from backscattering allowing the domain to lack resistivity.

Topological materials [170,172] are emerging as a new class of materials of great potential for novel optical, electronic, and quantum hardware. Such materials possess interesting surface or edge states that may enable high-speed and low-power computing and communication devices. Topological behavior can be exhibited by various electronic, photonic, and atomic systems, where the existence of specific states (e.g., edge states) facilitate electron conductance, photon propagation that is insensitive

to defects, disorders, and other disturbances [176]. The link between time-reversal symmetry (and other symmetries) and topology is of great importance in the electronic and photonic response of materials, such as topological insulators, i.e., materials that conduct charge on their surface but insulate in their interior [173,309]. The geometry of the electronic band structures in topological materials exhibits various arrangements that allow for unconventional surface states. Very recently, exploring the high-symmetry points in the Brillouin zone of various materials, nonmagnetic topological electronic materials have been cataloged [170] by calculating their invariant properties. Remarkably, Zhang et al. found that more than 8056 out of 26,688 materials examined are indeed topological, rendering nontrivial topology not exotic and scarce but abundant [170]. Concurrently, Vergniory et al. reported a similar finding by analyzing 26,938 stoichiometric materials (from the inorganic crystal structure database) [172]. Again, remarkably, 3307 topological insulators and 4078 topological semimetals were identified. As a result of their elementary or irreducible band representations (i.e., electronic bands that cannot be decomposed), Vergniory et al. estimated that more than 27% of all materials in nature were topological (out of which an estimated 12% were topological insulators) [172].

Consideration of topological properties of material within their electronic or photonic band structures, in analogy with mathematical topology, which links certain conserved quantities with continuous deformations, has recently generated an array of novel materials. The discovery of topological insulators, for example, has led to the demonstration of electron transport without dissipation, even in the presence of disturbances, such as defects and impurities. Similar to the specific topologies in the electronic band structures that support such useful transport properties, topologies in the wavevector-space can be created that supports photonic states, where light propagation can occur on the edges or boundaries without disturbance. For example, in novel materials, such as photonic crystals, and metamaterials, photonic waveguides may be designed to allow light propagation without back-reflection in the presence of imperfections [242].

Topological properties of low-dimensional materials are of particular interest since materials, such as graphene and CNTs, are already being explored for use in next-generation processors. For example, single-wall CNTs have been reported to be a topological insulator, due to winding number invariance (determining the number of edge states localized at the tube ends) [310]. With device feature sizes ~ 7 nm, CNTs are currently considered to be the most practical alternative for a transistor [297]. Use of topological materials to achieve processor size and performance advantages shares similar challenges as CNTs, including large scale fabrication and integration.

4.3. Nanophotonics and Plasmonics to Aid Edge Devices

The utility of light and optical excitations in various nanosystems is of tremendous importance for EC. In general, communication may be regarded as a transfer or exchange of information. Modulation is the essence of communication. Measurable variations in a quantity, such as the electric field amplitude, phase, or polarization, can provide a route to modulation and thus can convey information. Early examples include native American's messaging by smoke profile modulation. High-frequency modulation of light attributes is essential and can play a particular role for EC, where fast data processing and transfer is needed. Light-by-light modulation, an all-optical scheme, may provide a solution. However, direct light-by-light interaction is too weak, at least within the linear regime. Optical modulators typically rely on weak nonlinear light-matter interactions to accomplish light-by-light modulation. This is where the optical surface excitation of nanoparticles can provide a unique advantage. One approach is to utilize plasmons in communication. How do we implement a surface plasmon-based communication in a potential system/device? The physical implementation of modulation, using plasmon supporting nanostructures, offers a path. However, despite large volumes of investigation, no concrete consensus has been reached as to which physical system is most appropriate for light-by-light modulation.

Photons can outperform electrons in many aspects of communication and high-speed information networks, including long-distance communication. Additionally, both classical and nonclassical states

of light (e.g., coherent and squeezed quantum states) are being explored for the development of novel processors. Furthermore, photons can couple to collective electronic density oscillations, i.e., plasmon excitation and other quasiparticles in solids, and cause a range of fascinating near- and far-field phenomena. Plasmonic devices [205,207,311–314] are envisioned for several potential applications, including facilitating readout, amplification, modulation, etc., leading to on-chip nearfield devices and achieve operations, such as plasmon-induced transparency [315]. Quantum light (e.g., single-photon) sources [216] and detectors integrated with nanophotonic components provide a basis for developing all-optical processors [43], secure fast communications, and metrology. These features will accelerate the development of EC devices and can play a key role in the emerging quantum networks edge-nodes, or AI hardware platforms [316].

Fiber-optics introduced a drastically improved communication by capitalizing on the field propagation properties of fibers and the capability of modulating the fields. To be viable and a superior alternative to silicon chips, new photonic processors [40–42,44] must permit a high level of integration [45,317]. However, many optical systems are limited by diffraction, scattering, and losses. Additionally, (light-by-light) modulation, as the essence of information, is challenging, in particular, within the linear regime. However, in the nonlinear regime, optical modulation is possible by exploiting the weak light-matter interactions. Such modulation of light with light [213] can be enhanced or enabled via excitons in quantum dots [228,233], plasmons in nanowires [223,224], and 2D materials [318–320]. As a result, metallic, dielectric, and metallo-dielectric composites and multilayer thin films and particles, metasurfaces [239,241] and metamaterials [240], photonic crystals [321], and topological [322,323] and quantum materials [324] are all being actively explored to achieve new photonic functionalities [43,45]. Use of these emerging materials, in conjunction with light-matter interactions and the ensuing electronic, photonic, and phononic excitations (e.g., surface modes, plasmons, polaritons, etc.) [144,145,318,325], is paving the way for the development of compact, addressable, switchable, and optical components and systems [40,41,204,212,326]. An example is the integrated microwave photonics [327], where ultra-small high-bandwidth components, such as electro-optic modulators, frequency synthesizers, and chip signal processors, have been developed. Thanks to the maturity of the semiconductor industry, the integration of photonic components (light sources, detectors, splitters, modulators, polarizers, etc.) in a single microwave photonic processor chip is feasible [40]. Therefore, the development of optical signal processors [40] capable of similar functionality, modularity, and configurability as those of the electronic circuits is possible. The tremendous implication and impact of such communications and information processing capabilities and the perspectives of interoperability and relation with quantum [45] and neuromorphic photonics have been recently reviewed [327].

The potential of photonics to achieve high-speed computing and information processing [40,42] is also noticeable from on-chip devices capable of integrating [44] or solving differential equations [209].

While many photonic devices have been recognized to be of potential, to be a viable technology, integrated photonics is envisioned to take advantage of the well-established microelectronics CMOS foundries. Silicon photonics aims to fabricate passive and active photonic circuits on silicon substrates [211]. The very-large-scale integration of electronics and photonics to create dense electronic-photonic systems, on chips, will benefit processors, memory interconnects, ultrahigh bandwidth RF (radio frequency) signal processing, photonic A/D conversion, and other applications in optical interconnects and optical signal processing [328]. Monolithic photonic integration by use of state-of-the-art CMOS foundry infrastructure has been demonstrated to produce large numbers of nanophotonic devices integrated with high-density transistors. Specifically, sharing the same CMOS process mask set, grating-coupled microring-resonator filter banks [211] have been fabricated to achieve wavelength-division-multiplexing [329]. Similarly, fabricating optical waveguides and resonators, high-speed optical modulators and photodetectors, in conjunction with millions of transistors, operations at ten gigabits/s in a single optical bus for wavelength division multiplexing, has been reported [330]. Complete on-chip electro-optic modulators and systems (~5 Gb/s) and interfaces (including infrared detectors and receivers) to improve the processor-to-memory communication

energy have been demonstrated for 5 fJ/bit operation at 1.5 dB insertion loss and 8 dB extinction ratio [331].

Emerging nanomaterials and functional low-dimensional systems are particularly appealing as the physical basis for new processors, memory, and interconnect architectures. The VCSEL (vertical-cavity surface-emitting laser) technology has been explored through major initiatives for connectivity in modern data centers [332]. Connecting multiple servers, memory, and computing resources, optical interconnects at terabit/s is an enabling technology for the next-generation data centers [333]. Within integrated photonics and computing architectures, important challenges remain regarding photonic network-on-chip and chip-to-chip architectures [334]. However, significant flexibility is offered by photonics. For example, an information-carrying photon may be converted to an information-carrying plasmon that can then propagate through a quantum plasmonic [335,336] circuit in an optical computer or processor. The clock of a plasmonic chip may be designed based upon the surface plasmon amplification by stimulated emission of radiation (spacer) [337].

Undoubtedly, the collective electronic (e.g., plasmonic) effects in nanoparticles and nanostructures of certain materials are of potential importance in information and communication science. When the charge density is perturbed out of equilibrium, coherent electron oscillations can propagate through the material. When quantized, plasmons, the quanta of the density waves, can be created or annihilated, leading to a resonant scattering, absorption, field enhancement, and confinement of potential use in novel optical switches and modulators, which can be employed in integrated photonic devices, in the development of new on-chip or chip-to-chip interconnects, and in achieving computing functionality and implementation of a cellular automata algorithm [338]. Plasmon excitation and transport in CNT and graphene nanoribbons have been explored for their role in conduction in electrical interconnects in the THz range [152].

With the current trend of megawatts' energy consumption by data centers and HPCs, new low power and power-efficient interconnect technologies are needed for exascale computing and beyond. By 2020, the traffic in data centers is projected to be ~15 Zettabytes, i.e., a two-fold increase from 2017, with nearly 77% of the traffic accounting for intra data center needs [339]. Optical, photonic, and plasmonic interconnects are of potential for achieving the needed energy-efficiency and bandwidth-density [340].

Further flexibility offered by photonics is in crystals where photon propagation is governed by the naturally occurring periodic structure. Of use is propagation that can be manipulated or prohibited over some spectral bands, that is feasible in materials possessing artificial periodic structures. Such photonic bandgap materials are useful for optical processors (switches, modulators, etc.) similar to semiconducting materials in silicon-based electronics. In many cases, numerical and computational techniques, such as the finite difference time domain (FDTD) and time or frequency domain finite element (FE) methods, can be employed in the understanding (forward problem) and design (inverse problem) of photonic materials toward specific processing needs. Since photons are bosons, they do not readily interact, making the photonic device calculations easier, typically requiring the solutions of the photon wave equation (Maxwell's equations). Compared to the determination of the response of the electronic systems, requiring the many-body interaction (electron correlation) or the solution of the many-particle Schrödinger equation, such photonic advantages are however offset by the difficulties in localization and confining photons, making device miniaturization and integration nontrivial.

Most metal-based nanostructures that support collective electronic excitation are dissipative and generate heat (e.g., nonradiative decay of plasmons [341,342]), and thus may ultimately not be suitable for tight integration. Such challenges may be circumvented by the use of all-dielectric devices, which are promising candidates for the control and confinement of light [135,137].

4.4. Quantum Processor and Computing to Aid Edge Devices

Effects, such as scattering, and losses sustained by electrons confined to smaller dimensions can limit their use as information carriers or in signal transduction. However, the fundamental physical phenomena that place limitations upon the further increase of the density of the conventional

information processing materials also offer new opportunities for drastically breaking the conventional computing records [208]. Capitalizing upon quantum effects, such as the distinct polarization states of a photon or the spin states of an atomic or subatomic system, quantum computers [131] are envisioned to achieve operation on data with merits beyond the reach of any classical computer (the so-called quantum supremacy). Extensive research is ongoing to stably represent and manipulate information carried by a quantum system. Unlike the use of binary digits (bits) in classical computing, in a quantum computing platform, information is encoded using quantum bits (qubits); for example, the two orthogonal polarization states of photons or the states of a two-level quantum system and the superpositions of those states. Changes in the state or operations on the qubits lead to information processing.

Quantum dots made of composite metal, dielectric, or semiconductor materials are of potential as physical systems for hosting qubits. Being essentially 0D materials, their nanoscale dimensions allow arrangements of a large number of nodes on a surface with sufficient spatial separation to preserve the integrity of the qubits in a quantum processor.

Spin, as an intrinsic property of particles and measured to assume different quantized states for bosons (integer values) and fermions (half-integer values), has been identified as an information carrier for computing. For example, the spin (and charge) states of a semiconducting quantum dot allow it to be an ideal nanosystem for quantum computing. Further information on scientific advantages can be gleaned off by fermions and bosons obeying Fermi–Dirac (preserving Pauli exclusion) and Bose–Einstein (not preserving Pauli exclusion) statistics, respectively. Bose–Einstein condensate, using cold atoms (e.g., the alkali metal rubidium) that can be trapped or can trap an ion, shows fascinating many-body behavior of potential use in quantum devices [343].

In addition to photons as the information-carrying particles, dopants in silicon [344] or defects in diamond [345] are also being explored as potential atomic-scale qubits with stable coherence time and operation at room temperature. In diamond, a vacancy in the atomic structure can possess useful spin properties. The nitrogen-vacancy (NV) centers exhibit useful electron-spin coherence and relaxation times [237]. Similarly, qubits may be obtained from 2D materials, such as molybdenum disulfide [177] or graphene [206,319,320], which can host single donors with charge and spin states that can be controlled.

The predicted impact of quantum information science (e.g., quantum computing [45] and information processing), AI, machine learning, and their convergence [346] on EC devices will be hard to overestimate [347]. To realize quantum computing [45], quantum internet [347], and by extension quantum edge devices, a central topic is the identification of qubits that possess long coherence times, that is, sufficient times under which the information-carrying system stays in a superposition state to allow the transmission of information. Insufficient coherence times lead to the loss of quantum information and errors. Quantum gates operate on qubits, and thus the coherence time should be much longer than the time the gate needs to complete its operation [345]. To achieve a processor capable of controlling many qubits, the platform has to be scalable, and any errors due to noise and loss of coherence must be corrected (quantum error correction and fault-tolerant quantum computation) [348]. To benefit from quantum computing, in addition to the quantum hardware, development of quantum algorithms is also necessary.

For an object in an arbitrary unknown quantum state, one cannot precisely measure or perfectly replicate that state. However, the state can be teleported to another object, that is, transfer of the state without the physical transfer of the object. These and similar effects are being currently considered for long-distance communication [349,350]. The EC device communication could greatly benefit from such quantum effects, which have been demonstrated using optical fibers and terrestrial free-space channels over distances of ~100 km, and free space channels over distances of ~1400 km [349].

Quantum edge devices may be readily envisioned to incorporate quantum sensors that generate data to be processed by quantum processors and algorithms and communicated through quantum internet [347,349]. Further prospects of EC may be anticipated from the emerging distributed quantum sensing [351], where quantum correlations are exploited between multiple sensors to achieve superior

measurement of unknown parameters overcoming the limits of unentangled sensors. The emergence of the powerful capabilities of EC and quantum sensing, distributed or not, warrants an investigation of their specific and unique synergy. An important concern regarding the expansion of EC devices is security, for which quantum effects may provide powerful solutions [350]. Quantum key distribution is one such potential solution, where unconditional communication security between distant parties can be guaranteed by working with photons in quantum superposition states [350]. Additionally, cyber-physical systems are evolving into a state where processing occurs at the distributed sensing layer and not in a centralized manner [352]. EC will need new hardware platforms consistent with increased computing performance. Thus, distributed computing can bring physical sensors to a whole new potential for quality and operational capabilities.

An important application area for EC is cellular technology. Satellites provide services by accessing ground computing centers to transmit data. This process consumes a large amount of bandwidth and generates a delay. To improve resource utilization, computing power, and delay, the ground 5G mobile communications network employs EC. The mobile EC (MEC) distributes part of the computing resources to the edge of the network, thus saving bandwidth and reducing delay. For further improvements, a 5G satellite EC framework has been proposed [353] in addition to existing EC for terrestrial 5G communication. In addition to EC's potential to overcome the problems anticipated for cloud computing, further capabilities may be created by exploiting quantum effects that drastically boost satellite communication, as evident from a recent report, where teleportation of single-photon qubits was employed for ground-to-satellite communication [349]. Another impressive example is the recent report on using quantum key distribution to achieve secure communication from the satellite to the ground [350]. Thus, global quantum networks may become a reality in the near future. As such, despite the early stage of quantum technologies, efforts are underway to investigate and develop quantum networks edge-nodes. Such nodes are defined to be network locations capable of hosting quantum subsystems, such as photon detectors, transmitters and receivers, quantum buffers and memories, etc. These nodes are needed for connecting quantum information system applications (e.g., a quantum sensor) to the optical quantum networks. Quantum networks edge-nodes are then considered to provide peer-to-peer services at the quantum applications layer, i.e., a distributed application architecture. Through such an architecture, tasks and workloads are partitioned between equally privileged participants (peers) in the quantum application. An example of such peer-to-peer service is the ability to convert stationary qubits (e.g., generated by a trapped ion or other quantum applications) into flying qubits, which are suitable for transmission via optical fiber communication systems. Other service examples include transmission of flying qubits between specified locations. While the potential advantages of quantum processing for EC require further maturation of the quantum information science, the concept of a quantum edge device may stimulate further research.

4.5. Neuromorphic Computing and Edge Devices

The advances in the discovery and development of new HPC processors will undoubtedly impact the deployment of countless EC and IoT devices that are being envisioned. Since EC envisions to bring intelligence and connectivity to virtually all aspects of sensing, fast processing and communication of the large-scale (per sensing element) data generated is critical [354]. This is not unlike the amount of data and computing power of the sensory organs and brain of a human (~1 GB/s data from the eyes alone; and 10^{16} brain operations/s [355,356], and ~20 W power consumption [357]) to produce a decision. In the traditional computing realm, the memory and processing unit are separated, limiting data communication rate (the so-called von Neumann limit). Neuromorphic computing [358] is touted as a potential approach to address the inherent limitations of conventional silicon technology. Biological systems exhibit complex dynamics and responses that are being increasingly exploited in many fields, including sensing and computing [359–361], for example, as described in “neuromorphic engineering” [356], where a brief account is given on some of the early developments of brain-like technologies and neural circuits. Neuromorphic or brain-inspired computing, unlike the serial

processing of traditional digital computers, is envisioned to achieve massive parallel analog computing at high speed and low power [362]. To be comparable to the brain, neuromorphic hardware requires $\sim 10^{11}$ neurons [363] and thus needs to be extremely energy-efficient. An increasing number of studies are emerging toward achieving the basic elements needed to build neuromorphic devices [357,364–369], including the recent work on “evolvable organic electrochemical transistor”, which was reported to mimic the biological synapse [148]. Remarkably, similar to biological synapses, which establish, evolve, and operate, the devised transistor channel, formed by an electropolymerized conducting polymer, the first synaptic device was produced that generated new synapses within its working environment [148].

In the neural system, the synapse functions as an active memory unit, enabling learning and memory (with an energy consumption of ~ 1 –100 fJ per synaptic event [370]). A logical approach to implementing neuromorphic processors is the emulation of a synapse [354], which requires a compact and scalable physical basis if it is to be integrated into a three-dimensional architecture [365]. For example, intended to operate analogously to a synapse between neurons, a memristor [357,371] can alter its resistance dynamically depending on its history and thus can possess multilevel accessible conductance states, a useful feature for neuromorphic systems [372,373]. Memristive devices have also been used in sparse coding and dimension lowering, envisioned to aid neuromorphic computing [355,374]. Similarly, nanoscale spintronic oscillators, exhibiting nonlinearity, memory, and stability, have been experimented with to emulate collections of neurons [375]. Other recent developments, related to mimicking a synapse or synaptic behavior, include an electrochemical neuromorphic organic device made of inexpensive plastic material [376], neuromorphic circuits to emulate a sense of touch [377], memristive response using ionic effects in MoS_2 [378], quantum effects in superconducting circuits [366], photonic integrated-circuit synapse [354], quantum dots-based photonic synapse [370], oxide-based photonic synapse [379], single flux quantum circuits [380], and use of aligned CNT transistors [381].

In memristors, conductance can be modulated continuously by applying a voltage, a feature that can be used to naturally implement analog vector and matrix multiplication. How precisely the modulation occurs depends on the number of conductance states. Memristors, allowing analog computing, are particularly useful for EC and IoT as faster and more energy-efficient computing can be achieved when compared to conventional digital computing [382]. An example is a vector-matrix multiplication, which constitutes a core computing task, e.g., in signal processing and deep neural networks, both of which are fundamental for EC. Memristor crossbars, providing reconfigurable non-volatile resistance states, can be used for efficient analog signal and image processing as an alternative processing method for EC and IoT. Memristors could thus eliminate the speed and energy efficiency bottleneck. Using hafnium oxide memristors on top of metal-oxide-semiconductor transistors, signal processing, image compression, and convolutional filtering have been demonstrated [383]. Other exploratory investigations using memristor arrays include solving classic control problems associated with reinforcement learning algorithms that use deep neural networks [384].

In the quest for a competitive neuromorphic CPU, the experimental system of IBM stands out. The TrueNorth with a 5.4×10^9 transistors chip was reported in 2014 [385]. It featured 1×10^6 spiking neurons and 256×10^6 synapses but a power density of only 20 mW/cm², compared to tens of W of typical CPUs. A comparison of power densities and clock frequencies of processors with those of the brain has been reported by Merolla et al. [385]. Industry research efforts in developing neuromorphic processors are also producing novel results. The 60-mm² chip Loihi is a neuromorphic many-core processor fabricated on Intel’s 14-nm process [386,387]. It implements spiking neural networks with on-chip learning and has been shown to outperform other approaches in solving the LASSO (Least Absolute Shrinkage and Selection Operator) optimization problem [386,387].

4.6. Discussions

Having briefly surveyed the rapidly growing number of EC-related reports (see Figure 1) and considering the state of the technologies discussed above, the true contribution of EC to these fields

appear modest or hard to assess otherwise. Many of the fields noted are oblivious of EC. To date, the reported EC-related studies appear to be largely extensions of cloud-based scenarios, and considerations and are only weakly connected to what may be perceived as uniquely EC. On the one hand, the technologies above appear to offer or be of potential to offer hardware components and ingredients towards building the core systems of an edge device (e.g., low power high-performance processors). On the other hand, there are a number of algorithms and software efforts that aim to distinguish EC as a new computing paradigm (e.g., EC simulators [116]). Without catalyzed interaction between these two domains, progress may remain modest. While it may be challenging to sketch a road map for achieving the EC vision with respect to nanosystems, for these seemingly disparate fields to cooperatively achieve the EC vision, dissemination and exchange of the core characteristics of EC need to occur across these disciplines. In a sense, one may consider the traditional state of biology versus the emerging state of physical sciences biology, where increasingly models, theories, and experiments from mathematics, physics, and engineering are transforming our understanding and use of biological systems. In turn, biology stimulates and poses new challenges to physical and mathematical modeling and theories of physical systems. The EC could benefit from a similar convergence. For example, one may consider a molecular biologist as an EC investigator addressing questions, such as the development of a local information storing or computing protein to serve the processing needs of a local biomolecular sensor. Such problem statement within biology may be of potential to break the barrier between the fields.

5. Conclusions

While efforts to formulate uniquely EC-use cases are underway, the presented review sketches the overall state of the field. Whereas electronics may have been a major precursor of EC, nanoelectronics is here emphasized as essential for the evolution of EC. In an all-inclusive EC value-chain and ecosystem, nanoscience is an essential stakeholder. From the perspective of novel systems of potential for EC-specialized applications, discerning the technological challenges in achieving faster, smaller, and more energy-efficient processors and components, including interconnects, storage, communication, and software, helps to define the broader scope of the EC as a field. Clearly, despite the growing number of reports that are sharpening the boundaries of the EC field, the cross-disciplinary nature of the field must also be considered. This is not unlike the cross-disciplinary field of nanoscience, which provides the potential hardware and implementation solutions for EC, as described in the case of CNT-based transistors for post-Moore needs. However, in turn, emerging unique EC-use cases also provide new challenges for nanoscience. For example, from the presented discussion on CNT synaptic transistors for neuromorphic computing, it may be surmised that nanosystems and EC may amalgamize to become an inseparable entity, where device and function interact dynamically. Measuring the global needs for better and new sensors, it can readily be concluded that increasing the computing power and the intelligence of the sensors is only a natural evolution of the related industries. The majority of EC devices are expected to be fast, compact, low power, and resilient to becoming compromised (hardware and software). The processor unit that could give the EC sensors and devices the needed intelligence to provide an “edge” advantage needs also meet these same criteria. Remarkably, EC appears to impact a plethora of scientific and technological fields as it overcomes many challenges, such as the potential risk for increased hacking vector and licensing costs. Clearly, important challenges remain to be addressed with respect to security, software upgrade, and others related to the touted EC advantages. From the brief review presented, it may be concluded that the role of nanomaterials and nanosystems in overcoming these obstacles takes the center stage. Not only the hardware that accommodates the computing power, intelligence, and communication capacity of the EC devices but also the signal generating sensors and controlling actuators benefit from the extraordinary properties of the reviewed materials. With the rising fusion of the IoT devices globally, EC could help to unburden the resulting colossal computing and communication loads. In turn, the evolution of EC devices and the synergy among the sensing, computing, and AI components are expected to enable new scientific and technological capabilities. As the EC device dimensions are pushed to smaller scales

to achieve higher density integration, the boundaries of nanosystems and EC further merge. It may be argued that the state of the nanosystems-EC field is only at its infancy with such perspectives as collective and holistic responses from high connectivity, synchronized, and real-time EC devices may be tamed to provide new horizons of information technological capabilities. Mathematical problems, for the spatial distribution of edge devices, or the rate of computing and data exchange, etc. may be formulated, to better understand the underlying complexity, and thus emergence. EC will reach its climax as novel nanosystems that switch fast, dissipate less energy per switching, implement functions, transport information-carrying signals fast and with little dissipation per unit length are discovered and harnessed. Currently, materials that exhibit topological and quantum behavior, metamaterials, and nanoparticles and nanowires that can be integrated are under consideration. With evolving nanosystems, one may envision molecular systems, e.g., proteins and DNAs, as EC devices. With sensing at the atomic and molecular levels, nanoscale communication, molecular processing, and nano-EC devices may pave the way to nano-IoT. Molecular networks of billions of sensors already occur in biological systems, and this may be mimicked by nano-EC devices. Can the human body be regarded as a centralized cloud-based system? How would an EC-augmented human be envisioned? In the tradition of cloud-computing, nanosystems and EC will stimulate future applications with far-reaching impact.

Acknowledgments: This work was supported by the United States Department of Defense (DoD) and used resources of the Computational Research and Development Programs at Oak Ridge National Laboratory (ORNL). ORNL is managed by UT-Battelle, LLC, for the US DOE under contract DE-AC05-00OR22725.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Spanner, K.; Gloss, R. New Challenges in Nanopositioning Technologies. In Proceedings of the International Conference and Exhibition on New Actuators and Drive Systems, Bremen, Germany, 14–16 June 2010; pp. 258–263.
2. Bolonkin, A.A. Femtotechnology: Design of the Strongest AB Matter for Aerospace. *J. Aerosp. Eng.* **2010**, *23*, 281–292. [[CrossRef](#)]
3. Khan, N.; Abas, N.; Kalair, A.R. Electronic and Photonic Communique Bottlenecks Mandate Ultrafast Optics. *Nonlinear Opt. Quantum Opt.* **2017**, *48*, 185–192.
4. Jones, D.E.H. Nano—Remaking the World Atom by Atom—Regis, E. *Nature* **1995**, *374*, 835–837. [[CrossRef](#)]
5. Vaughan, O. A closer look at the atoms in a molecule. *Nat. Nanotechnol.* **2009**, *4*, 619. [[CrossRef](#)] [[PubMed](#)]
6. Vaughan, O. Fullerene synthesis Caught on camera. *Nat. Nanotechnol.* **2010**, *5*, 386. [[CrossRef](#)] [[PubMed](#)]
7. Vaughan, O. Scanning probe microscopy a discerning look at the bonds in a molecule. *Nat. Nanotechnol.* **2012**, *7*, 619. [[CrossRef](#)] [[PubMed](#)]
8. Joachim, C. Bonding more atoms together for a single molecule computer. *Nanotechnology* **2002**, *13*, R1–R7. [[CrossRef](#)]
9. Vaughan, O. Molecular switches order and control. *Nat. Nanotechnol.* **2008**, *3*, 644. [[CrossRef](#)]
10. Endres, M.; Bernien, H.; Keesling, A.; Levine, H.; Anschuetz, E.R.; Krajenbrink, A.; Senko, C.; Vuletic, V.; Greiner, M.; Lukin, M.D. Atom-by-atom assembly of defect-free one-dimensional cold atom arrays. *Science* **2016**, *354*, 1024–1027. [[CrossRef](#)] [[PubMed](#)]
11. Barredo, D.; de Leseleuc, S.; Lienhard, V.; Lahaye, T.; Browaeys, A. An atom-by-atom assembler of defect-free arbitrary two-dimensional atomic arrays. *Science* **2016**, *354*, 1021–1023. [[CrossRef](#)]
12. Barredo, D.; Lienhard, V.; De Leseleuc, S.; Lahaye, T.; Browaeys, A. Synthetic three-dimensional atomic structures assembled atom by atom. *Nature* **2018**, *561*, 79–82. [[CrossRef](#)] [[PubMed](#)]
13. Vaughan, O. Patterned surfaces—An organized union. *Nat. Nanotechnol.* **2008**, *3*, 526. [[CrossRef](#)]
14. Electronic Computers in Molecular Quantum Mechanics. *Nature* **1956**, *177*, 362. [[CrossRef](#)]
15. Normile, D. Molecular computing—DNA-based computer takes aim at genes. *Science* **2002**, *295*, 951. [[CrossRef](#)] [[PubMed](#)]
16. Goldup, S. Molecular machines swap rings. *Nature* **2018**, *557*, 39–40. [[CrossRef](#)] [[PubMed](#)]

17. Moe-Behrens, G.H. The biological microprocessor, or how to build a computer with biological parts. *Comput. Struct. Biotechnol. J.* **2013**, *7*, e201304003. [[CrossRef](#)] [[PubMed](#)]
18. Dunn, K.E.; Trefzer, M.A.; Johnson, S.; Tyrrell, A.M. Towards a Bioelectronic Computer: A Theoretical Study of a Multi-Layer Biomolecular Computing System That Can Process Electronic Inputs. *Int. J. Mol. Sci.* **2018**, *19*, 2620. [[CrossRef](#)]
19. Hilbert, M.; Lopez, P. The World's Technological Capacity to Store, Communicate, and Compute Information. *Science* **2011**, *332*, 60–65. [[CrossRef](#)]
20. Forbes, B.D.M. Big Data Market Revenues Are Projected to Increase from \$42B in 2018 to \$103B in 2027 #BigData#Analytics. Available online: <http://www.forbes.com/sites/louiscolombus/2018/05/23/10-charts-that-will-change-your-perspective-of-big-datas-growth/> (accessed on 15 June 2019).
21. Henno, J. Information and Interaction. *Front. Artif. Intell. Appl.* **2017**, *292*, 426–449. [[CrossRef](#)]
22. Gleick, J. The Information: A History, a Theory, a Flood. *IEEE Trans. Inf. Theory* **2011**, *57*, 6332–6333. [[CrossRef](#)]
23. Robinson, A. The Information a History, a Theory, a Flood. *Science* **2011**, *333*, 1826–1827. [[CrossRef](#)]
24. Davis, C.H. The Information: A History, a Theory, a Flood. *J. Am. Soc. Inf. Sci. Technol.* **2011**, *62*, 2543–2545. [[CrossRef](#)]
25. Misa, T.J. The Information: A History, a Theory, a Flood. *Nature* **2011**, *471*, 300–301. [[CrossRef](#)]
26. Smillie, K. The information: A History, a Theory, a Flood. *IEEE Ann. Hist. Comput.* **2012**, *34*, 99–101.
27. Hobart, M.E. The Information: A History, a Theory, a Flood. *Technol. Cult.* **2014**, *55*, 489–490. [[CrossRef](#)]
28. Akan, O.B.; Andreev, S.; Dobre, C. Internet of Things and Sensor Networks. *IEEE Commun. Mag.* **2019**, *57*, 40. [[CrossRef](#)]
29. Jaeik, C.; Chilamkurti, N.; Wang, S.J. Editorial of special section on enabling technologies for industrial and smart sensor internet of things systems. *J. Supercomput.* **2018**, *74*, 4171–4172. [[CrossRef](#)]
30. Akmandor, A.O.; Yin, H.X.; Jha, N.K. Smart, Secure, Yet Energy-Efficient, Internet-of-Things Sensors. *IEEE Trans. Multi-Scale Comput. Syst.* **2018**, *4*, 914–930. [[CrossRef](#)]
31. Marx, V. The Big Challenges of Big Data. *Nature* **2013**, *498*, 255–260. [[CrossRef](#)]
32. Han, L.X. Towards Sustainable Smart Society: Big Data Driven Approaches. In Proceedings of the International Conference on Future Networks and Distributed Systems (ICFNDS '17), Cambridge, UK, 19–20 July 2017. [[CrossRef](#)]
33. The Digital Universe in 2020: Big Data, Bigger Digital Shadows, and Biggest Growth in the Far East. 2012. Available online: www.emc.com/leadership/digital-universe/index.htm (accessed on 15 June 2019).
34. Kothe, D.; Lee, S.; Qualters, I. Exascale Computing in the United States. *Comput. Sci. Eng.* **2019**, *21*, 17–29. [[CrossRef](#)]
35. Satyanarayanan, M. How we created edge computing. *Nat. Electron.* **2019**, *2*, 42. [[CrossRef](#)]
36. Svorobej, S.; Endo, P.T.; Bendeche, M.; Filelis-Papadopoulos, C.; Giannoutakis, K.M.; Gravvanis, G.A.; Tzovaras, D.; Byrne, J.; Lynn, T. Simulating Fog and Edge Computing Scenarios: An Overview and Research Challenges. *Future Internet* **2019**, *11*, 55. [[CrossRef](#)]
37. Ai, Y.; Peng, M.G.; Zhang, K.C. Edge computing technologies for Internet of Things: A primer. *Digit. Commun. Netw.* **2018**, *4*, 77–86. [[CrossRef](#)]
38. Mao, Y.Y.; You, C.S.; Zhang, J.; Huang, K.B.; Letaief, K.B. A Survey on Mobile Edge Computing: The Communication Perspective. *IEEE Commun. Surv. Tutor.* **2017**, *19*, 2322–2358. [[CrossRef](#)]
39. Mach, P.; Becvar, Z. Mobile Edge Computing: A Survey on Architecture and Computation Offloading. *IEEE Commun. Surv. Tutor.* **2017**, *19*, 1628–1656. [[CrossRef](#)]
40. Liu, W.L.; Li, M.; Guzzon, R.S.; Norberg, E.J.; Parker, J.S.; Lu, M.Z.; Coldren, L.A.; Yao, J.P. A fully reconfigurable photonic integrated signal processor. *Nat. Photonics* **2016**, *10*, 190–195. [[CrossRef](#)]
41. Gogoi, N.; Sahu, P.P. All-Optical Surface Plasmonic Universal Logic Gate Devices. *Plasmonics* **2016**, *11*, 1537–1542. [[CrossRef](#)]
42. Brunner, D.; Soriano, M.C.; Mirasso, C.R.; Fischer, I. Parallel photonic information processing at gigabyte per second data rates using transient states. *Nat. Commun.* **2013**, *4*. [[CrossRef](#)]
43. Fu, Y.L.; Hu, X.Y.; Lu, C.C.; Yue, S.; Yang, H.; Gong, Q.H. All-Optical Logic Gates Based on Nanoscale Plasmonic Slot Waveguides. *Nano Lett.* **2012**, *12*, 5784–5790. [[CrossRef](#)] [[PubMed](#)]
44. Ferrera, M.; Park, Y.; Razzari, L.; Little, B.E.; Chu, S.T.; Morandotti, R.; Moss, D.J.; Azana, J. On-chip CMOS-compatible all-optical integrator. *Nat. Commun.* **2010**, *1*. [[CrossRef](#)] [[PubMed](#)]

45. Kwiat, P.G. Quantum information—An integrated light circuit. *Nature* **2008**, *453*, 294–295. [[CrossRef](#)]
46. Shulaker, M.M.; Hills, G.; Wong, H.S.P.; Mitra, S. Transforming Nanodevices to Next Generation Nanosystems. In Proceedings of the 2016 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), Agios Konstantinos, Greece, 17–21 July 2016; pp. 288–292.
47. Shulaker, M.; Wong, H.S.P.; Mitra, S. Computing With Carbon Nanotubes. *IEEE Spectr.* **2016**, *53*, 26–52. [[CrossRef](#)]
48. Jäck, B.; Xie, Y.; Li, J.; Jeon, S.; Bernevig, B.A.; Yazdani, A. Observation of a Majorana zero mode in a topologically protected edge channel. *Science* **2019**. [[CrossRef](#)]
49. Mohammadi Estakhri, N.; Edwards, B.; Engheta, N. Inverse-designed metastructures that solve equations. *Science* **2019**, *363*, 1333. [[CrossRef](#)]
50. Pinna, D.; Araujo, F.A.; Kim, J.V.; Cros, V.; Querlioz, D.; Bessiere, P.; Droulez, J.; Grollier, J. Skyrmion Gas Manipulation for Probabilistic Computing. *Phys. Rev. Appl.* **2018**, *9*. [[CrossRef](#)]
51. Lee, V.T.; Alaghi, A.; Pamula, R.; Sathe, V.S.; Ceze, L.; Oskin, M. Architecture Considerations for Stochastic Computing Accelerators. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2018**, *37*, 2277–2289. [[CrossRef](#)]
52. Alaghi, A.; Qian, W.K.; Hayes, J.P. The Promise and Challenge of Stochastic Computing. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2018**, *37*, 1515–1531. [[CrossRef](#)]
53. Alaghi, A.; Hayes, J.P. Computing with randomness Stochastic computing, a 50-year-old idea, is set for a comeback. *IEEE Spectr.* **2018**, *55*, 46–51. [[CrossRef](#)]
54. Web of Science. Available online: [http://apps.webofknowledge.com/WOS_GeneralSearch_input.do?product=WOS&search_mode=GeneralSearch&SID=7BM5N2TzxEC4pCic7w\]&preferencesSaved=](http://apps.webofknowledge.com/WOS_GeneralSearch_input.do?product=WOS&search_mode=GeneralSearch&SID=7BM5N2TzxEC4pCic7w]&preferencesSaved=) (accessed on 15 June 2019).
55. Satyanarayanan, M.; Bahl, P.; Caceres, R.; Davies, N. The Case for VM-Based Cloudlets in Mobile Computing. *IEEE Pervasive Comput.* **2009**, *8*, 14–23. [[CrossRef](#)]
56. Satyanarayanan, M.; Kistler, J.J.; Mummert, L.B.; Ebling, M.R.; Kumar, P.; Lu, Q. Experience with Disconnected Operation in a Mobile Computing Environment. In Proceedings of the Usenix Mobile & Location-Independent Computing Symposium, Cambridge, MA, USA, 2–3 August 1993; pp. 11–28.
57. Satyanarayanan, M. Mobile Computing. *Computer* **1993**, *26*, 81–82. [[CrossRef](#)]
58. Vaughan, O. Working on the edge. *Nat. Electron.* **2019**, *2*, 2–3. [[CrossRef](#)]
59. Tu, W.Q.; Pop, F.; Jia, W.J.; Wu, J.; Iacono, M. High-Performance Computing in Edge Computing Networks. *J. Parallel Distrib. Comput.* **2019**, *123*, 230. [[CrossRef](#)]
60. Take it to the edge. *Nat. Electron.* **2019**, *2*, 1. [[CrossRef](#)]
61. Suarez-Albela, M.; Fraga-Lamas, P.; Fernandez-Carames, T.M. A Practical Evaluation on RSA and ECC-Based Cipher Suites for IoT High-Security Energy-Efficient Fog and Mist Computing Devices. *Sensors* **2018**, *18*, 3868. [[CrossRef](#)]
62. Park, D.; Kim, S.; An, Y.; Jung, J.Y. LiReD: A Light-Weight Real-Time Fault Detection System for Edge Computing Using LSTM Recurrent Neural Networks. *Sensors* **2018**, *18*, 2110. [[CrossRef](#)]
63. Amazon Elastic Compute Cloud (Amazon EC2). Available online: <https://aws.amazon.com/ec2/> (accessed on 15 June 2019).
64. Google Cloud Platform. Available online: <https://cloud.google.com/> (accessed on 15 June 2019).
65. Wachter, S. Data protection in the age of big data. *Nat. Electron.* **2019**, *2*, 6–7. [[CrossRef](#)]
66. Yang, Y. Multi-tier computing networks for intelligent IoT. *Nat. Electron.* **2019**, *2*, 4–5. [[CrossRef](#)]
67. Mujica, G.; Rodriguez-Zurrunero, R.; Wilby, M.; Portilla, J.; Gonzalez, A.B.R.; Araujo, A.; Riesgo, T.; Diaz, J.J.V. Edge and Fog Computing Platform for Data Fusion of Complex Heterogeneous Sensors. *Sensors* **2018**, *18*, 3630. [[CrossRef](#)]
68. Cha, H.J.; Yang, H.K.; Song, Y.J. A Study on the Design of Fog Computing Architecture Using Sensor Networks. *Sensors* **2018**, *18*, 3633. [[CrossRef](#)]
69. Chen, Y.S.; Tsai, Y.T. A Mobility Management Using Follow-Me Cloud-Cloudlet in Fog-Computing-Based RANs for Smart Cities. *Sensors* **2018**, *18*, 489. [[CrossRef](#)]
70. Barrias, A.; Casas, J.R.; Villalba, S. A Review of Distributed Optical Fiber Sensors for Civil Engineering Applications. *Sensors* **2016**, *16*, 748. [[CrossRef](#)]
71. Inaudi, D.; Glisic, B. Long-Range Pipeline Monitoring by Distributed Fiber Optic Sensing. *J. Press. Vessel Technol.* **2010**, *132*. [[CrossRef](#)]

72. Wang, J.; Li, D. Adaptive Computing Optimization in Software-Defined Network-Based Industrial Internet of Things with Fog Computing. *Sensors* **2018**, *18*, 2509. [[CrossRef](#)]
73. Qureshi, F.; Krishnan, S. Wearable Hardware Design for the Internet of Medical Things (IoMT). *Sensors* **2018**, *18*, 3812. [[CrossRef](#)]
74. Klonoff, D.C. Fog Computing and Edge Computing Architectures for Processing Data From Diabetes Devices Connected to the Medical Internet of Things. *J. Diabetes Sci. Technol.* **2017**, *11*, 647–652. [[CrossRef](#)]
75. Srivastava, M.; Suvarna, S.; Srivastava, A.; Bharathiraja, S. Automated emergency paramedical response system. *Health Inf. Sci. Syst.* **2018**, *6*, 22. [[CrossRef](#)]
76. Kumari, P.; Lopez-Benitez, M.; Gyu Myoung, L.; Tae-Seong, K.; Minhas, A.S. Wearable Internet of Things—From human activity tracking to clinical integration. In Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Seogwipo, Korea, 11–15 July 2017; pp. 2361–2364. [[CrossRef](#)]
77. Henson, A.B.; Gromski, P.S.; Cronin, L. Designing Algorithms To Aid Discovery by Chemical Robots. *ACS Cent. Sci.* **2018**, *4*, 793–804. [[CrossRef](#)]
78. Kang, J.; Eom, D.S. Offloading and Transmission Strategies for IoT Edge Devices and Networks. *Sensors* **2019**, *19*, 835. [[CrossRef](#)]
79. Murakami, M.; Kominami, D.; Leibnitz, K.; Murata, M. Drawing Inspiration from Human Brain Networks: Construction of Interconnected Virtual Networks. *Sensors* **2018**, *18*, 1133. [[CrossRef](#)]
80. Jang, I.; Lee, D.; Choi, J.; Son, Y. An Approach to Share Self-Taught Knowledge between Home IoT Devices at the Edge. *Sensors* **2019**, *19*, 833. [[CrossRef](#)]
81. Taherizadeh, S.; Stankovski, V.; Grobelsnik, M. A Capillary Computing Architecture for Dynamic Internet of Things: Orchestration of Microservices from Edge Devices to Fog and Cloud Providers. *Sensors* **2018**, *18*, 2938. [[CrossRef](#)]
82. Dinh, N.T.; Kim, Y. An Efficient Availability Guaranteed Deployment Scheme for IoT Service Chains over Fog-Core Cloud Networks. *Sensors* **2018**, *18*, 3970. [[CrossRef](#)]
83. An, C.; Wu, C.; Yoshinaga, T.; Chen, X.; Ji, Y. A Context-Aware Edge-Based VANET Communication Scheme for ITS. *Sensors* **2018**, *18*, 2022. [[CrossRef](#)]
84. Fan, X.; Cui, T.; Cao, C.; Chen, Q.; Kwak, K.S. Minimum-Cost Offloading for Collaborative Task Execution of MEC-Assisted Platooning. *Sensors* **2019**, *19*, 847. [[CrossRef](#)]
85. Dong, C.; Wen, W. Joint Optimization for Task Offloading in Edge Computing: An Evolutionary Game Approach. *Sensors* **2019**, *19*, 740. [[CrossRef](#)]
86. Sun, Y.; Lin, F.; Zhang, N. A security mechanism based on evolutionary game in fog computing. *Saudi J. Biol. Sci.* **2018**, *25*, 237–241. [[CrossRef](#)]
87. Zhao, Y.; Wu, J.; Li, W.; Lu, S. Efficient Interference Estimation with Accuracy Control for Data-Driven Resource Allocation in Cloud-RAN. *Sensors* **2018**, *18*, 3000. [[CrossRef](#)]
88. Zeng, F.; Ren, Y.; Deng, X.; Li, W. Cost-Effective Edge Server Placement in Wireless Metropolitan Area Networks. *Sensors* **2018**, *19*, 32. [[CrossRef](#)]
89. Wu, Y.; Chen, X.; Shi, J.; Ni, K.; Qian, L.; Huang, L.; Zhang, K. Optimal Computational Power Allocation in Multi-Access Mobile Edge Computing for Blockchain. *Sensors* **2018**, *18*, 3472. [[CrossRef](#)]
90. Deniz, O.; Vallez, N.; Espinosa-Aranda, J.L.; Rico-Saavedra, J.M.; Parra-Patino, J.; Bueno, G.; Moloney, D.; Dehghani, A.; Dunne, A.; Pagani, A.; et al. Eyes of Things. *Sensors* **2017**, *17*, 1173. [[CrossRef](#)]
91. Mora-Gimeno, F.J.; Mora-Mora, H.; Marcos-Jorquera, D.; Volckaert, B. A Secure Multi-Tier Mobile Edge Computing Model for Data Processing Offloading Based on Degree of Trust. *Sensors* **2018**, *18*, 3211. [[CrossRef](#)]
92. Fan, K.; Yin, J.; Zhang, K.; Li, H.; Yang, Y. EARS-DM: Efficient Auto Correction Retrieval Scheme for Data Management in Edge Computing. *Sensors* **2018**, *18*, 3616. [[CrossRef](#)]
93. Gogoi, N.; Sahu, P.P. Compact surface plasmonic waveguide component for integrated optical processor. In Proceedings of the International Conference on Optics and Photonics 2015, Kolkata, India, 20–22 February 2015. [[CrossRef](#)]
94. Silva, A.; Monticone, F.; Castaldi, G.; Galdi, V.; Alu, A.; Engheta, N. Performing Mathematical Operations with Metamaterials. *Science* **2014**, *343*, 160–163. [[CrossRef](#)]
95. Rodriguez-Zurrunero, R.; Utrilla, R.; Rozas, A.; Araujo, A. Process Management in IoT Operating Systems: Cross-Influence between Processing and Communication Tasks in End-Devices. *Sensors* **2019**, *19*, 805. [[CrossRef](#)]

96. Zhang, H.; Chen, Z.; Wu, J.; Deng, Y.; Xiao, Y.; Liu, K.; Li, M. Energy-Efficient Online Resource Management and Allocation Optimization in Multi-User Multi-Task Mobile-Edge Computing Systems with Hybrid Energy Harvesting. *Sensors* **2018**, *18*, 3140. [[CrossRef](#)]
97. Perez-Torres, R.; Torres-Huitzil, C.; Galeana-Zapien, H. A Cognitive-Inspired Event-Based Control for Power-Aware Human Mobility Analysis in IoT Devices. *Sensors* **2019**, *19*, 832. [[CrossRef](#)]
98. Nguyen, Q.N.; Liu, J.; Pan, Z.; Benkacem, I.; Tsuda, T.; Taleb, T.; Shimamoto, S.; Sato, T. PPCS: A Progressive Popularity-Aware Caching Scheme for Edge-Based Cache Redundancy Avoidance in Information-Centric Networks. *Sensors* **2019**, *19*, 694. [[CrossRef](#)]
99. Avgeris, M.; Spatharakis, D.; Dechouniotis, D.; Kalatzis, N.; Roussaki, I.; Papavassiliou, S. Where There Is Fire There Is SMOKE: A Scalable Edge Computing Framework for Early Fire Detection. *Sensors* **2019**, *19*, 639. [[CrossRef](#)]
100. Nguyen, V.C.; Dinh, N.T.; Kim, Y. A Distributed NFV-Enabled Edge Cloud Architecture for ICN-Based Disaster Management Services. *Sensors* **2018**, *18*, 4136. [[CrossRef](#)]
101. Zhu, L.; Fu, Y.; Chow, R.; Spencer, B.F.; Park, J.W.; Mechitov, K. Development of a High-Sensitivity Wireless Accelerometer for Structural Health Monitoring. *Sensors* **2018**, *18*, 262. [[CrossRef](#)]
102. Zhang, X.; Lin, J.; Chen, Z.; Sun, F.; Zhu, X.; Fang, G. An Efficient Neural-Network-Based Microseismic Monitoring Platform for Hydraulic Fracture on an Edge Computing Architecture. *Sensors* **2018**, *18*, 1828. [[CrossRef](#)] [[PubMed](#)]
103. Sun, J.; Wang, X.; Wang, S.; Ren, L. A searchable personal health records framework with fine-grained access control in cloud-fog computing. *PLoS ONE* **2018**, *13*, e0207543. [[CrossRef](#)] [[PubMed](#)]
104. Athavale, Y.; Krishnan, S. A Device-Independent Efficient Actigraphy Signal-Encoding System for Applications in Monitoring Daily Human Activities and Health. *Sensors* **2018**, *18*, 2966. [[CrossRef](#)] [[PubMed](#)]
105. Oueida, S.; Kotb, Y.; Aloqaily, M.; Jararweh, Y.; Baker, T. An Edge Computing Based Smart Healthcare Framework for Resource Management. *Sensors* **2018**, *18*, 4307. [[CrossRef](#)] [[PubMed](#)]
106. Rosario, D.; Schimunek, M.; Camargo, J.; Nobre, J.; Both, C.; Rochol, J.; Gerla, M. Service Migration from Cloud to Multi-tier Fog Nodes for Multimedia Dissemination with QoE Support. *Sensors* **2018**, *18*, 329. [[CrossRef](#)] [[PubMed](#)]
107. Rodriguez, A.; Valverde, J.; Portilla, J.; Otero, A.; Riesgo, T.; de la Torre, E. FPGA-Based High-Performance Embedded Systems for Adaptive Edge Computing in Cyber-Physical Systems: The ARTICo(3) Framework. *Sensors* **2018**, *18*, 1877. [[CrossRef](#)] [[PubMed](#)]
108. Deak, N.; Cret, O.; Echim, M.; Teodorescu, E.; Negrea, C.; Vacariu, L.; Munteanu, C.; Hangan, A. Edge computing for space applications: Field programmable gate array-based implementation of multiscale probability distribution functions. *Rev. Sci. Instrum.* **2018**, *89*, 125005. [[CrossRef](#)] [[PubMed](#)]
109. Chen, C.L.; Chuang, C.T. A QRS Detection and R Point Recognition Method for Wearable Single-Lead ECG Devices. *Sensors* **2017**, *17*, 1969. [[CrossRef](#)]
110. Idrees, Z.; Zou, Z.; Zheng, L. Edge Computing Based IoT Architecture for Low Cost Air Pollution Monitoring Systems: A Comprehensive System Analysis, Design Considerations & Development. *Sensors* **2018**, *18*, 3021. [[CrossRef](#)]
111. Ferrandez-Pastor, F.J.; Garcia-Chamizo, J.M.; Nieto-Hidalgo, M.; Mora-Martinez, J. Precision Agriculture Design Method Using a Distributed Computing Architecture on Internet of Things Context. *Sensors* **2018**, *18*, 1731. [[CrossRef](#)]
112. Ferrandez-Pastor, F.J.; Garcia-Chamizo, J.M.; Nieto-Hidalgo, M.; Mora-Pascual, J.; Mora-Martinez, J. Developing Ubiquitous Sensor Network Platform Using Internet of Things: Application in Precision Agriculture. *Sensors* **2016**, *16*, 1141. [[CrossRef](#)] [[PubMed](#)]
113. Huang, D.; Xu, C.; Zhao, D.; Song, W.; He, Q. A Multi-Objective Partition Method for Marine Sensor Networks Based on Degree of Event Correlation. *Sensors* **2017**, *17*, 2168. [[CrossRef](#)] [[PubMed](#)]
114. Zhong, P.; Zhang, Y.; Ma, S.; Kui, X.; Gao, J. RCSS: A Real-Time On-Demand Charging Scheduling Scheme for Wireless Rechargeable Sensor Networks. *Sensors* **2018**, *18*, 1601. [[CrossRef](#)] [[PubMed](#)]
115. Scionti, A.; Mazumdar, S.; Portero, A. Towards a Scalable Software Defined Network-on-Chip for Next Generation Cloud. *Sensors* **2018**, *18*, 2330. [[CrossRef](#)] [[PubMed](#)]
116. Sonmez, C.; Ozgovde, A.; Ersoy, C. EdgeCloudSim: An environment for performance evaluation of edge computing systems. *Trans. Emerg. Telecommun. Technol.* **2018**, *29*. [[CrossRef](#)]

117. Wang, H.Z.; Xiong, F.; Li, J.N.; Shi, S.F.; Li, J.Z.; Gao, H. Data management on new processors: A survey. *Parallel Comput.* **2018**, *72*, 1–13. [[CrossRef](#)]
118. Bu, L.K.; Mark, M.; Kinsy, M.A. A Short Survey at the Intersection of Reliability and Security in Processor Architecture Designs. In Proceedings of the 2018 IEEE Computer Society Annual Symposium on VLSI, Hong Kong, China, 8–11 July 2018; pp. 118–123. [[CrossRef](#)]
119. Blake, G.; Dreslinski, R.G.; Mudge, T. A Survey of Multicore Processors A review of their common attributes. *IEEE Signal Process. Mag.* **2009**, *26*, 26–37. [[CrossRef](#)]
120. Vazhkudai, S.S.; Supinski, B.R.d.; Bland, A.S.; Geist, A.; Sexton, J.; Kahle, J.; Zimmer, C.J.; Atchley, S.; Oral, S.; Maxwell, D.E.; et al. The design, deployment, and evaluation of the CORAL pre-exascale systems. In Proceedings of the International Conference for High Performance Computing, Networking, Storage, and Analysis, Dallas, TX, USA, 11–16 November 2018; pp. 1–12.
121. Patterson, D. 50 years of Computer Architecture: From the Mainframe CPU to the Domain-Specific TPU and the Open RISC-V Instruction Set. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 27–31.
122. Patterson, D. Reduced Instruction Set Computers Then and Now. *Computer* **2017**, *50*, 10–12. [[CrossRef](#)]
123. RISC-V. 2019. Available online: <https://riscv.org> (accessed on 15 June 2019).
124. Karandikar, S.; Mao, H.; Kim, D.; Biancolin, D.; Amid, A.; Lee, D.; Pemberton, N.; Amaro, E.; Schmidt, C.; Chopra, A.; et al. FireSim: FPGA-Accelerated Cycle-Exact Scale-Out System Simulation in the Public Cloud. *IEEE Micro* **2019**, *39*, 56–65. [[CrossRef](#)]
125. ARM. Available online: <https://www.arm.com/> (accessed on 15 June 2019).
126. Zhang, Y.Q.; Khayat-zadeh, M.; Yang, K.Y.; Saligane, M.; Pinckney, N.; Alioto, M.; Blaauw, D.; Sylvester, D. iRazor: Current-Based Error Detection and Correction Scheme for PVT Variation in 40-nm ARM Cortex-R4 Processor. *IEEE J. Solid-State Circuits* **2018**, *53*, 619–631. [[CrossRef](#)]
127. Neoverse. Available online: <https://www.arm.com/products/silicon-ip-cpu/neoverse/neoverse-n1> (accessed on 15 June 2019).
128. NVIDIA. Available online: <https://www.nvidia.com/en-us/data-center/products/egx-edge-computing/> (accessed on 15 June 2019).
129. APC. Available online: <https://www.apc.com/us/en/solutions/business-solutions/edge-computing.jsp> (accessed on 15 June 2019).
130. Open Edge Computing Initiative. Available online: <https://www.openedgecomputing.org/> (accessed on 15 June 2019).
131. Monroe, C.; Kim, J. Scaling the Ion Trap Quantum Processor. *Science* **2013**, *339*, 1164–1169. [[CrossRef](#)] [[PubMed](#)]
132. Ohl de Mello, D.; Schäffner, D.; Werkmann, J.; Preuschoff, T.; Kohfahl, L.; Schlosser, M.; Birkel, G. Defect-Free Assembly of 2D Clusters of More Than 100 Single-Atom Quantum Systems. *Phys. Rev. Lett.* **2019**, *122*, 203601. [[CrossRef](#)] [[PubMed](#)]
133. Molmer, K.; Sorensen, A. RISQ—Reduced instruction set quantum computers. *J. Mod. Opt.* **2000**, *47*, 2515–2527. [[CrossRef](#)]
134. Spassov, D.; Paskaleva, A.; Krajewski, T.A.; Guzewicz, E.; Luka, G.; Ivanov, T. Al₂O₃/HfO₂ Multilayer High-k Dielectric Stacks for Charge Trapping Flash Memories. *Phys. Status Solidi A* **2018**, *215*. [[CrossRef](#)]
135. Amra, C.; Zerrad, M.; Lemarchand, F.; Lereu, A.; Passian, A.; Zapien, J.A.; Lequime, M. Energy density engineering via zero-admittance domains in all-dielectric stratified materials. *Phys. Rev. A* **2018**, *97*. [[CrossRef](#)]
136. Xu, W.G.; Liu, W.W.; Schmidt, J.F.; Zhao, W.J.; Lu, X.; Raab, T.; Diederichs, C.; Gao, W.B.; Seletskiy, D.V.; Xiong, Q.H. Correlated fluorescence blinking in two-dimensional semiconductor heterostructures. *Nature* **2017**, *541*, 62–67. [[CrossRef](#)] [[PubMed](#)]
137. Lereu, A.L.; Zerrad, M.; Passian, A.; Amra, C. Surface plasmons and Bloch surface waves: Towards optimized ultra-sensitive optical sensors. *Appl. Phys. Lett.* **2017**, *111*. [[CrossRef](#)]
138. Vigneau, F.; Mizokuchi, R.; Zanuz, D.C.; Huang, X.H.; Tang, S.S.; Maurand, R.; Frolov, S.; Sammak, A.; Scappucci, G.; Lefloch, F.; et al. Germanium Quantum-Well Josephson Field-Effect Transistors and Interferometers. *Nano Lett.* **2019**, *19*, 1023–1027. [[CrossRef](#)] [[PubMed](#)]

139. Chen, C.; Youngblood, N.; Peng, R.M.; Yoo, D.; Mohr, D.A.; Johnson, T.W.; Oh, S.H.; Li, M. Three-Dimensional Integration of Black Phosphorus Photodetector with Silicon Photonics and Nanoplasmonics. *Nano Lett.* **2017**, *17*, 985–991. [[CrossRef](#)]
140. Davis, T.J.; Gomez, D.E.; Roberts, A. Plasmonic circuits for manipulating optical information. *Nanophotonics* **2017**, *6*, 543–559. [[CrossRef](#)]
141. Engel, M.; Steiner, M.; Lombardo, A.; Ferrari, A.C.; Lohneysen, H.V.; Avouris, P.; Krupke, R. Light-matter interaction in a microcavity-controlled graphene transistor. *Nat. Commun.* **2012**, *3*. [[CrossRef](#)] [[PubMed](#)]
142. Steiner, M.; Xia, F.N.; Qian, H.H.; Lin, Y.M.; Hartschuh, A.; Meixner, A.J.; Avouris, P. Carbon Nanotubes and Optical Confinement—Controlling Light Emission in Nanophotonic Devices. In *Carbon Nanotubes and Associated Devices, Proceedings of the Nanoscience + Engineering, San Diego, CA, USA, 10–14 August 2008*; Volume 7037, p. 10111712801630.
143. Ray, S.K.; Katiyar, A.K.; Raychaudhuri, A.K. One-dimensional Si/Ge nanowires and their heterostructures for multifunctional applications—A review. *Nanotechnology* **2017**, *28*. [[CrossRef](#)] [[PubMed](#)]
144. Peng, J.; Sun, S.; Narayana, V.K.; Sorger, V.J.; El-Ghazawi, T. Residue number system arithmetic based on integrated nanophotonics. *Opt. Lett.* **2018**, *43*, 2026–2029. [[CrossRef](#)] [[PubMed](#)]
145. Otto, L.M.; Ogletree, D.F.; Aloni, S.; Staffaroni, M.; Stipe, B.C.; Hammack, A.T. Visualizing the bidirectional optical transfer function for near-field enhancement in waveguide coupled plasmonic transducers. *Sci. Rep.* **2018**, *8*. [[CrossRef](#)] [[PubMed](#)]
146. Yan, H.; Choe, H.S.; Nam, S.W.; Hu, Y.J.; Das, S.; Klemic, J.F.; Ellenbogen, J.C.; Lieber, C.M. Programmable nanowire circuits for nanoprocessors. *Nature* **2011**, *470*, 240–244. [[CrossRef](#)]
147. Crone, B.; Dodabalapur, A.; Lin, Y.Y.; Filas, R.W.; Bao, Z.; LaDuca, A.; Sarpeshkar, R.; Katz, H.E.; Li, W. Large-scale complementary integrated circuits based on organic transistors. *Nature* **2000**, *403*, 521–523. [[CrossRef](#)] [[PubMed](#)]
148. Gerasimov, J.Y.; Gabrielson, R.; Forchheimer, R.; Stavrinidou, E.; Simon, D.T.; Berggren, M.; Fabiano, S. An Evolvable Organic Electrochemical Transistor for Neuromorphic Applications. *Adv. Sci.* **2019**, *6*, 1801339. [[CrossRef](#)]
149. Wu, T.F.; Li, H.T.; Huang, P.C.; Rahimi, A.; Hills, G.; Hodson, B.; Hwang, W.; Rabaey, J.M.; Wong, H.S.P.; Shulaker, M.M.; et al. Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration. *IEEE J. Solid-State Circuits* **2018**, *53*, 3183–3196. [[CrossRef](#)]
150. Luo, S.; Song, M.; Li, X.; Zhang, Y.; Hong, J.; Yang, X.; Zou, X.; Xu, N.; You, L. Reconfigurable Skyrmion Logic Gates. *Nano Lett.* **2018**, *18*, 1180–1184. [[CrossRef](#)]
151. Sharma, H.; Sandha, K.S. Multilayer Graphene Nanoribbon (MLG NR) as VLSI Interconnect Material at Nano-scaled Technology Nodes. *Trans. Electr. Electron. Mater.* **2018**, *19*, 456–461. [[CrossRef](#)]
152. Paddubskaya, A.; Shuba, M.; Maksimenko, S.; Maffucci, A. Plasmonic carbon interconnects to enable the THz technology: Properties and limits. In Proceedings of the 2017 IEEE 21st Workshop on Signal and Power Integrity (SPI), Baveno, Italy, 7–10 May 2017.
153. Chen, Z.H. Applications of 2D Materials in Interconnect Technology. In Proceedings of the 2018 International Symposium on Vlsi Technology, Systems and Application (Vlsi-Tsa), Hsinchu, Taiwan, 16–19 April 2018.
154. Vyas, A.A.; Zhou, C.J.; Yang, C.Y. On-Chip Interconnect Conductor Materials for End-of-Roadmap Technology Nodes. *IEEE Trans. Nanotechnol.* **2018**, *17*, 4–10. [[CrossRef](#)]
155. Xia, Z.B.; Wang, C.Y.; Kalarickal, N.K.; Stemmer, S.; Rajan, S. Design of Transistors Using High-Permittivity Materials. *IEEE Trans. Electron Devices* **2019**, *66*, 896–900. [[CrossRef](#)]
156. Rios, C.; Youngblood, N.; Cheng, Z.G.; Le Gallo, M.; Pernice, W.H.P.; Wright, C.D.; Sebastian, A.; Bhaskaran, H. In-memory computing on a photonic platform. *Sci. Adv.* **2019**, *5*. [[CrossRef](#)] [[PubMed](#)]
157. Hu, W.G.; Zhang, C.; Wang, Z.L. Recent progress in piezotronics and tribotronics. *Nanotechnology* **2019**, *30*. [[CrossRef](#)] [[PubMed](#)]
158. Alam, M.A.; Si, M.; Ye, P.D. A critical review of recent progress on negative capacitance field-effect transistors. *Appl. Phys. Lett.* **2019**, *114*, 090401. [[CrossRef](#)]
159. Sun, H.D.; Gerasimov, J.; Berggren, M.; Fabiano, S. n-Type organic electrochemical transistors: Materials and challenges. *J. Mater. Chem. C* **2018**, *6*, 11778–11784. [[CrossRef](#)]
160. Schanze, K.S. Forum on Materials and Interfaces for Next-Generation Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2018**, *10*, 25833. [[CrossRef](#)]

161. Iannaccone, G.; Bonaccorso, F.; Colombo, L.; Fiori, G. Quantum engineering of transistors based on 2D materials heterostructures. *Nat. Nanotechnol.* **2018**, *13*, 183–191. [[CrossRef](#)]
162. Hwang, C.S.; Dieny, B. Advanced memory-Materials for a new era of information technology. *MRS Bull.* **2018**, *43*, 330–333. [[CrossRef](#)]
163. Zhang, Y.H.; Mei, Z.X.; Liang, H.L.; Du, X.L. Review of flexible and transparent thin-film transistors based on zinc oxide and related materials. *Chin. Phys. B* **2017**, *26*. [[CrossRef](#)]
164. Kumar, B.; Kaushik, B.K.; Negi, Y.S. Organic Thin Film Transistors: Structures, Models, Materials, Fabrication, and Applications: A Review. *Polym. Rev.* **2014**, *54*, 33–111. [[CrossRef](#)]
165. Zhou, Y.; Ramanathan, S. Correlated Electron Materials and Field Effect Transistors for Logic: A Review. *Crit. Rev. Solid State Mater. Sci.* **2013**, *38*, 286–317. [[CrossRef](#)]
166. Dekker, C. How we made the carbon nanotube transistor. *Nat. Electron.* **2018**, *1*, 518. [[CrossRef](#)]
167. Han, S.J.; Tang, J.S.; Kumar, B.; Falk, A.; Farmer, D.; Tulevski, G.; Jenkins, K.; Afzali, A.; Oida, S.; Ott, J.; et al. High-speed logic integrated circuits with solution-processed self-assembled carbon nanotubes. *Nat. Nanotechnol.* **2017**, *12*, 861–865. [[CrossRef](#)] [[PubMed](#)]
168. Hu, Z.Y.; Comeras, J.M.M.L.; Park, H.; Tang, J.S.; Afzali, A.; Tulevski, G.S.; Hannon, J.B.; Liehr, M.; Han, S.J. Physically unclonable cryptographic primitives using self-assembled carbon nanotubes. *Nat. Nanotechnol.* **2016**, *11*, 559–565. [[CrossRef](#)] [[PubMed](#)]
169. Cao, Q.; Han, S.J.; Tulevski, G.S.; Zhu, Y.; Lu, D.D.; Haensch, W. Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics. *Nat. Nanotechnol.* **2013**, *8*, 180–186. [[CrossRef](#)] [[PubMed](#)]
170. Zhang, T.T.; Jiang, Y.; Song, Z.D.; Huang, H.; He, Y.Q.; Fang, Z.; Weng, H.M.; Fang, C. Catalogue of topological electronic materials. *Nature* **2019**, *566*, 475–479. [[CrossRef](#)]
171. Xue, H.R.; Yang, Y.H.; Gao, F.; Chong, Y.D.; Zhang, B.L. Acoustic higher-order topological insulator on a kagome lattice. *Nat. Mater.* **2019**, *18*, 108–112. [[CrossRef](#)] [[PubMed](#)]
172. Vergniory, M.G.; Elcoro, L.; Felser, C.; Regnault, N.; Bernevig, B.A.; Wang, Z.J. A complete catalogue of high-quality topological materials. *Nature* **2019**, *566*, 480–485. [[CrossRef](#)]
173. Tang, F.; Po, H.C.; Vishwanath, A.; Wan, X. Comprehensive search for topological materials using symmetry indicators. *Nature* **2019**, *566*, 486–489. [[CrossRef](#)]
174. Ni, X.; Weiner, M.; Alu, A.; Khanikaev, A.B. Observation of higher-order topological acoustic states protected by generalized chiral symmetry. *Nat. Mater.* **2019**, *18*, 113–120. [[CrossRef](#)] [[PubMed](#)]
175. He, H.L.; Qiu, C.Y.; Ye, L.P.; Cai, X.X.; Fan, X.Y.; Ke, M.Z.; Zhang, F.; Liu, Z.Y. Topological negative refraction of surface acoustic waves in a Weyl phononic crystal. *Nature* **2018**, *560*, 61–64. [[CrossRef](#)] [[PubMed](#)]
176. Hafezi, M.; Mittal, S.; Fan, J.; Migdall, A.; Taylor, J.M. Imaging topological edge states in silicon photonics. *Nat. Photonics* **2013**, *7*, 1001–1005. [[CrossRef](#)]
177. Wachter, S.; Polyushkin, D.K.; Bethge, O.; Mueller, T. A microprocessor based on a two-dimensional semiconductor. *Nat. Commun.* **2017**, *8*, 14948. [[CrossRef](#)] [[PubMed](#)]
178. Bardeen, J. Research Leading to Point-Contact Transistor. *Science* **1957**, *126*, 105–112. [[CrossRef](#)] [[PubMed](#)]
179. Aly, M.M.S.; Wu, T.F.; Bartolo, A.; Malviya, Y.H.; Hwang, W.; Hills, G.; Markov, I.; Wootters, M.; Shulaker, M.M.; Wong, H.S.P.; et al. The N3XT Approach to Energy-Efficient Abundant-Data Computing. *Proc. IEEE* **2019**, *107*, 19–48. [[CrossRef](#)]
180. Balestra, F. Nanoscale FETs for high performance and ultra low power operation at the end of the Roadmap. In Proceedings of the 2018 14th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Qingdao, China, 31 October–3 November 2018; pp. 46–49.
181. Qiu, C.G.; Liu, F.; Xu, L.; Deng, B.; Xiao, M.M.; Si, J.; Lin, L.; Zhang, Z.Y.; Wang, J.; Guo, H.; et al. Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches. *Science* **2018**, *361*, 387–391. [[CrossRef](#)]
182. Vasen, T.; Ramvall, P.; Afzalian, A.; Doornbos, G.; Holland, M.; Thelander, C.; Dick, K.A.; Wernersson, L.E.; Passlack, M. Vertical Gate-All-Around Nanowire GaSb-InAs Core-Shell n-Type Tunnel FETs. *Sci. Rep.* **2019**, *9*. [[CrossRef](#)]
183. Pandey, R.; Ghosh, R.; Datta, S. Band Structure Engineered Germanium-Tin (GeSn) p-channel Tunnel Transistors. In Proceedings of the 2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 25–27 April 2016.

184. Nourbakhsh, A.; Zubair, A.; Sajjad, R.N.; Tavakkoli, K.G.A.; Chen, W.; Fang, S.; Ling, X.; Kong, J.; Dresselhaus, M.S.; Kaxiras, E.; et al. MoS₂ Field-Effect Transistor with Sub-10 nm Channel Length. *Nano Lett.* **2016**, *16*, 7798–7806. [[CrossRef](#)]
185. Kinloch, I.A.; Suhr, J.; Lou, J.; Young, R.J.; Ajayan, P.M. Composites with carbon nanotubes and graphene: An outlook. *Science* **2018**, *362*, 547–553. [[CrossRef](#)]
186. Raychowdhury, A. MRAM and FinFETs team up. *Nat. Electron.* **2018**, *1*, 618–619. [[CrossRef](#)]
187. Liu, C.C.; Franke, E.; Mignot, Y.; Xie, R.L.; Yeung, C.W.; Zhang, J.Y.; Chi, C.; Zhang, C.; Farrell, R.; Lai, K.F.; et al. Directed self-assembly of block copolymers for 7 nanometre FinFET technology and beyond. *Nat. Electron.* **2018**, *1*, 562–569. [[CrossRef](#)]
188. Hills, G.; Bardon, M.G.; Doornbos, G.; Yakimets, D.; Schuddinck, P.; Baert, R.; Jang, D.Y.; Mattii, L.; Sherazi, S.M.Y.; Rodopoulos, D.; et al. Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI. *IEEE Trans. Nanotechnol.* **2018**, *17*, 1259–1269. [[CrossRef](#)]
189. Zhang, P.P.; Qiu, C.G.; Zhang, Z.Y.; Ding, L.; Chen, B.Y.; Peng, L.M. Performance projections for ballistic carbon nanotube FinFET at circuit level. *Nano Res.* **2016**, *9*, 1785–1794. [[CrossRef](#)]
190. Mobarakeh, M.S.; Omrani, S.; Vali, M.; Bayani, A.; Omrani, N. Theoretical logic performance estimation of Silicon, Germanium and SiGe nanowire Fin-Field Effect Transistor. *Superlattice Microstruct.* **2018**, *120*, 578–587. [[CrossRef](#)]
191. Muller, K.; Bugnicourt, E.; Latorre, M.; Jorda, M.; Sanz, Y.E.; Lagaron, J.M.; Miesbauer, O.; Bianchin, A.; Hankin, S.; Bolz, U.; et al. Review on the Processing and Properties of Polymer Nanocomposites and Nanocoatings and Their Applications in the Packaging, Automotive and Solar Energy Fields. *Nanomaterials* **2017**, *7*, 74. [[CrossRef](#)] [[PubMed](#)]
192. Altebaeumer, T.; Gotsmann, B.; Pozidis, H.; Knoll, A.; Duerig, U. Nanoscale Shape-Memory Function in Highly Cross-Linked Polymers. *Nano Lett.* **2008**, *8*, 4398–4403. [[CrossRef](#)]
193. Vettiger, P.; Cross, G.; Despont, M.; Drechsler, U.; Durig, U.; Gotsmann, B.; Haberle, W.; Lantz, M.A.; Rothuizen, H.E.; Stutz, R.; et al. The “millipede”—Nanotechnology entering data storage. *IEEE Trans. Nanotechnol.* **2002**, *1*, 39–55. [[CrossRef](#)]
194. Cho, Y.; Hong, S. Scanning probe-type data storage beyond hard disk drive and flash memory. *MRS Bull.* **2018**, *43*, 365–370. [[CrossRef](#)]
195. Srimani, T.; Hills, G.; Bishop, M.D.; Radhakrishna, U.; Zubair, A.; Park, R.S.; Stein, Y.; Palacios, T.; Antoniadis, D.; Shulaker, M.M. Negative Capacitance Carbon Nanotube FETs. *IEEE Electron Device Lett.* **2018**, *39*, 304–307. [[CrossRef](#)]
196. Lau, C.; Srimani, T.; Bishop, M.D.; Hills, G.; Shulaker, M.M. Tunable n-Type Doping of Carbon Nanotubes through Engineered Atomic Layer Deposition HfOX Films. *ACS Nano* **2018**, *12*, 10924–10931. [[CrossRef](#)] [[PubMed](#)]
197. Kanhaiya, P.S.; Hills, G.; Antoniadis, D.A.; Shulaker, M.M. DISC-FETs: Dual Independent Stacked Channel Field-Effect Transistors. *IEEE Electron Device Lett.* **2018**, *39*, 1250–1253. [[CrossRef](#)]
198. Park, R.S.; Hills, G.; Sohn, J.; Mitra, S.; Shulaker, M.M.; Wong, H.S.P. Hysteresis-Free Carbon Nanotube Field-Effect Transistors. *ACS Nano* **2017**, *11*, 4785–4791. [[CrossRef](#)] [[PubMed](#)]
199. Gielen, G.; Van Rethy, J.; Marin, J.; Shulaker, M.M.; Hills, G.; Wong, H.S.P.; Mitra, S. Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies. *IEEE Trans. Circuits Syst. I* **2016**, *63*, 577–586. [[CrossRef](#)]
200. Pitkanen, O.; Jarvinen, T.; Cheng, H.; Lorite, G.S.; Dombovari, A.; Rieppo, L.; Talapatra, S.; Duong, H.M.; Toth, G.; Juhasz, K.L.; et al. On-chip integrated vertically aligned carbon nanotube based super- and pseudocapacitors. *Sci. Rep.* **2017**, *7*, 16594. [[CrossRef](#)]
201. Hills, G.; Bankman, D.; Moons, B.; Yang, L.T.; Hillard, J.; Kahng, A.; Park, R.; Verhelst, M.; Murmann, B.; Shulaker, M.M.; et al. TRIG: Hardware Accelerator for Inference-Based Applications and Experimental Demonstration Using Carbon Nanotube FETs. In Proceedings of the 2018 55th ACM/ESDA/IEEE Design Automation Conference (DAC), San Francisco, CA, USA, 24–28 June 2018. [[CrossRef](#)]
202. Hills, G.; Zhang, J.; Shulaker, M.M.; Wei, H.; Lee, C.S.; Balasingam, A.; Wong, H.S.P.; Mitra, S. Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations. *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.* **2015**, *34*, 1082–1095. [[CrossRef](#)]

203. Cao, Q.; Han, S.J.; Penumatcha, A.V.; Frank, M.M.; Tulevski, G.S.; Tersoff, J.; Haensch, W.E. Origins and characteristics of the threshold voltage variability of quasiballistic single-walled carbon nanotube field-effect transistors. *ACS Nano* **2015**, *9*, 1936–1944. [[CrossRef](#)]
204. Wei, H.; Wang, Z.X.; Tian, X.R.; Kall, M.; Xu, H.X. Cascaded logic gates in nanophotonic plasmon networks. *Nat. Commun.* **2011**, *2*. [[CrossRef](#)]
205. Siampour, H.; Kumar, S.; Bozhevolnyi, S.I. Nanofabrication of Plasmonic Circuits Containing Single Photon Sources. *ACS Photonics* **2017**, *4*, 1879–1884. [[CrossRef](#)]
206. Lundeberg, M.B.; Gao, Y.D.; Asgari, R.; Tan, C.; Van Duppen, B.; Autore, M.; Alonso-Gonzalez, P.; Woessner, A.; Watanabe, K.; Taniguchi, T.; et al. Tuning quantum nonlocal effects in graphene plasmonics. *Science* **2017**, *357*, 187–190. [[CrossRef](#)]
207. Savage, K.J.; Hawkeye, M.M.; Esteban, R.; Borisov, A.G.; Aizpurua, J.; Baumberg, J.J. Revealing the quantum regime in tunnelling plasmonics. *Nature* **2012**, *491*, 574–577. [[CrossRef](#)] [[PubMed](#)]
208. Morton, J.J.L.; McCamey, D.R.; Eriksson, M.A.; Lyon, S.A. Embracing the quantum limit in silicon computing. *Nature* **2011**, *479*, 345–353. [[CrossRef](#)] [[PubMed](#)]
209. Wu, J.Y.; Liu, B.Y.; Peng, J.Z.; Mao, J.M.; Jiang, X.H.; Qiu, C.Y.; Tremblay, C.; Su, Y.K. On-Chip Tunable Second-Order Differential-Equation Solver Based on a Silicon Photonic Mode-Split Microresonator. *J. Lightwave Technol.* **2015**, *33*, 3542–3549. [[CrossRef](#)]
210. Polman, A. Photonic materials—Teaching silicon new tricks. *Nat. Mater.* **2002**, *1*, 10–12. [[CrossRef](#)] [[PubMed](#)]
211. Dong, P.; Kim, K.W.; Melikyan, A.; Baeyens, Y. Silicon Photonics: A Scaling Technology for Communications and Interconnects. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018.
212. Vishkin, U.; Smolyaninov, I.; Davis, C. Plasmonics and the parallel programming problem—Art no. 64770M. In Proceedings of the Silicon Photonics II, San Jose, CA, USA, 22–27 January 2007; Volume 6477. [[CrossRef](#)]
213. Lereu, A.L. Modulation—Plasmons lend a helping hand. *Nat. Photonics* **2007**, *1*, 368–369. [[CrossRef](#)]
214. Passian, A.; Lereu, A.L.; Arakawa, E.T.; Wig, A.; Thundat, T.; Ferrell, T.L. Modulation of multiple photon energies by use of surface plasmons. *Opt. Lett.* **2005**, *30*, 41–43. [[CrossRef](#)] [[PubMed](#)]
215. Passian, A.; Lereu, A.L.; Ritchie, R.H.; Meriaudeau, F.; Thundat, T.; Ferrell, T.L. Surface plasmon assisted thermal coupling of multiple photon energies. *Thin Solid Film* **2006**, *497*, 315–320. [[CrossRef](#)]
216. He, X.; Htoon, H.; Doorn, S.K.; Pernice, W.H.P.; Pyatkov, F.; Krupke, R.; Jeantet, A.; Chassagneux, Y.; Voisin, C. Carbon nanotubes as emerging quantum-light sources. *Nat. Mater.* **2018**, *17*, 663–670. [[CrossRef](#)]
217. Tans, S.J.; Verschueren, A.R.M.; Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **1998**, *393*, 49–52. [[CrossRef](#)]
218. Postma, H.W.C.; Teepen, T.; Yao, Z.; Grifoni, M.; Dekker, C. Carbon nanotube single-electron transistors at room temperature. *Science* **2001**, *293*, 76–79. [[CrossRef](#)]
219. Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **2001**, *294*, 1317–1320. [[CrossRef](#)] [[PubMed](#)]
220. Tang, X.P.; Kleinhammes, A.; Shimoda, H.; Fleming, L.; Bennoune, K.Y.; Sinha, S.; Bower, C.; Zhou, O.; Wu, Y. Electronic structures of single-walled carbon nanotubes determined by NMR. *Science* **2000**, *288*, 492–494. [[CrossRef](#)] [[PubMed](#)]
221. Hone, J.; Batlogg, B.; Benes, Z.; Johnson, A.T.; Fischer, J.E. Quantized phonon spectrum of single-wall carbon nanotubes. *Science* **2000**, *289*, 1730–1733. [[CrossRef](#)] [[PubMed](#)]
222. Zhang, H.; Liu, C.X.; Gazibegovic, S.; Xu, D.; Logan, J.A.; Wang, G.Z.; van Loo, N.; Bommer, J.D.S.; de Moor, M.W.A.; Car, D.; et al. Quantized Majorana conductance. *Nature* **2018**, *556*, 74–79. [[CrossRef](#)] [[PubMed](#)]
223. Kim, S.; Yan, R.X. Recent developments in photonic, plasmonic and hybrid nanowire waveguides. *J. Mater. Chem. C* **2018**, *6*, 11795–11816. [[CrossRef](#)]
224. Chen, Y.; Lee, C.; Lu, L.; Liu, D.; Wu, Y.K.; Feng, L.T.; Li, M.; Rockstuhl, C.; Guo, G.P.; Guo, G.C.; et al. Quantum plasmonic NOON state in a silver nanowire and its use for quantum sensing. *Optica* **2018**, *5*, 1229–1235. [[CrossRef](#)]
225. Gazibegovic, S.; Car, D.; Zhang, H.; Balk, S.C.; Logan, J.A.; de Moor, M.W.A.; Cassidy, M.C.; Schmits, R.; Xu, D.; Wang, G.Z.; et al. Epitaxy of advanced nanowire quantum devices. *Nature* **2017**, *548*, 434–438. [[CrossRef](#)]

226. Petersson, K.D.; McFaul, L.W.; Schroer, M.D.; Jung, M.; Taylor, J.M.; Houck, A.A.; Petta, J.R. Circuit quantum electrodynamics with a spin qubit. *Nature* **2012**, *490*, 380–383. [[CrossRef](#)]
227. Nadj-Perge, S.; Frollov, S.M.; Bakkers, E.P.A.M.; Kouwenhoven, L.P. Spin-orbit qubit in a semiconductor nanowire. *Nature* **2010**, *468*, 1084–1087. [[CrossRef](#)]
228. Buonacorsi, B.; Cai, Z.Y.; Ramirez, E.B.; Willick, K.S.; Walker, S.M.; Li, J.H.; Shaw, B.D.; Xu, X.S.; Benjamin, S.C.; Baugh, J. Network architecture for a topological quantum computer in silicon. *Quantum Sci. Technol.* **2019**, *4*. [[CrossRef](#)]
229. Zhang, X.; Li, H.O.; Wang, K.; Cao, G.; Xiao, M.; Guo, G.P. Qubits based on semiconductor quantum dots. *Chin. Phys. B* **2018**, *27*. [[CrossRef](#)]
230. Watson, T.F.; Philips, S.G.J.; Kawakami, E.; Ward, D.R.; Scarlino, P.; Veldhorst, M.; Savage, D.E.; Lagally, M.G.; Friesen, M.; Coppersmith, S.N.; et al. A programmable two-qubit quantum processor in silicon. *Nature* **2018**, *555*, 633–637. [[CrossRef](#)] [[PubMed](#)]
231. Kim, J.H.; Aghaeimeibodi, S.; Richardson, C.J.K.; Leavitt, R.P.; Waks, E. Super-Radiant Emission from Quantum Dots in a Nanophotonic Waveguide. *Nano Lett.* **2018**, *18*, 4734–4740. [[CrossRef](#)] [[PubMed](#)]
232. Fogarty, M.A.; Chan, K.W.; Hensen, B.; Huang, W.; Tantt, T.; Yang, C.H.; Laucht, A.; Veldhorst, M.; Hudson, F.E.; Itoh, K.M.; et al. Integrated silicon qubit platform with single-spin addressability, exchange control and single-shot singlet-triplet readout. *Nat. Commun.* **2018**, *9*. [[CrossRef](#)] [[PubMed](#)]
233. Wu, X.F.; Jiang, P.; Razinskas, G.; Huo, Y.H.; Zhang, H.Y.; Kamp, M.; Rastelli, A.; Schmidt, O.G.; Hecht, B.; Lindfors, K.; et al. On-Chip Single-Plasmon Nanocircuit Driven by a Self-Assembled Quantum Dot. *Nano Lett.* **2017**, *17*, 4291–4296. [[CrossRef](#)] [[PubMed](#)]
234. Veldhorst, M.; Eenink, H.G.J.; Yang, C.H.; Dzurak, A.S. Silicon CMOS architecture for a spin-based quantum computer. *Nat. Commun.* **2017**, *8*. [[CrossRef](#)]
235. Veldhorst, M.; Yang, C.H.; Hwang, J.C.C.; Huang, W.; Dehollain, J.P.; Muhonen, J.T.; Simmons, S.; Laucht, A.; Hudson, F.E.; Itoh, K.M.; et al. A two-qubit logic gate in silicon. *Nature* **2015**, *526*, 410–414. [[CrossRef](#)]
236. Zu, C.; Wang, W.B.; He, L.; Zhang, W.G.; Dai, C.Y.; Wang, F.; Duan, L.M. Experimental realization of universal geometric quantum gates with solid-state spins. *Nature* **2014**, *514*, 72–75. [[CrossRef](#)]
237. Hemmer, P.; Lukin, M. Room-temperature solid-state quantum processors in diamond. In Proceedings of the Quantum Information and Computation VI, Orlando, FL, USA, 19–20 March 2008; Volume 6976. [[CrossRef](#)]
238. Cirac, J.I.; Zoller, P. A scalable quantum computer with ions in an array of microtraps. *Nature* **2000**, *404*, 579–581. [[CrossRef](#)]
239. Faraji-Dana, M.; Arbabi, E.; Arbabi, A.; Kamali, S.M.; Kwon, H.; Faraon, A. Compact folded metasurface spectrometer. *Nat. Commun.* **2018**, *9*. [[CrossRef](#)]
240. Babashah, H.; Kavehvas, Z.; Koochi, S.; Khavasi, A. Integration in analog optical computing using metasurfaces revisited: Toward ideal optical integration. *J. Opt. Soc. Am. B* **2017**, *34*, 1270–1279. [[CrossRef](#)]
241. Achouri, K.; Lavigne, G.; Salem, M.A.; Caloz, C. Metasurface Spatial Processor for Electromagnetic Remote Control. *IEEE Trans. Antennas Propag.* **2016**, *64*, 1759–1767. [[CrossRef](#)]
242. Lu, L.; Joannopoulos, J.D.; Soljacic, M. Topological photonics. *Nat. Photonics* **2014**, *8*, 821–829. [[CrossRef](#)]
243. Friedman, R.S.; McAlpine, M.C.; Ricketts, D.S.; Ham, D.; Lieber, C.M. High-speed integrated nanowire circuits. *Nature* **2005**, *434*, 1085. [[CrossRef](#)] [[PubMed](#)]
244. Wang, R.X.; Xia, H.Y.; Zhang, D.G.; Chen, J.X.; Zhu, L.F.; Wang, Y.; Yang, E.C.; Zang, T.Y.; Wen, X.L.; Zou, G.; et al. Bloch surface waves confined in one dimension with a single polymeric nanofibre. *Nat. Commun.* **2017**, *8*. [[CrossRef](#)]
245. Tans, S.J.; Dekker, C. Molecular transistors—Potential modulations along carbon nanotubes. *Nature* **2000**, *404*, 834–835. [[CrossRef](#)]
246. Park, R.S.; Shulaker, M.M.; Hills, G.; Liyanage, L.S.; Lee, S.; Tang, A.; Mitra, S.; Wong, H.S.P. Hysteresis in Carbon Nanotube Transistors: Measurement and Analysis of Trap Density, Energy Level, and Spatial Distribution. *ACS Nano* **2016**, *10*, 4599–4608. [[CrossRef](#)]
247. Cao, Q.; Kim, H.S.; Pimparkar, N.; Kulkarni, J.P.; Wang, C.J.; Shim, M.; Roy, K.; Alam, M.A.; Rogers, J.A. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **2008**, *454*, 495–500. [[CrossRef](#)]
248. Yamamoto, T.; Watanabe, K.; Hernandez, E.R. Mechanical properties, thermal stability and heat transport in carbon nanotubes. *Top. Appl. Phys.* **2008**, *111*, 165–194.

249. Zhang, S.; Kang, L.; Wang, X.; Tong, L.; Yang, L.; Wang, Z.; Qi, K.; Deng, S.; Li, Q.; Bai, X.; et al. Arrays of horizontal carbon nanotubes of controlled chirality grown using designed catalysts. *Nature* **2017**, *543*, 234–238. [[CrossRef](#)]
250. Shulaker, M.M.; Hills, G.; Park, R.S.; Howe, R.T.; Saraswat, K.; Wong, H.S.P.; Mitra, S. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. *Nature* **2017**, *547*, 74–78. [[CrossRef](#)] [[PubMed](#)]
251. Gielen, G.; Van Rethy, J.; Shulaker, M.M.; Hills, G.; Wong, H.S.P.; Mitra, S. Time-Based Sensor Interface Circuits in Carbon Nanotube Technology. In Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 24–27 May 2015; pp. 2924–2927.
252. McCoy, M. Nantero to move nanotubes into computer chips. *Chem. Eng. News Arch.* **2004**, *82*, 14. [[CrossRef](#)]
253. Wolf, L. The Nanotube Computer Debuts. *Chem. Eng. News Arch.* **2013**, *91*, 7.
254. Winkless, L. Carbon nanotube computer becomes reality. *Mater. Today* **2013**, *16*, 415–416. [[CrossRef](#)]
255. Welter, K. The First Carbon Nanotube Computer. *ChemPhysChem* **2013**, *14*, 3439.
256. Wei, H.; Shulaker, M.; Wong, H.S.P.; Mitra, S. Monolithic Three-Dimensional Integration of Carbon Nanotube FET Complementary Logic Circuits. In Proceedings of the 2013 IEEE International Electron Devices Meeting (IEDM), Honolulu, HI, USA, 9–12 June 2013.
257. Wei, H.; Shulaker, M.; Hills, G.; Chen, H.Y.; Lee, C.S.; Liyanage, L.; Zhang, J.; Wong, H.S.P.; Mitra, S. Carbon Nanotube Circuits: Opportunities and Challenges. In Proceedings of the Conference on Design, Automation and Test in Europe, Grenoble, France, 18–22 March 2013; pp. 619–624.
258. Talbot, D. Nanotube Computers. *Technol. Rev.* **2013**, *116*, 84–86.
259. Shulaker, M.M.; Hills, G.; Patil, N.; Wei, H.; Chen, H.Y.; PhilipWong, H.S.; Mitra, S. Carbon nanotube computer. *Nature* **2013**, *501*, 526–530. [[CrossRef](#)]
260. Shulaker, M.; Van Rethy, J.; Hills, G.; Chen, H.Y.; Gielen, G.; Wong, H.S.P.; Mitra, S. Experimental Demonstration of a Fully Digital Capacitive Sensor Interface Built Entirely Using Carbon-Nanotube FETs. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; Volume 56, pp. 112–113.
261. Shulaker, M.; Van Rethy, J.; Hills, G.; Chen, H.Y.; Gielen, G.; Wong, H.S.P.; Mitra, S. Sacha: The Stanford Carbon Nanotube Controlled Handshaking Robot. In Proceedings of the 50th Annual Design Automation Conference, Austin, TX, USA, 29 May–7 June 2013.
262. Sealy, C. Scientists switch on first carbon nanotube computer. *Nano Today* **2013**, *8*, 555–556. [[CrossRef](#)]
263. Kreupl, F. ELECTRONICS The carbon-nanotube computer has arrived. *Nature* **2013**, *501*, 495–496. [[CrossRef](#)]
264. Garber, L. Researchers Build First Carbon-Nanotube Computer. *Computer* **2013**, *46*, 21–22.
265. Wong, H.S.P.; Mitra, S.; Akinwande, D.; Beasley, C.; Chai, Y.; Chen, H.Y.; Chen, X.Y.; Close, G.; Deng, J.; Hazeghi, A.; et al. Carbon Nanotube Electronics—Materials, Devices, Circuits, Design, Modeling, and Performance Projection. In Proceedings of the 2011 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 5–7 December 2011.
266. Wei, H.; Zhang, J.; Wei, L.; Patil, N.; Lin, A.; Shulaker, M.M.; Chen, H.Y.; Wong, H.S.P.; Mitra, S. Carbon Nanotube Imperfection-Immune Digital VLSI: Frequently Asked Questions Updated Invited Paper. In Proceedings of the International Conference on Computer-Aided Design, San Jose, CA, USA, 7–10 November 2011; pp. 227–230.
267. Faster nanotube transistors can speed computers. *Intech* **2004**, *51*, 6–18.
268. Chen, Z.H.; Appenzeller, J.; Lin, Y.M.; Sippel-Oakley, J.; Rinzler, A.G.; Tang, J.Y.; Wind, S.J.; Solomon, P.M.; Avouris, P. An integrated logic circuit assembled on a single carbon nanotube. *Science* **2006**, *311*, 1735. [[CrossRef](#)] [[PubMed](#)]
269. Sandha, K.S.; Thakur, A. Comparative Analysis of Mixed CNTs and MWCNTs as VLSI Interconnects for Deep Sub-micron Technology Nodes. *J. Electron. Mater.* **2019**, *48*, 2543–2554. [[CrossRef](#)]
270. Dale, M.; Miller, J.F.; Stepney, S.; Trefzer, M.A. Evolving Carbon Nanotube Reservoir Computers. *Lect. Notes Comput. Sci.* **2016**, *9726*, 49–61. [[CrossRef](#)]
271. Tanaka, G.; Yamane, T.; Héroux, J.B.; Nakane, R.; Kanazawa, N.; Takeda, S.; Numata, H.; Nakano, D.; Hirose, A. Recent advances in physical reservoir computing: A review. *Neural Netw.* **2019**, *115*, 100–123. [[CrossRef](#)] [[PubMed](#)]
272. Ouyang, M.; Huang, J.L.; Cheung, C.L.; Lieber, C.M. Energy gaps in “metallic” single-walled carbon nanotubes. *Science* **2001**, *292*, 702–705. [[CrossRef](#)]

273. Hou, Q.W.; Cao, B.Y.; Guo, Z.Y. Thermal conductivity of carbon nanotube: From ballistic to diffusive transport. *Acta Phys. Sin.* **2009**, *58*, 7809–7814.
274. Donadio, D.; Galli, G. Thermal Conductivity of Isolated and Interacting Carbon Nanotubes: Comparing Results from Molecular Dynamics and the Boltzmann Transport Equation. *Phys. Rev. Lett.* **2007**, *99*, 255502. [[CrossRef](#)]
275. Ilani, S.; McEuen, P.L. Electron Transport in Carbon Nanotubes. *Annu. Rev. Condens. Matter Phys.* **2010**, *1*, 1–25. [[CrossRef](#)]
276. Chiodarelli, N.; Fournier, A.; Dijon, J. Impact of the contact's geometry on the line resistivity of carbon nanotubes bundles for applications as horizontal interconnects. *Appl. Phys. Lett.* **2013**, *103*. [[CrossRef](#)]
277. Chiodarelli, N.; Masahito, S.; Kashiwagi, Y.; Li, Y.L.; Arstila, K.; Richard, O.; Cott, D.J.; Heyns, M.; De Gendt, S.; Groeseneken, G.; et al. Measuring the electrical resistivity and contact resistance of vertical carbon nanotube bundles for application as interconnects. *Nanotechnology* **2011**, *22*. [[CrossRef](#)] [[PubMed](#)]
278. Bandaru, P.R. Electrical properties and applications of carbon nanotube structures. *J. Nanosci. Nanotechnol.* **2007**, *7*, 1239–1267. [[CrossRef](#)] [[PubMed](#)]
279. Sfeir, M.Y.; Beetz, T.; Wang, F.; Huang, L.M.; Huang, X.M.H.; Huang, M.Y.; Hone, J.; O'Brien, S.; Misewich, J.A.; Heinz, T.F.; et al. Optical spectroscopy of individual single-walled carbon nanotubes of defined chiral structure. *Science* **2006**, *312*, 554–556. [[CrossRef](#)] [[PubMed](#)]
280. Lee, J.; Stein, I.Y.; Devoe, M.E.; Lewis, D.J.; Lachman, N.; Kessler, S.S.; Buschhorn, S.T.; Wardle, B.L. Impact of carbon nanotube length on electron transport in aligned carbon nanotube networks. *Appl. Phys. Lett.* **2015**, *106*. [[CrossRef](#)]
281. Pyatkov, F.; Futterling, V.; Khasminskaya, S.; Flavel, B.S.; Hennrich, F.; Kappes, M.M.; Krupke, R.; Pernice, W.H.P. Cavity-enhanced light emission from electrically driven carbon nanotubes. *Nat. Photonics* **2016**, *10*, 420–427. [[CrossRef](#)]
282. Xu, J.L.; Dai, R.X.; Xin, Y.; Sun, Y.L.; Li, X.; Yu, Y.X.; Xiang, L.; Xie, D.; Wang, S.D.; Ren, T.L. Efficient and Reversible Electron Doping of Semiconductor-Enriched Single-Walled Carbon Nanotubes by Using Decamethylcobaltocene. *Sci. Rep.* **2017**, *7*. [[CrossRef](#)] [[PubMed](#)]
283. Srimani, T.; Hills, G.; Bishop, M.D.; Shulaker, M.M. 30-nm Contacted Gate Pitch Back-Gate Carbon Nanotube FETs for Sub-3-nm Nodes. *IEEE Trans. Nanotechnol.* **2019**, *18*, 132–138. [[CrossRef](#)]
284. Shulaker, M.M.; Wu, T.F.; Pal, A.; Zhao, L.; Nishi, Y.; Saraswat, K.; Wong, H.S.P.; Mitra, S. Monolithic 3D Integration of Logic and Memory: Carbon Nanotube FETs, Resistive RAM, and Silicon FETs. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014.
285. Shulaker, M.M.; Van Rethy, J.; Wu, T.F.; Liyanage, L.S.; Wei, H.; Li, Z.Y.; Pop, E.; Gielen, G.; Wong, H.S.P.; Mitra, S. Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. *ACS Nano* **2014**, *8*, 3434–3443. [[CrossRef](#)]
286. Shulaker, M.M.; Van Rethy, J.; Hills, G.; Wei, H.; Chen, H.Y.; Gielen, G.; Wong, H.S.P.; Mitra, S. Sensor-to-Digital Interface Built Entirely with Carbon Nanotube FETs. *IEEE J. Solid-State Circuits* **2014**, *49*, 190–201. [[CrossRef](#)]
287. Shulaker, M.M.; Saraswat, K.; Wong, H.S.P.; Mitra, S. Monolithic Three-Dimensional Integration of Carbon Nanotube FETs with Silicon CMOS. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014.
288. Shulaker, M.M.; Pitner, G.; Hills, G.; Giachino, M.; Wong, H.S.P.; Mitra, S. High-Performance Carbon Nanotube Field-Effect Transistors. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014.
289. Shulaker, M.; Hills, G.; Wei, H.; Chen, H.Y.; Patil, N.; Wong, H.S.P.; Mitra, S. Advancements With Carbon Nanotube Digital Systems. In Proceedings of the 2014 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC), San Jose, CA, USA, 20–23 May 2014; pp. 319–321.
290. Hills, G.; Shulaker, M.; Wei, H.; Chen, H.Y.; Wong, H.S.P.; Mitra, S. Robust Design and Experimental Demonstrations of Carbon Nanotube Digital Circuits. In Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, San Jose, CA, USA, 15–17 September 2014.
291. Keren, K.; Berman, R.S.; Buchstab, E.; Sivan, U.; Braun, E. DNA-templated carbon nanotube field-effect transistor. *Science* **2003**, *302*, 1380–1382. [[CrossRef](#)]
292. Carbon nanotube computers. *Technol. Rev.* **2006**, *109*, 92.

293. Jacoby, M. ACS meeting—Carbon nanotube computer circuits—Novel processing and microfabrication lead to first single-molecule logic gate. *Chem. Eng. News* **2001**, *79*, 9. [CrossRef]
294. Jarillo-Herrero, P.; van Dam, J.A.; Kouwenhoven, L.P. Quantum supercurrent transistors in carbon nanotubes. *Nature* **2006**, *439*, 953–956. [CrossRef] [PubMed]
295. Colwell, R.P. How we made the Pentium processors. *Nat. Electron.* **2019**, *2*, 83–84. [CrossRef]
296. Qiu, C.G.; Zhang, Z.Y.; Xiao, M.M.; Yang, Y.J.; Zhong, D.L.; Peng, L.M. Scaling carbon nanotube complementary transistors to 5-nm gate lengths. *Science* **2017**, *355*, 271–276. [CrossRef] [PubMed]
297. Franklin, A.D. ELECTRONICS The road to carbon nanotube transistors. *Nature* **2013**, *498*, 443–444. [CrossRef] [PubMed]
298. LeMieux, M.C.; Roberts, M.; Barman, S.; Jin, Y.W.; Kim, J.M.; Bao, Z.N. Self-sorted, aligned nanotube networks for thin-film transistors. *Science* **2008**, *321*, 101–104. [CrossRef] [PubMed]
299. Kanungo, M.; Lu, H.; Malliaras, G.G.; Blanchet, G.B. Suppression of Metallic Conductivity of Single-Walled Carbon Nanotubes by Cycloaddition Reactions. *Science* **2009**, *323*, 234–237. [CrossRef] [PubMed]
300. Jin, S.H.; Dunham, S.N.; Song, J.Z.; Xie, X.; Kim, J.H.; Lu, C.F.; Islam, A.; Du, F.; Kim, J.; Felts, J.; et al. Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes. *Nat. Nanotechnol.* **2013**, *8*, 347–355. [CrossRef]
301. Park, H.; Afzali, A.; Han, S.J.; Tulevski, G.S.; Franklin, A.D.; Tersoff, J.; Hannon, J.B.; Haensch, W. High-density integration of carbon nanotubes via chemical self-assembly. *Nat. Nanotechnol.* **2012**, *7*, 787–791. [CrossRef]
302. Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H.J. Ballistic carbon nanotube field-effect transistors. *Nature* **2003**, *424*, 654–657. [CrossRef] [PubMed]
303. Odom, T.W.; Huang, J.L.; Kim, P.; Lieber, C.M. Atomic structure and electronic properties of single-walled carbon nanotubes. *Nature* **1998**, *391*, 62–64. [CrossRef]
304. International Technology Roadmap for Semiconductors 2.0 2015 Edition. 2015. Available online: www.itrs2.net/itrs-reports.html (accessed on 15 June 2019).
305. Cao, Q.; Tersoff, J.; Farmer, D.B.; Zhu, Y.; Han, S.-J. Carbon nanotube transistors scaled to a 40-nanometer footprint. *Science* **2017**, *356*, 1369–1372. [CrossRef] [PubMed]
306. Vandenberghe, W. Two-dimensional Topological Insulator Transistors as Energy Efficient Switches Robust against Material and Device Imperfections. In Proceedings of the 2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S), Berkeley, CA, USA, 19–20 October 2017.
307. Vandenberghe, W.G.; Fischetti, M.V. Imperfect two-dimensional topological insulator field-effect transistors. *Nat. Commun.* **2017**, *8*, 14184. [CrossRef] [PubMed]
308. Bradlyn, B.; Elcoro, L.; Cano, J.; Vergniory, M.G.; Wang, Z.; Felser, C.; Aroyo, M.I.; Bernevig, B.A. Topological quantum chemistry. *Nature* **2017**, *547*, 298–305. [CrossRef] [PubMed]
309. Ginley, T.; Wang, Y.; Wang, Z.; Law, S. Dirac plasmons and beyond: The past, present, and future of plasmonics in 3D topological insulators. *MRS Commun.* **2018**, *8*, 782–794. [CrossRef]
310. Okuyama, R.; Izumida, W.; Eto, M. Topological classification of the single-wall carbon nanotube. *Phys. Rev. B* **2019**, *99*. [CrossRef]
311. Pelzman, C.; Chanover, N.; Voelz, D.; Cho, S.Y. Plasmonic device for spectral analysis. *Electron. Lett.* **2019**, *55*, 142–143. [CrossRef]
312. Liu, Z.H.; Ding, L.Z.; Yi, J.P.; Wei, Z.C.; Guo, J.P. Design of a multi-bits input optical logic device with high intensity contrast based on plasmonic waveguides structure. *Opt. Commun.* **2019**, *430*, 112–118. [CrossRef]
313. Ciminelli, C.; Dell’Olio, F.; Conteduca, D.; Armenise, M.N. Integrated Photonic and Plasmonic Resonant Devices for Label-Free Biosensing and Trapping at the Nanoscale. *Phys. Status Solidi A* **2019**, *216*. [CrossRef]
314. Yan, H.G.; Li, X.S.; Chandra, B.; Tulevski, G.; Wu, Y.Q.; Freitag, M.; Zhu, W.J.; Avouris, P.; Xia, F.N. Tunable infrared plasmonic devices using graphene/insulator stacks. *Nat. Nanotechnol.* **2012**, *7*, 330–334. [CrossRef]
315. Zhao, W.J.; Qi, J.W.; Lu, Y.; Wang, R.D.; Zhang, Q.; Xiong, H.; Zhang, Y.Q.; Wu, Q.; Xu, J.J. On-chip plasmon-induced transparency in THz metamaterial on a LiNbO₃ subwavelength planar waveguide. *Opt. Express* **2019**, *27*, 7373–7383. [CrossRef] [PubMed]
316. Welser, J.; Pitera, J.W.; Goldberg, C. Future Computing Hardware for AI. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018.
317. Lu, C.C.; Hu, X.Y.; Yang, H.; Gong, Q.H. Integrated all-optical logic discriminators based on plasmonic bandgap engineering. *Sci. Rep.* **2013**, *3*. [CrossRef] [PubMed]

318. Llatser, I.; Abadal, S.; Sugranes, A.M.; Cabellos-Aparicio, A.; Alarcon, E. Graphene-enabled Wireless Networks-on-Chip. In Proceedings of the 2013 First International Black Sea Conference on Communications and Networking (BlackSeaCom), Batumi, Georgia, 3–5 July 2013; pp. 69–73.
319. Lin, Y.M.; Valdes-Garcia, A.; Han, S.J.; Farmer, D.B.; Meric, I.; Sun, Y.N.; Wu, Y.Q.; Dimitrakopoulos, C.; Grill, A.; Avouris, P.; et al. Wafer-Scale Graphene Integrated Circuit. *Science* **2011**, *332*, 1294–1297. [[CrossRef](#)] [[PubMed](#)]
320. Ni, G.X.; McLeod, A.S.; Sun, Z.; Wang, L.; Xiong, L.; Post, K.W.; Sunku, S.S.; Jiang, B.Y.; Hone, J.; Dean, C.R.; et al. Fundamental limits to graphene plasmonics. *Nature* **2018**, *557*, 530–533. [[CrossRef](#)] [[PubMed](#)]
321. Yablonovitch, E. Photonic crystals—Towards rational material design. *Nat. Mater.* **2003**, *2*, 648–649. [[CrossRef](#)]
322. Stutzer, S.; Plotnik, Y.; Lumer, Y.; Titum, P.; Lindner, N.H.; Segev, M.; Rechtsman, M.C.; Szameit, A. Photonic topological Anderson insulators. *Nature* **2018**, *560*, 461–465. [[CrossRef](#)]
323. Lustig, E.; Weimann, S.; Plotnik, Y.; Lumer, Y.; Bandres, M.A.; Szameit, A.; Segev, M. Photonic topological insulator in synthetic dimensions. *Nature* **2019**. [[CrossRef](#)]
324. Basov, D.N.; Averitt, R.D.; Hsieh, D. Towards properties on demand in quantum materials. *Nat. Mater.* **2017**, *16*, 1077–1088. [[CrossRef](#)]
325. Zhu, T.; Zhou, Y.; Lou, Y.; Ye, H.; Qiu, M.; Ruan, Z.; Fan, S. Plasmonic computing of spatial differentiation. *Nat. Commun.* **2017**, *8*, 15391. [[CrossRef](#)]
326. Calva, P.A.; Medina, I. Power Breakdown Threshold of a Plasmonic Waveguide Filter. *Plasmonics* **2014**, *9*, 561–564. [[CrossRef](#)]
327. Marpaung, D.; Yao, J.P.; Capmany, J. Integrated microwave photonics. *Nat. Photonics* **2019**, *13*, 80–90. [[CrossRef](#)]
328. Yang, J.Y.; Zhao, Y.; Qiu, C.; Wang, W.J.; Jiang, G.M.; Hao, Y.L.; Jiang, X.Q. Study of Silicon Photonics Based on Standard CMOS Foundry. In Proceedings of the Optoelectronic Devices and Integration III, Beijing, China, 18–20 October 2010; Volume 7847. [[CrossRef](#)]
329. Orcutt, J.S.; Khilo, A.; Holzwarth, C.W.; Popovic, M.A.; Li, H.Q.; Sun, J.; Bonifield, T.; Hollingsworth, R.; Kartner, F.X.; Smith, H.I.; et al. Nanophotonic integration in state-of-the-art CMOS foundries. *Opt. Express* **2011**, *19*, 2335–2346. [[CrossRef](#)] [[PubMed](#)]
330. Atabaki, A.H.; Moazeni, S.; Pavanello, F.; Gevorgyan, H.; Notaros, J.; Alloatti, L.; Wade, M.T.; Sun, C.; Kruger, S.A.; Meng, H.Y.; et al. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature* **2018**, *556*, 349–354. [[CrossRef](#)] [[PubMed](#)]
331. Popovic, M.A.; Wade, M.T.; Oreutt, J.S.; Shainline, J.M.; Sun, C.; Georgas, M.; Moss, B.; Kumar, E.; Alloatti, L.; Pavanello, F.; et al. Monolithic Silicon Photonics in a Sub-100nm SOI CMOS Microprocessor Foundry: Progress from Devices to Systems. In Proceedings of the Silicon Photonics X, San Francisco, CA, USA, 9–12 February 2015; Volume 9367. [[CrossRef](#)]
332. Liu, Y.S. Pioneering Research in VCSEL-Based Parallel Optical Interconnect Technology for Today's Data Centers. *Nonlinear Opt. Quantum Opt.* **2019**, *50*, 217–226.
333. Cheng, Q.X.; Bahadori, M.; Glick, M.; Rumley, S.; Bergman, K. Recent advances in optical technologies for data centers: A review. *Optica* **2018**, *5*, 1354–1370. [[CrossRef](#)]
334. Alexoudi, T.; Terzenidis, N.; Pitris, S.; Moralís-Pegios, M.; Maniotis, P.; Vagionas, C.; Mitsolidou, C.; Mourgias-Alexandris, G.; Kanellos, G.T.; Miliou, A.; et al. Optics in Computing: From Photonic Network-on-Chip to Chip-to-Chip Interconnects and Disintegrated Architectures. *J. Lightwave Technol.* **2019**, *37*, 363–379. [[CrossRef](#)]
335. Moaied, M.; Palomba, S.; Ostrikov, K. Quantum plasmonics: Longitudinal quantum plasmons in copper, gold, and silver. *J. Opt.* **2017**, *19*. [[CrossRef](#)]
336. Bozhevolnyi, S.I.; Khurgin, J.B. The case for quantum plasmonics. *Nat. Photonics* **2017**, *11*, 398–400. [[CrossRef](#)]
337. Nechepurenko, I.A.; Dorofeenko, A.V.; Vinogradov, A.P.; Nikitov, S.A. Passively Q-switched Spaser as a Terahertz Clock Oscillator for Plasmon Computer. *J. Commun. Technol. Electron.* **2017**, *62*, 1209–1215. [[CrossRef](#)]
338. Saiki, T. Switching of localized surface plasmon resonance of gold nanoparticles using phase-change materials and implementation of computing functionality. *Appl. Phys. A Mater.* **2017**, *123*. [[CrossRef](#)]

339. Morsy-Osman, M.; Plant, D.V. A Comparative Study of Technology Options for Next Generation Intra- and Inter-datacenter Interconnects. In Proceedings of the 2018 Optical Fiber Communications Conference and Exposition (OFC), San Diego, CA, USA, 11–15 March 2018.
340. Thraskias, C.A.; Lallas, E.N.; Neumann, N.; Schares, L.; Offrein, B.J.; Henker, R.; Plettemeier, D.; Ellinger, F.; Leuthold, J.; Tomkos, I. Survey of Photonic and Plasmonic Interconnect Technologies for Intra-Datacenter and High-Performance Computing Communications. *IEEE Commun. Surv. Tutor.* **2018**, *20*, 2758–2783. [[CrossRef](#)]
341. Lereu, A.L.; Farahi, R.H.; Tetard, L.; Enoch, S.; Thundat, T.; Passian, A. Plasmon assisted thermal modulation in nanoparticles. *Opt. Express* **2013**, *21*, 12145–12158. [[CrossRef](#)] [[PubMed](#)]
342. Lereu, A.L.; Passian, A.; Farahi, R.H.; van Hulst, N.F.; Ferrell, T.L.; Thundat, T. Thermoplasmonic shift and dispersion in thin metal films. *J. Vac. Sci. Technol. A* **2008**, *26*, 836–841. [[CrossRef](#)]
343. Zipkes, C.; Palzer, S.; Sias, C.; Kohl, M. A trapped single ion inside a Bose-Einstein condensate. *Nature* **2010**, *464*, 388–391. [[CrossRef](#)] [[PubMed](#)]
344. Abadillo-Uriel, J.C.; Koiller, B.; Calderon, M.J. Two-dimensional semiconductors pave the way towards dopant-based quantum computing. *Beilstein J. Nanotechnol.* **2018**, *9*, 2668–2673. [[CrossRef](#)] [[PubMed](#)]
345. Brandenburg, F.; Nagumo, R.; Saichi, K.; Tahara, K.; Iwasaki, T.; Hatano, M.; Jelezko, F.; Igarashi, R.; Yatsui, T. Improving the electron spin properties of nitrogen-vacancy centres in nanodiamonds by near-field etching. *Sci. Rep.* **2018**, *8*, 15847. [[CrossRef](#)]
346. Dunjko, V.; Briegel, H.J. Machine learning & artificial intelligence in the quantum domain: A review of recent progress. *Rep. Prog. Phys.* **2018**, *81*, 074001. [[CrossRef](#)]
347. Kimble, H.J. The quantum internet. *Nature* **2008**, *453*, 1023–1030. [[CrossRef](#)]
348. Layden, D.; Zhou, S.; Cappellaro, P.; Jiang, L. Ancilla-Free Quantum Error Correction Codes for Quantum Metrology. *Phys. Rev. Lett.* **2019**, *122*. [[CrossRef](#)]
349. Ren, J.G.; Xu, P.; Yong, H.L.; Zhang, L.; Liao, S.K.; Yin, J.; Liu, W.Y.; Cai, W.Q.; Yang, M.; Li, L.; et al. Ground-to-satellite quantum teleportation. *Nature* **2017**, *549*, 70–73. [[CrossRef](#)] [[PubMed](#)]
350. Liao, S.K.; Cai, W.Q.; Liu, W.Y.; Zhang, L.; Li, Y.; Ren, J.G.; Yin, J.; Shen, Q.; Cao, Y.; Li, Z.P.; et al. Satellite-to-ground quantum key distribution. *Nature* **2017**, *549*, 43–47. [[CrossRef](#)] [[PubMed](#)]
351. Zhuang, Q.T.; Zhang, Z.S.; Shapiro, J.H. Distributed quantum sensing using continuous-variable multipartite entanglement. *Phys. Rev. A* **2018**, *97*. [[CrossRef](#)]
352. Fernandez-Carames, T.M.; Fraga-Lamas, P.; Suarez-Albela, M.; Diaz-Bouza, M.A. A Fog Computing Based Cyber-Physical System for the Automation of Pipe-Related Tasks in the Industry 4.0 Shipyard. *Sensors* **2018**, *18*, 1961. [[CrossRef](#)] [[PubMed](#)]
353. Yan, L.; Cao, S.; Gong, Y.; Han, H.; Wei, J.; Zhao, Y.; Yang, S. SatEC: A 5G Satellite Edge Computing Framework Based on Microservice Architecture. *Sensors* **2019**, *19*, 831. [[CrossRef](#)] [[PubMed](#)]
354. Cheng, Z.; Rios, C.; Pernice, W.H.P.; Wright, C.D.; Bhaskaran, H. On-chip photonic synapse. *Sci. Adv.* **2017**, *3*, e1700160. [[CrossRef](#)]
355. Olshausen, B.A.; Rozell, C.J. Neuromorphic computation sparse codes from memristor grids. *Nat. Nanotechnol.* **2017**, *12*, 722–723. [[CrossRef](#)]
356. Watson, A. Neuromorphic engineering—Why can't a computer be more like a brain. *Science* **1997**, *277*, 1934–1936. [[CrossRef](#)]
357. Boybat, I.; Le Gallo, M.; Nandakumar, S.R.; Moraitis, T.; Parnell, T.; Tuma, T.; Rajendran, B.; Leblebici, Y.; Sebastian, A.; Eleftheriou, E. Neuromorphic computing with multi-memristive synapses. *Nat. Commun.* **2018**, *9*. [[CrossRef](#)]
358. Van de Burgt, Y.; Melianas, A.; Keene, S.T.; Malliaras, G.; Salleo, A. Organic electronics for neuromorphic computing. *Nat. Electron.* **2018**, *1*, 386–397. [[CrossRef](#)]
359. Indiveri, G.; Douglas, F. Robotic vision—Neuromorphic vision sensors. *Science* **2000**, *288*, 1189–1190. [[CrossRef](#)]
360. Neftci, E.; Binas, J.; Rutishauser, U.; Chicca, E.; Indiveri, G.; Douglas, R.J. Synthesizing cognition in neuromorphic electronic systems. *Proc. Natl. Acad. Sci. USA* **2013**, *110*, E3468–E3476. [[CrossRef](#)] [[PubMed](#)]
361. Prezioso, M.; Merrih-Bayat, F.; Hoskins, B.D.; Adam, G.C.; Likharev, K.K.; Strukov, D.B. Training and operation of an integrated neuromorphic network based on metal-oxide memristors. *Nature* **2015**, *521*, 61–64. [[CrossRef](#)] [[PubMed](#)]

362. Esser, S.K.; Merolla, P.A.; Arthur, J.V.; Cassidy, A.S.; Appuswamy, R.; Andreopoulos, A.; Berg, D.J.; McKinstry, J.L.; Melano, T.; Barch, D.R.; et al. Convolutional networks for fast, energy-efficient neuromorphic computing. *Proc. Natl. Acad. Sci. USA* **2016**, *113*, 11441–11446. [[CrossRef](#)] [[PubMed](#)]
363. Buckley, S.M.; Chiles, J.; McCaughan, A.N.; Mirin, R.P.; Nam, S.W.; Shainline, J.M. Photonic interconnect with superconducting electronics for large-scale neuromorphic computing (Invited Paper). In Proceedings of the 2017 IEEE Photonics Society Summer Topical Meeting Series (Sum), San Juan, PR, USA, 10–12 July 2017; pp. 51–52.
364. Choi, S.; Tan, S.H.; Li, Z.F.; Kim, Y.; Choi, C.; Chen, P.Y.; Yeon, H.; Yu, S.M.; Kim, J. SiGe epitaxial memory for neuromorphic computing with reproducible high performance based on engineered dislocations. *Nat. Mater.* **2018**, *17*, 335–340. [[CrossRef](#)] [[PubMed](#)]
365. Sarkar, D.; Tao, J.; Wang, W.; Lin, Q.F.; Yeung, M.; Ren, C.H.; Kapadia, R. Mimicking Biological Synaptic Functionality with an Indium Phosphide Synaptic Device on Silicon for Scalable Neuromorphic Computing. *ACS Nano* **2018**, *12*, 1656–1663. [[CrossRef](#)] [[PubMed](#)]
366. Cheng, R.; Goteti, U.S.; Hamilton, M.C. Superconducting Neuromorphic Computing Using Quantum Phase-Slip Junctions. *IEEE Trans. Appl. Supercond.* **2019**, *29*. [[CrossRef](#)]
367. Sorger, V.J.; Amin, R.; Khurgin, J.B.; Ma, Z.Z.; Dalir, H.; Khan, S. Scaling vectors of attoJoule per bit modulators. *J. Opt.* **2018**, *20*. [[CrossRef](#)]
368. Laporte, F.; Katumba, A.; Dambre, J.; Bienstman, P. Numerical demonstration of neuromorphic computing with photonic crystal cavities. *Opt. Express* **2018**, *26*, 7955–7964. [[CrossRef](#)]
369. Gong, N.; Ide, T.; Kim, S.; Boybat, I.; Sebastian, A.; Narayanan, V.; Ando, T. Signal and noise extraction from analog memory elements for neuromorphic computing. *Nat. Commun.* **2018**, *9*. [[CrossRef](#)]
370. Wang, Y.; Lv, Z.Y.; Chen, J.R.; Wang, Z.P.; Zhou, Y.; Zhou, L.; Chen, X.L.; Han, S.T. Photonic Synapses Based on Inorganic Perovskite Quantum Dots for Neuromorphic Computing. *Adv. Mater.* **2018**, *30*. [[CrossRef](#)] [[PubMed](#)]
371. Wang, Z.R.; Joshi, S.; Savel'ev, S.E.; Jiang, H.; Midya, R.; Lin, P.; Hu, M.; Ge, N.; Strachan, J.P.; Li, Z.Y.; et al. Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **2017**, *16*, 101–108. [[CrossRef](#)] [[PubMed](#)]
372. Jang, B.C.; Kim, S.; Yang, S.Y.; Park, J.; Cha, J.H.; Oh, J.; Choi, J.; Im, S.G.; Dravid, V.P.; Choi, S.Y. Polymer Analog Memristive Synapse with Atomic-Scale Conductive Filament for Flexible Neuromorphic Computing System. *Nano Lett.* **2019**, *19*, 839–849. [[CrossRef](#)] [[PubMed](#)]
373. Waser, R.; Dittmann, R.; Menzel, S.; Noll, T. Introduction to new memory paradigms: Memristive phenomena and neuromorphic applications. *Faraday Discuss.* **2019**, *213*, 11–27. [[CrossRef](#)] [[PubMed](#)]
374. Prando, G. Neuromorphic computation Lowering dimensions. *Nat. Nanotechnol.* **2017**, *12*, 449.
375. Torrejon, J.; Riou, M.; Araujo, F.A.; Tsunegi, S.; Khalsa, G.; Querlioz, D.; Bortolotti, P.; Cros, V.; Yakushiji, K.; Fukushima, A.; et al. Neuromorphic computing with nanoscale spintronic oscillators. *Nature* **2017**, *547*, 428–431. [[CrossRef](#)] [[PubMed](#)]
376. Van de Burgt, Y.; Lubberman, E.; Fuller, E.J.; Keene, S.T.; Faria, G.C.; Agarwal, S.; Marinella, M.J.; Talin, A.A.; Salleo, A. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **2017**, *16*, 414–418. [[CrossRef](#)]
377. Bartolozzi, C. Neuromorphic circuits impart a sense of touch. *Science* **2018**, *360*, 966–967. [[CrossRef](#)]
378. Zhu, X.J.; Li, D.; Liang, X.G.; Lu, W.D. Ionic modulation and ionic coupling effects in MoS₂ devices for neuromorphic computing. *Nat. Mater.* **2019**, *18*, 141–148. [[CrossRef](#)]
379. Kumar, M.; Abbas, S.; Kim, J. All-Oxide-Based Highly Transparent Photonic Synapse for Neuromorphic Computing. *ACS Appl. Mater. Interfaces* **2018**, *10*, 34370–34376. [[CrossRef](#)]
380. Russek, S.E.; Donnelly, C.A.; Schneider, M.L.; Baek, B.; Pufall, M.R.; Rippard, W.H.; Hopkins, P.F.; Dresselhaus, P.D.; Benz, S.P. Stochastic Single Flux Quantum Neuromorphic Computing using Magnetically Tunable Josephson Junctions. In Proceedings of the 2016 IEEE International Conference on Rebooting Computing (ICRC), San Diego, CA, USA, 17–19 October 2016.
381. Esqueda, I.S.; Yan, X.D.; Rutherglen, C.; Kane, A.; Cain, T.; Marsh, P.; Liu, Q.Z.; Galatsis, K.; Wang, H.; Zhou, C.W. Aligned Carbon Nanotube Synaptic Transistors for Large-Scale Neuromorphic Computing. *ACS Nano* **2018**, *12*, 7352–7361. [[CrossRef](#)] [[PubMed](#)]
382. Wu, H.; Yao, P.; Gao, B.; Qian, H. Multiplication on the edge. *Nat. Electron.* **2018**, *1*, 8–9. [[CrossRef](#)]

383. Li, C.; Hu, M.; Li, Y.; Jiang, H.; Ge, N.; Montgomery, E.; Zhang, J.; Song, W.; Dávila, N.; Graves, C.E.; et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **2018**, *1*, 52–59. [[CrossRef](#)]
384. Green, S.; Aimone, J.B. Memristors learn to play. *Nat. Electron.* **2019**, *2*, 96–97. [[CrossRef](#)]
385. Merolla, P.A.; Arthur, J.V.; Alvarez-Icaza, R.; Cassidy, A.S.; Sawada, J.; Akopyan, F.; Jackson, B.L.; Imam, N.; Guo, C.; Nakamura, Y.; et al. A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science* **2014**, *345*, 668–673. [[CrossRef](#)]
386. Lin, C.K.; Wild, A.; Chinya, G.N.; Lin, T.H.; Davies, M.; Wang, H. Mapping Spiking Neural Networks onto a Manycore Neuromorphic Architecture. *ACM Sigplan Not.* **2018**, *53*, 78–89. [[CrossRef](#)]
387. Davies, M.; Srinivasa, N.; Lin, T.H.; Chinya, G.; Cao, Y.Q.; Choday, S.H.; Dimou, G.; Joshi, P.; Imam, N.; Jain, S.; et al. Loihi: A Neuromorphic Manycore Processor with On-Chip Learning. *IEEE Micro* **2018**, *38*, 82–99. [[CrossRef](#)]



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