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Anomalous enhancement of the sheet carrier density beyond the classic limit on a $SrTiO_3$ surface

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Electrostatic carrier accumulation on an insulating (100) surface of $SrTiO_3$ by fabricating a field effect transistor with Parylene-C (6 nm)/HfO_2 (20 nm) bilayer gate insulator has revealed a mystifying phenomenon: sheet carrier density n_{2D} is about 10 times as large as $C_{2D}^{ins}V_G/e$ (C_{2D}^{ins} is the sheet capacitance of the gate insulator, V_G is the gate voltage, and e is the elementary charge). The channel is so clean to exhibit small subthreshod swing of 170 mV/decade and large mobility of 11 cm^2/Vs for n_{2D} of 1×10^{14} cm^{-2} at room temperature. Since C_{2D}^{ins} does not depend on either V_G nor time duration, n_{2D} beyond $C_{2D}^{ins}V_G/e$ is solely ascribed to negative charge compressibility of the carriers, which was in general considered as due to exchange interactions among electrons in the small n_{2D} limit. However, the observed n_{2D} is too large to be naively understood by the framework. Alternative ideas are proposed in this work.

The Gauss's law $Q = CV$ in a field effect transistor (FET) is generally believed to be $en_{2D} = C_{2D}^{ins}V_G$, where, e, n_{2D}, C_{2D}^{ins}, and V_G are the elementary charge, sheet carrier density of the channel, sheet capacitance of the gate insulator, and gate voltage, respectively[1]. The equation is valid, but only when the channel is an ideal metal, where the gate electric field is completely screened (zero screening length) at the channel surface due to the infinite charge compressibility $\kappa \equiv (n_{2D}^2 d\mu/dn_{2D})^{-1}$ (μ is the chemical potential). Meanwhile, for finite κ, C_{2D}^{ins} is replaced by $(1/C_{2D}^{ins} + 1/C_{2D}^{q})^{-1}$. $C_{2D}^{q} \equiv e^2 n_{2D}^2 \kappa$ is called a quantum capacitance[2]. Total energy of the carriers corresponds to $1/C_{2D}^{q}$, thus, in general, C_{2D}^{q} is positive and $en_{2D} < C_{2D}^{ins}V_G$. Nevertheless, negative κ, for which $en_{2D} > C_{2D}^{ins}V_G$, is a long-standing target of research both experimentally[3–9] and theoretically[10,11], manifesting itself due to strong exchange interactions between carriers. Especially, in two-dimensional electron system (2DES), the exchange energy is negative and scales as $\sqrt{n_{2D}}$, while the positive (*e.g.*, kinetic) energy scales as n_{2D}; therefore, for sufficiently small n_{2D}, the total energy ($\propto 1/C_{2D}^{q}$) can be negative. What we demonstrate here is, however, far beyond the classic examples. A quasi-2DES at the channel of $SrTiO_3$ FET shows anomalous enhancement of n_{2D}: ten times as large as $C_{2D}^{ins}V_G/e$. The enhancement cannot be explained only by the exchange interaction, suggesting another mechanism of inducing negative κ.

A schematic cross-section of a standard FET is shown in Fig. 1 with the band diagrams and the relationships between the capacitances following a widely-accepted concept of the accumulation-type metal-oxide-semiconductor FET; thick substrate (channel) of the FET is implicitly grounded in the far distance, which gives zero of the chemical potential. The gate voltage $V_G = en_{2D}/C_{2D}$ is a sum of the voltage drop in the gate insulator $V_{ins} = en_{2D}/C_{2D}^{ins}$ and the band-bending of the channel material $\varphi = en_{2D}/C_{2D}^{ch}$. Therefore, $V_G = V_{ins} + \varphi$ means $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{ch}$ (Fig. 1a). For the metallic channel, the chemical potential (Fermi energy) μ/e substitutes for φ, and C_{2D}^{ch} is replaced by the quantum capacitance $C_{2D}^{q} \equiv e^2 n_{2D}^2 \kappa$ (Fig. 1b). It is still possible to consider C_{2D}^{ch} for the nonmetallic bulk part of the substrate, and $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{q} + 1/C_{2D}^{ch}$. But $1/C_{2D}^{ch} (\ll 1/C_{2D}^{q})$ term is usually omitted. The channel material in this study is $SrTiO_3$. It changes from an insulator to metal by gating[12], so we use a notation C_{2D}^{sto} in lieu of both C_{2D}^{ch} and C_{2D}^{q}. $SrTiO_3$ is a classic material for solid-state physics but is a cynosure of modern oxide-electronics researches because of the formation of quasi 2DES at the surface[13–15] or interface[16,17], as well as the large mobility of the confined 2D carriers without a freeze-out[18–21]. Both the confinement and the large mobility are originated in or, if not more, influenced by the quantum paraelectricity[22] with a large and nonlinear dielectric response[23]. Furthermore, at the surface and interface, where the inversion

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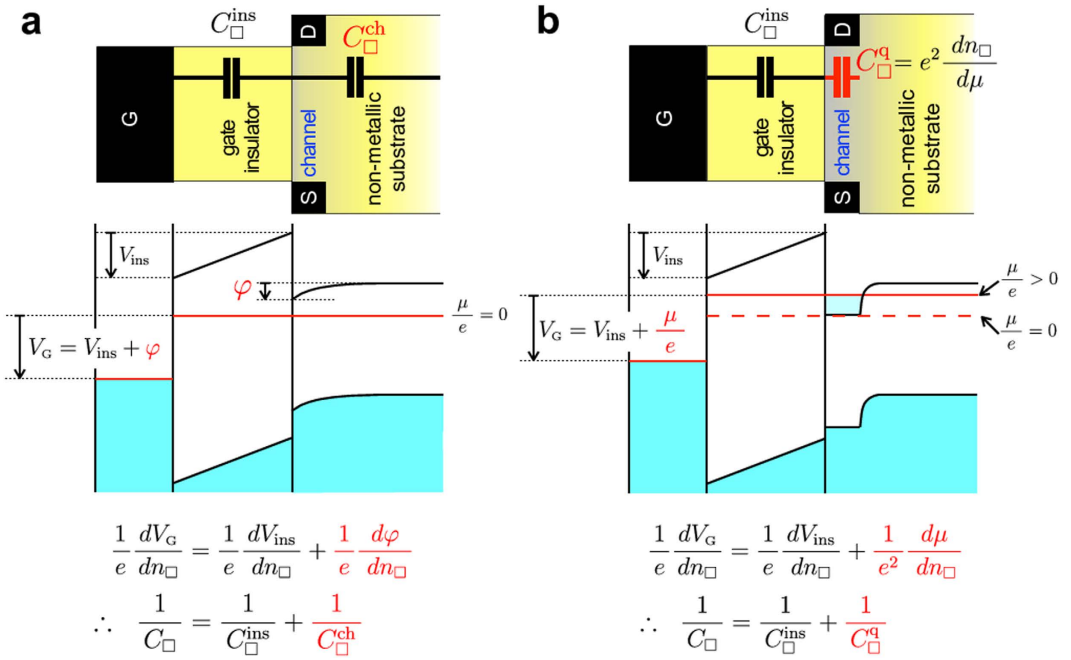

Figure 1. Schematic pictures of the cross section and the band diagram of FET. Neither distance nor energy of the picture scales to that of the real device. (**a**) The channel is an n-type non-metallic material (*e.g.*, non-doped $SrTiO_3$). By differentiating $V_G = V_{ins} + \varphi$ with respect to n_{2D}, and by using the Gauss's law, we obtain $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{ch}$. (**b**) For larger V_G, the channel becomes metallic and $V_G = V_{ins} + \mu/e$. Same as (**a**) the relationship $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{q}$ is obtained, where C_{2D}^{q} is called a quantum capacitance (ref. 2). $n_{2D} = C_{2D}V_G$ becomes larger than $C_{2D}^{ins}V_G$ only when C_{2D}^{q} is negative.

symmetry is broken, the charge confinement induces some intriguing electronic properties; for example, the Rashba spin-orbit coupling at the surface of $SrTiO_3$ discussed in refs 24–26.

However, it is intensely difficult to fabricate such a high quality FET on $SrTiO_3$ as to reveal the true nature of the exotic phenomena. The band gap of $SrTiO_3$ is nearly 3.2 eV[27,28], but it turns to be a good metal by *a very tiny electron doping* of $8.5 \times 10^{15}\,cm^{-3}$ (corresponding to the removal of a few oxygen atoms out of 10^7), which is orders of magnitude lower than the threshold of metallicity in Si ($3.5 \times 10^{18}\,cm^{-3}$) or Ge ($3.5 \times 10^{17}\,cm^{-3}$)[29]. Thus, the channel of $SrTiO_3$ FET becomes conductive quite easily by the oxygen-defect formation. In other words, the channel current of some $SrTiO_3$ FETs might be rather dominated by electrochemical reaction than purely electrostatic carrier-density modulation[30]. Therefore, in this paper, we propose an alternative gate insulator: an organic/inorganic bilayer consisting of 6 nm ultra-thin poly-monochloro-*para*-xylylene (Parylene-C) and 20 nm HfO_2, as schematically shown in Fig. 2a. The film of Parylene-C polymer is widely used for coating a variety of material surfaces, because it is highly conformal, pin-hole free, quite inert to any gases and chemicals, and sufficiently stable from around 200 °C down to at least 60 mK[31]. The bilayer gate insulator was deposited on the atomically-flat (100) surface (miscut-angle is less than about 0.03°) of non-doped $SrTiO_3$ single crystals provided by Shinkosha Co., Ltd. The photos of our FETs are shown in Fig. 2, and the cross-section images obtained by the transmission electron microscopy (TEM) are shown in Fig. 3a–d. The step and terrace surface of our $SrTiO_3$ crystals is noticeably insulating with the sheet resistance above our instrumental limit ($\sim 10^{13}\,\Omega$) at room temperature, and this surface is kept sufficiently insulating after the fabrication process of FET.

The high quality of our FET manifested itself in the subthreshold behaviour. Figure 3e shows $I_{SD} - V_{SD}$ plot for fixed V_G for the three-terminal device (See Fig. 2c). $I_{SD} \propto V_{SD}$ for small V_G, but it shows upward convex for $V_G \gtrsim 1.6\,V$, which is called the threshold voltage V_{th} and the region $V_{SD} < V_{th}$ is dubbed as the subthreshold region. As shown in the $I_{SD} - V_G$ curves in Fig. S1 of the Supplementary Materials, it is seen in the subthreshold region that $\log_{10} I_{SD} \propto V_G$. Indeed, with φ in Fig. 1a, $I_{SD} \propto \exp(e\varphi/k_BT)$, where T is the temperature and k_B is the Boltzmann constant, because only the thermally activated carriers of the valence band can contribute to the transport. Since $\varphi = n_{2D}/C_{2D}^{sto} = (1 + C_{2D}^{sto}/C_{2D}^{ins})^{-1}V_G$, the subthreshold swing defined as $S \equiv \Delta V_G/\Delta(\log_{10} I_{SD})$ can be expressed as $S = (k_B T/e)\ln 10 \times (1 + C_{2D}^{sto}/C_{2D}^{ins}) \equiv n(T) \times m$. $n(T)$ is denoted as transport factor, and m as body factor[32,33]. By measuring S, we can obtain $C_{2D}^{sto}/C_{2D}^{ins}$ ratio.

S is in general estimated from the $I_{SD} - V_G$ plot, but it might include a significant contribution of the contact resistance. Therefore, we deduced S in a more comprehensive manner. We carried out $I_{SD} - V_G$ measurements in the subthreshold region with fixed $V_{SD} = 1\,V$ for the devices with $L = 2$, 4 and 9 μm and $W = 4L$. Then, WR_{exp} was plotted against L (Fig. 3f). Here, $R_{exp} = V_{SD}/I_{SD}$ at $V_G^{eff} \equiv V_G - V_G^O = 0.5\,V$. V_G^O is the cut-off gate voltage, below which I_{SD} is smaller than the noise level of 100 fA (see Supplementary Materials for details). By comparing WR_{exp} with $R_O + LR_{2D}$, the sheet resistance R_{2D} is obtained. We applied this method for dozens of V_G^{eff}, and all the R_{2D} values were plotted in Fig. 3g. We can see $\log_{10} R_{2D}$ is clearly proportional to V_G^{eff}, and deduced $S = 171\,mV/dec$-

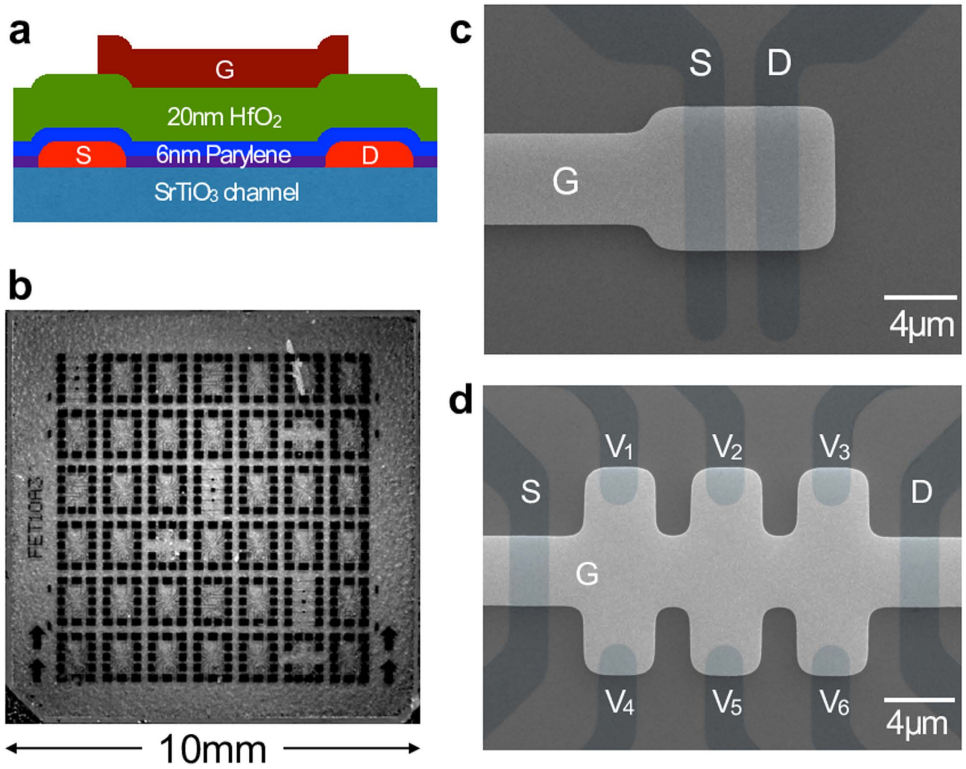

Figure 2. FET with HfO_2 (20 nm)/Parylene-C (6 nm) solid-state bilayer gate insulator studied in this work. (**a**) Schematic cross-section image of our three-terminal FET device. (**b**) Photograph of a 10 mm × 10 mm (100) $SrTiO_3$ substrate with the FET devices fabricated on it. Scanning electron microscopy images of (**c**) a three-terminal FET device, and (**d**) multi-terminal one. G, S and D stand for gate, source, and drain electrodes, respectively. V_1–V_6 are potential probes.

ade. This is indeed in good coincidence with the values simply estimated from the $I_{SD} - V_G$ plot, indicating that the contact resistance of our FET does not contribute to the S value. Since the material-independent transport factor $n(T) = (k_B T/e)\ln 10$ is 60 mV/decade at 300 K, $S = 171$ mV/decade of this study is surprisingly small. (It was reported that the value of S was ~100 mV/decade even for Si[34], ~250 mV/decade for $SrTiO_3$[35], and ~1200 mV/decade for $KTaO_3$[36]). From $m = 2.8$, we deduced $C_{2D}^{sto} = 0.50\,\mu F/cm^2$. If we assume the dielectric constant of $SrTiO_3$ is 310 at room temperature, the effective thickness for C_{2D}^{sto} is 0.55 μm. This means in the subthreshold region the gate electric field can penetrate into deep bulk of $SrTiO_3$ (0.55 μm) without a large Thomas-Fermi screening of free carriers possibly originated in the defects of Parylene-C/$SrTiO_3$ interface. Put plainly, the Parylene-C passivation on the defect-prone $SrTiO_3$ surface[37,38] works fairly well. This is one of the two important premisses of this study.

The other premise is that the ultra-thin Parylene-C film works not only as a passivation layer protecting $SrTiO_3$ channel from the high-k dielectric HfO_2 but also works as a good capacitive layer by itself. We fabricated Ti(10 nm)/Parylene-C (3 nm)/HfO_2 (20 nm)/Ti(5 nm)/Au(500 nm) parallel plate capacitors, and scrutinised the capacitance by both quasi-static and ac measurement. Details are given in the Supplementary Materials. The deduced sheet capacitance of the gate insulator of our FET, Parylene-C (6 nm)/HfO_2 (20 nm), is $C_{2D}^{ins} = 0.28\,\mu F/cm^2$ as well as the dielectric constants of 21.5 and 2.70 for the HfO_2 layer and the Parylene-C layer, respectively, consistent to the values of 20 and 3.15 reported in literature. Alternatively, we may also assume the dielectric constants of 20 and 3.15 for HfO_2 and Parylene-C, respectively. Then, the film thickness becomes 18.6 nm and 3.5 nm for HfO_2 and Parylene-C, respectively, both of which are almost equivalent to the results of TEM.

By using this bilayer gate insulator, we have finally obtained both the fairly clean channel and the continuous electrostatic control of the carrier density on $SrTiO_3$. This achievement, however, has given a new twist to the research of $SrTiO_3$. Figure 4a shows n_{2D} obtained by the Hall effect measurement for the multi-terminal FET device (Fig. 2d: details of the experiments are described in the Supplementary Materials). As mentioned above, $n_{2D} = C_{2D}(V_G - 1.88)/e$, where $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{sto}$ with $C_{2D}^{ins} = 0.28\,\mu F/cm^2$ and $C_{2D}^{sto} = 0.50\,\mu F/cm^2$. Thus, $n_{2D} = 1.1 \times 10^{12}(V_G - 1.88)\,cm^{-2}$. (It should be noted here that the 1.88 V offset, above which the accumulation of the carriers in the channel becomes observable by the Hall effect measurements, may be due to the relatively larger contact resistance of the multi-terminal FET device used for the measurements; however, the origin of this offset does not affect to the following discussion). To our surprise, the measured n_{2D} is *much larger than this naive estimation*; it reaches to around $1 \times 10^{14}\,cm^{-2}$ for $V_G = 6$ V. Even if this extra carriers are provided by the formation of oxygen/cation defects in the $SrTiO_3$ channel during the application of the large V_G (though the channel is

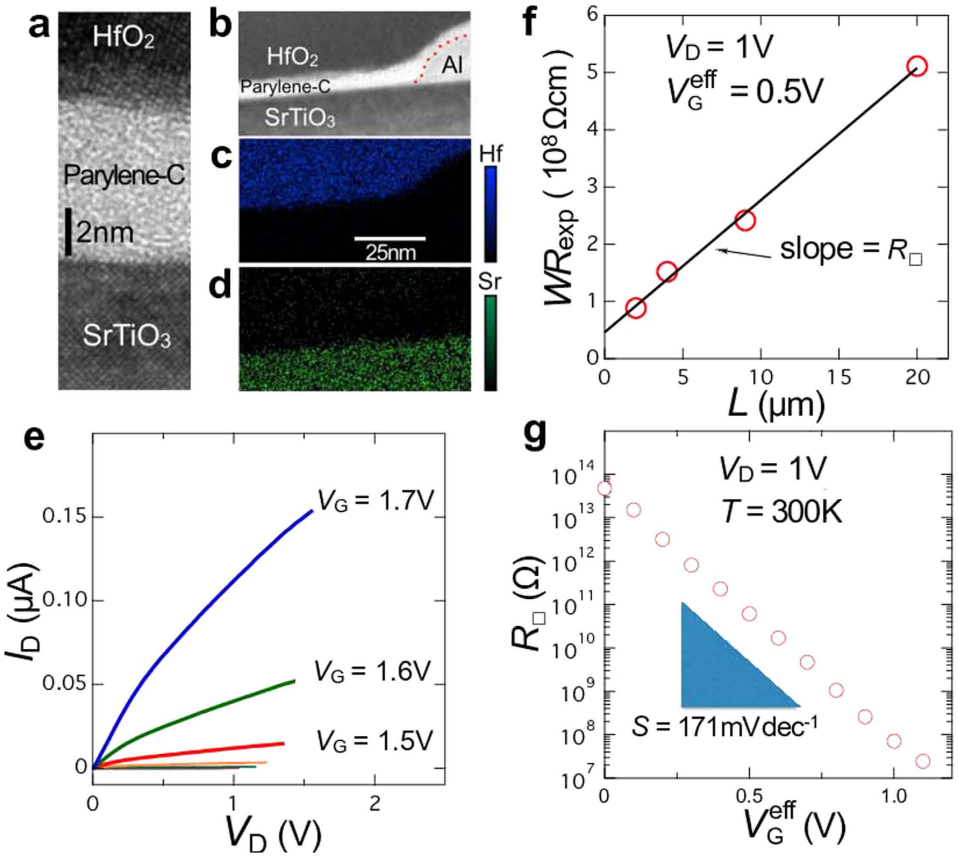

Figure 3. Characteristics of $SrTiO_3$ FET with HfO_2 (20 nm)/Parylene-C (6 nm) bilayer gate insulator. (**a**) Cross sectional TEM image of the channel. (**b**) Cross sectional scanning TEM (STEM) image near the Al electrode (dotted line is a guide to eyes separating Parylene-C and Al). (**c**) Energy-dispersive x-ray spectroscopy mapping for Hf atom and (**d**) that for Sr atom. (**e**) $I_{SD} - V_{SD}$ plots for 3-terminal device with $L = 20\,\mu$m and $W = 80\,\mu$m for several V_G. (**f**) $WR_{exp} \equiv WV_{SD}/I_{SD}$ for four FETs with different sizes but fixed W/L ratio plotted as a function of L (open circles). Solid line is the least-square fit ($WR_{exp} = R_O + LR_{2D}$) to deduce R_{2D}. (**g**) R_{2D} vs. V_G^{eff} plot gives S of 171 mV/decade.

fairly protected by Parylene-C layer and is actually clean), it should be noted that n_{2D} cannot be modulated without a change of C_{2D}, independent of sources of the carriers.

We have measured the Hall effect for more than ten FET devices on three different $SrTiO_3$ substrates (two results are shown in Fig. S3), and confirmed all of them showed qualitatively same n_{2D} enhancement. In order to explain this large discrepancy, we have assumed a naive model that the channel is a *serial* connection of a bulk $SrTiO_3$ ($C_{2D}^b = 0.50\,\mu$F/cm^2), and a surface layer (C_{2D}^s). When V_G is small, C_{2D}^b is most dominant to C_{2D}^{sto}, but as V_G increased, accumulated carriers screen the gate voltage; *i.e.*, for $V_G > V_{min}$, C_{2D}^s becomes more dominant. Then, we introduced a tractable model: $1/C_{2D}^{sto} = (1 - \eta) \times (1/C_{2D}^b) + \eta \times (1/C_{2D}^s)$, where $\eta \equiv 1/2 + \tanh[\alpha(V_G - V_{min})]$. ($\alpha = 0.68$ and $V_{min} = 2.8$ V are non-essential parameters). This is an ad-hoc phenomenological model to express that C_{2D}^b changes smoothly from C_{2D}^{sto}-dominant to C_{2D}^s-dominant, thus the mathematical formula is not relevant. If C_{2D}^s is a large positive number as that of a good metal, $1/C_{2D}^{sto}$ and corresponding n_{2D} behave as dash-dotted lines (purple) in Fig. 4a. Deviation is still large. Then, if we assume negative capacitance $C_{2D}^s = -0.31\,\mu$F/cm^2, the calculated n_{2D} coincides with the measured n_{2D}.

We understand that I_{SD}, C_{2D}^{sto} and n_{2D} should behave as shown schematically in Fig. 4b. Negative $C_{2D}^{sto} = -0.31\,\mu$F/cm^2, *i.e.*, *negative* κ, *is inevitable for explaining the large enhancement of* n_{2D}. But a question arises. If this is ascribed to the exchange interaction of the quasi-2DES on $SrTiO_3$ as explained in literature[3–5], averaged distance between the electrons should be much larger than the Bohr radius a_B, *i.e.*, $(\pi n_{2D} a_B^2)^{-1/2} \gg 1$, and the system may become like the Wigner crystal with negative chemical potential $\mu \simeq -2.9 e^2 n_{2D}^{1/2}/\varepsilon$, where ε is a direlectric constant of $SrTiO_3$ (ref. 39). However, n_{2D} in this study is in the order of 10^{14} cm^{-2}, then the corresponding values $(\pi n_{2D} a_B^2)^{-1/2} \simeq 11$ and $\mu \simeq -53$ eV are both unreasonable. It was suggested that negative κ is also realised in electronic systems close to half filling[40], but this neither is applicable to our samples. Therefore, the significant enhancement of n_{2D} cannot be explained solely by the negative κ originating in the exchange interactions; we need an alternative idea.

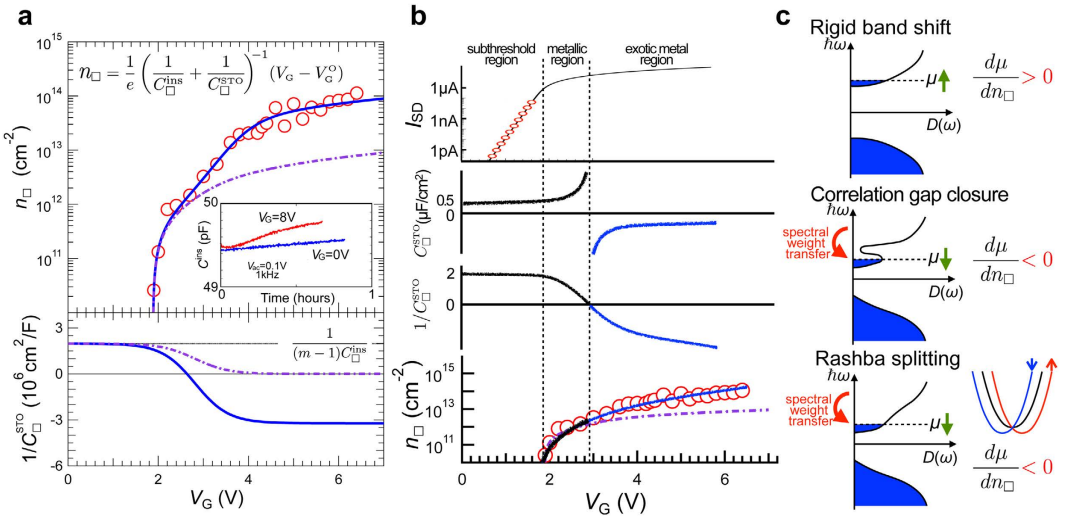

Figure 4. Interpretation of n_{2D} enhancement by a negative κ model. (**a**) Top: sheet carrier density n_{2D} (open circles) obtained by the Hall effect measurement for the multi-terminal FET device. Solid line (blue) is a least-square fit of the data to $n_{2D} = C_{2D}(V_G - V_G^O)/e$, where $1/C_{2D} = 1/C_{2D}^{ins} + 1/C_{2D}^{sto}$, C_{2D}^{ins} is 0.28 μF/cm^2, and V_G^O is 1.88 V. For C_{2D}^{sto}, we used a model shown in the bottom panel (See main text for details). Bottom: the dash-dotted line (purple) represents a case that $C_{2D}^{sto} = (m-1)C_{2D}^{ins}$ in the subthreshold region with the body factor m of 2.8 changes to $C_{2D}^{sto} = \infty$ of the ideal metal. The solid line (blue) becomes negative which explains the enhancement of n_{2D}. Inset shows the capacitance of the HfO_2/Parylene-C gate insulator as a function of time measured while continuously applying the voltage. The variation is less than 2% for one hour even for the application of 8 V which is close to the breakdown voltage. (**b**) Schematic picture of I_{SD}, C_{2D}^{sto} and n_{2D} with respect to V_G. In the metal region, $C_{2D}^{sto} \to +\infty$, and comes back from $-\infty$. However, $1/C_{2D}^{sto}$ changes continuously, which explains the observed n_{2D}. (**c**) Negative capacitance means the charge compressibility $\kappa \equiv (n_{2D}{}^2 d\mu/dn_{2D})^{-1}$ is negative, *i.e.*, $d\mu/dn_{2D}$ is negative. In the general rigid-band model, $d\mu/dn_{2D} > 0$. If the density of states $D(\omega)$ is changed by the carrier doping, $d\mu/dn_{2D} < 0$ can be realised. Closure of the correlation gap such as the Mott transition, and a band-splitting such as the Rashba effect are the typical examples.

Then, we consider the shift of μ further. In a rigid-band model, where the binding energy of each band shifts monotonously without changing the gaps, μ increases by the electron doping and decreases by the hole doping, always leading to positive $d\mu/dn_{2D}$ and thus positive κ as shown in Fig. 4c (top). On the contrary, in strongly correlated electron systems, the carrier doping drives the spectral weight transfer (naively a change of the density of states) from the higher energy incoherent states to the lower energy quasiparticle band to fill the Mott-Hubbard gap. Since the band gap decreases, μ decreases effectively and $d\mu/dn_{2D}$ becomes negative[41] as shown in Fig. 4c (middle) more interesting is that the carrier confinement at the surface of $SrTiO_3$ with perpendicular gate electric field gives rise to the Rashba effect[42]. If the Rashba spin-orbit coupling is large, the band structure depends on the gate voltage, *i.e.*, n_{2D}, leading to a non-rigid band structure as well. That is, the coupling lowers the band edge quadratically, and thus the negative $d\mu/dn_{2D}$ is realised[43,44] as depicted in Fig. 4c (bottom). However, the absolute value of our negative capacitance $-0.31\ \mu$F/cm^2, which corresponds to $d\mu/dn_{2D} = -5.1 \times 10^{-13}$ eV cm^2, is too large. For V_G between 4 V and 6 V, Δn_{2D} is around 5×10^{13} cm^{-2}, then $\Delta\mu \simeq -26$ eV, which is difficult to be understood either by the Mott transition[10,41] or the Rashba effect[43–45].

We think a clue to approach this problem is an inhomogeneity of the channel. As shown in Fig. S7c in the Supplementary Materials, we have observed a sudden decrease of the internal voltage distribution in the channel along I_{SD} while increasing V_G. This has already been observed in other $SrTiO_3$ -FET, indicating a formation of conducting domains in the insulating matrix, which eventually forms a conducting filament by percolation[19]. Here we assume that the channel consists of two regions, *i.e.*, the metallic domains with the negative sheet capacitance C_{2D}^-, and the non-metallic matrix with the normal positive sheet capacitance C_{2D}^+. Then, the channel sheet capacitance C_{2D}^{sto}, which is given by $C_{2D}^{sto} = (1-\xi)C_{2D}^+ + \xi C_{2D}^-$ with the volume fraction ξ can be $-0.31\ \mu$F/cm^2, even if C_{2D}^- is the value which gives a reasonably small $\Delta\mu$. Details are given in the Supplementary Materials.

Inhomogeneity of Parylene-C thickness in our gate insulator (~30% at most), and other features such as the one dimensional metallic state at the step edge of $SrTiO_3$ (ref. 46) would be the origins of charge inhomogeneity. Moreover, the large positive κ, which the insulating $SrTiO_3$ substrate holds due to the quantum paraelectricity, can augment the inhomogeneities further. Nevertheless, those "*extrinsic inhomogeneities*" cannot explain the 1000% enhancement of n_{2D} as observed in this study. Therefore, we made an inference that an electronic phase separation with the spinodal instability may be induced by $\kappa \to 0$, *i.e.*, $C_{2D}^{sto} \to \infty$ in our case[47]. In fact, the phase separation and the charge segregation are natural consequences of the negative capacitance even in ideally homogeneous 2DES[43]. The charge segregation may cause a local charge imbalance at finite length scales. The frustration between the electrostatic cost and the energy gain due to the phase separation is a possible mechanism of charge inhomogeneous (stripe) states[48]. However, in our FET, the local charge on the $SrTiO_3$ surface is balanced by the

charge on the gate, thus the frustration may be weaken and the typical size of inhomogeneous regions can be microscopic. We hope that this insight motivate further investigation and brings us better understanding of the intriguing physics still hidden in the $SrTiO_3$ surface.

In summary, n_{2D} of the channel of $SrTiO_3$ FET with Parylene-C (6 nm)/HfO_2 (20 nm) hybrid gate insulator showed anomalous enhancement: ten times as large as the expected value $C_{2D}^{ins} V_G/e$, indicating negative κ, *i.e.*, negative C_{2D}^{sto}. However, if the whole channel is a single metallic state with the negative κ, the chemical potential shift becomes too large. On the other hand, transport behaviour suggests the inhomogeneous carrier distribution of the channel, though the channel is fairly clean as evidenced by the small subthreshold swing $S = 171$ mV/decade and large carrier mobility ~11 cm^2/Vs. An intrinsic electronic inhomogeneity is a natural consequence of the negative κ, thus it can happen on the channel of our $SrTiO_3$ -FET. The missing link among the huge n_{2D} enhancement, the negative κ, and the intrinsic inhomogeneity will be elucidated by detailed studies.

Methods Summary

Experimental and data analysis methods with associated references are available in the Supplementary Materials.

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Author Contributions

N.K. and A.K. fabricated the devices, and N.K. performed all the measurements. I.H.I. conceived and supervised the project. All the authors discussed the results, and N.K. and I.H.I. cowrote the manuscript.

Additional Information

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