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A Neuransistor with Excitatory and Inhibitory Neuronal Behaviors for Liquid State Machine

*Woon Hyung Cheong, Geunyoung Kim, Younghyun Lee, Eun Young Kim, Jae Bum Jeon, Do Hoon Kim, and Kyung Min Kim**

A liquid state machine (LSM) is a spiking neural network model inspired by biological neural network dynamics designed to process time-varying inputs. In the LSM, maintaining a proper excitatory/inhibitory (E/I) balance among neurons is essential for ensuring network stability and generating rich temporal dynamics for accurate data processing. In this study, a "neuransistor" is proposed that implements the E/I neurons in a single device, allowing for the hardware implementation of the LSM. The device features a three-terminal transistor structure embodying TiO_{2-x}/Al_2O_3 bi-layer, providing a two-dimensional electron electron gas (2DEG) channel at their interface. This device demonstrates hybrid excitatory and inhibitory dynamics with respect to the applied gate bias polarity, originating from the charge trapping/detrapping between the 2DEG and TiO_{2-x} layers. Additionally, the three-terminal configuration allows masking capabilities by selecting terminal biases, realizing a reservoir behavior with superior reliability and durability. Its use in an LSM reservoir for time-series data prediction tasks using the Henon dataset and a chaotic equation solver for the Lorenz attractor is demonstrated. This benchmarking indicates that the LSM exhibits enhanced performance and efficiency compared to the conventional echo state network, underscoring its potential for advanced applications in reservoir computing.

1. Introduction

Biological neurons communicate by exchanging various neurotransmitters via synapses. These neurotransmitters contribute to the formation of the membrane potential in the neuron, facilitating the transmission of action potentials.[1–3] Depending on their role in action potential generation, the neurotransmitters can be classified as excitatory neurotransmitters (e.g., glutamate) or inhibitory neurotransmitters (e.g., gamma-aminobutyric acid). The proportion of excitatory or inhibitory neurotransmitters flowing to the post-synaptic neuron determines whether the net gain of the post-synaptic potential is positive or negative.[4] When the membrane potential is positive (or depolarized), it is called excitatory post-synaptic potential (EPSP), and when it is negative (or hyperpolarized), it is called inhibitory post-synaptic potential (IPSP).[5–7] The membrane potential decays over time, which is called repolarization, making the neuron system function as a temporal signal encoder.[8–10]

The neural system maintains appropriate ratios of the excitatory and inhibitory signals, known as the E/I balance. A representative example of E/I balance is the phenomenon where hyperpolarization follows depolarization during an action potential when a neuron fires. This occurs due to the feedback mechanism of EPSPs and IPSPs, which helps prevent continuous neuronal firing. Even before a neuron fires, EPSPs and IPSPs work together to regulate the neuron's membrane potential (see Figure S1 in the Supporting Information for the biological mechanism of E/I balance). This prevents excessive signal transmission or over-inhibition that can lead to neurological disorders like epilepsy and ensures stable neural activity and efficient information processing, as illustrated in **Figure 1a**.[11–14]

One of the neuromorphic computing technologies that best mimics these characteristics of the brain is the liquid state machine (LSM). LSM is a type of reservoir computing (RC), specifically designed to process spiking inputs, making it particularly strong in temporal pattern recognition. The most notable feature of LSM is that, like the brain, it utilizes the dynamic balance and regulation between excitatory and inhibitory neurons, as depicted in Figure 1b.[15,16] Therefore, LSM is considered the most

W. H. Cheong, G. Kim
Applied Science Research Institute
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon 34141, Republic of Korea
Y. Lee, J. B. Jeon, D. H. Kim, K. M. Kim
Department of Materials Science and Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon 34141, Republic of Korea
E-mail: km.kim@kaist.ac.kr
E. Y. Kim, K. M. Kim
Department of Semiconductor Technology
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon 34141, Republic of Korea

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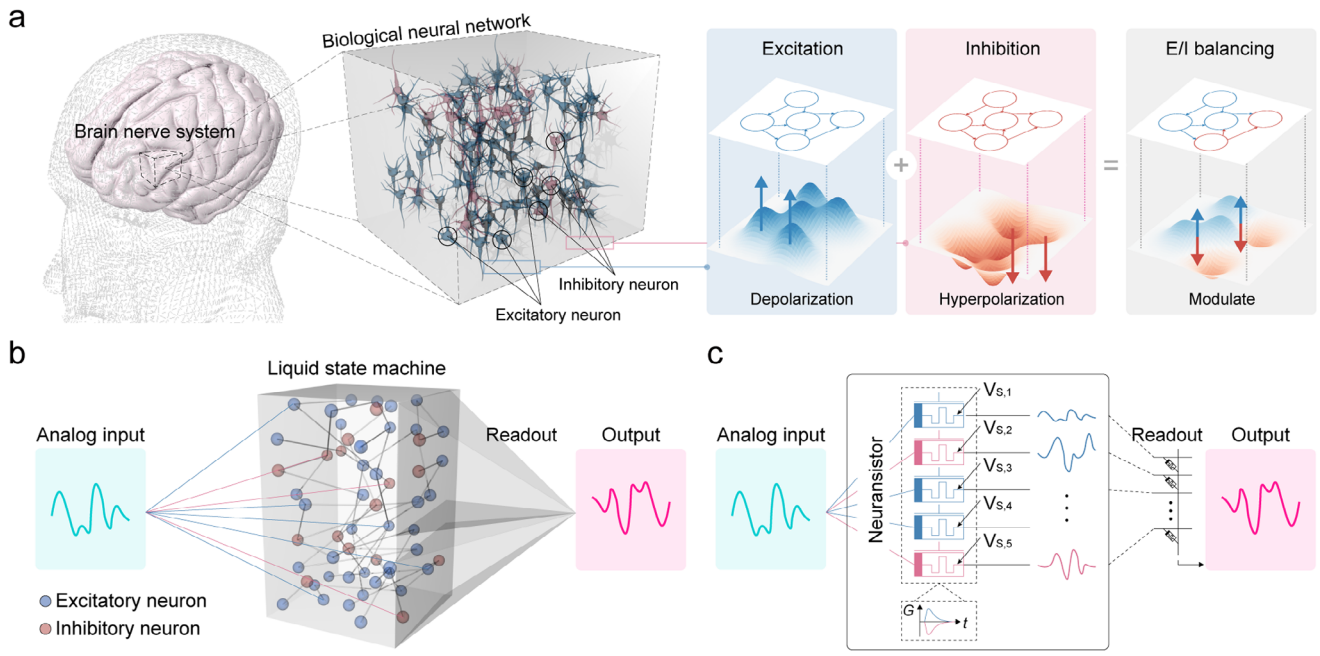

Figure 1. The neuransistor exhibiting hybrid excitatory and inhibitory neural dynamics and its application in the brain-like LSM. a) The brain nerve system includes a neural network with excitatory and inhibitory neurons, producing excitation (depolarization) and inhibition (hyperpolarization) signals, leading to E/I balancing. b) The LSM with excitatory and inhibitory nodes for analog input processing and output generation. c) A hardware form of the LSM with the neuransistor. Each neuransistor encodes the input in various forms, and their weighted summation produces the encoded output.

accurate model for replicating biological neuronal activities among known RC models.[17] While the advantages of LSM are clear, implementing its required bi-directional polarization behavior (the ability to polarize in both directions, known as depolarization and hyperpolarization, respectively) and repolarization behavior (i.e., the relaxation of the facilitated potential) within a single device necessitates a complex circuit design, and no effective solution has yet been proposed.

Memristors or memtransistors can realize such complicated neuromorphic functionalities directly with simple device architectures. so brain emulation using them has already been extensively investigated for long-term synaptic plasticity,[18–20] short-term synaptic plasticity,[21,22] their hybrid synaptic characteristics,[23–25] and neuronal behaviors.[26–28] Long-term synaptic plasticity enables stable memory retention, making it suitable for vector-matrix multiplication accelerators through array integration. Short-term synaptic plasticity is essential for mimicking biological learning rules such as spike-timing-dependent plasticity.[29] Notably, hybrid synaptic devices that exhibit both long- and short-term plasticity hold promise for implementing flexible learning and adaptive mechanisms within neural networks. Furthermore, memristor-based artificial neurons have been developed to emulate leaky integrate-and-fire characteristics, allowing for efficient neural signal processing.[26] Research has also explored the replication of complex sensory neural responses using simple electronic devices.[30] These advancements suggest that memristors can play a crucial role beyond memory applications, contributing to neuromorphic computing and the precise emulation of biological neural networks. They operate through various mechanisms, making them realize various plasticity characteristics of synapses or neurons. However, despite the wide variety of known mechanisms, identifying mechanisms capable of producing the bi-directional polarization and repolarization behaviors—i.e., maintaining a stable intermediate state and exhibiting both EPSP and IPSP dynamics in a single device—remains challenging.

Moreover, encoding the inputs into diverse outputs is crucial in RC, as it generates richer temporal dynamics, thereby improving the accuracy and efficiency of learning and predicting complex time-series data. To achieve this, masking methods are commonly applied to the reservoir.[31–33] However, previous masking methods typically require preprocessing of input signals, making them complex. Therefore, new methods that can implement masking without the need for preprocessing input signals need to be explored.

In this study, we propose a neuronal memtransistor device, which we have named a "neuransistor," capable of exhibiting bi-directional polarization and repolarization dynamics while offering masked reservoir characteristics through bias configuration regulation. The neuransistor features a three-terminal (top gate (G) and bottom source and drain (S/D)) structure with an Al_2O_3/TiO_{2-x} bilayered gate oxide embodying a two-dimensional electron gas (2DEG) channel at their interface. The neuransistor exhibits bi-directional neuronal dynamics by applying a gate bias (V_G), in which the V_G polarity and amplitude can determine the polarization direction and amplitude of the plasticity. The dynamic states can be read through the S/D current (I_{SD}), making it plausibly applicable to the LSM. We present the mechanism behind this unique behavior, attributed to charge trapping/detrapping dynamics between the 2DEG and TiO_{2-x} layers, distinct from any existing mechanisms. The neuransistor can precisely encode the time-series inputs in both EPSP and IPSP

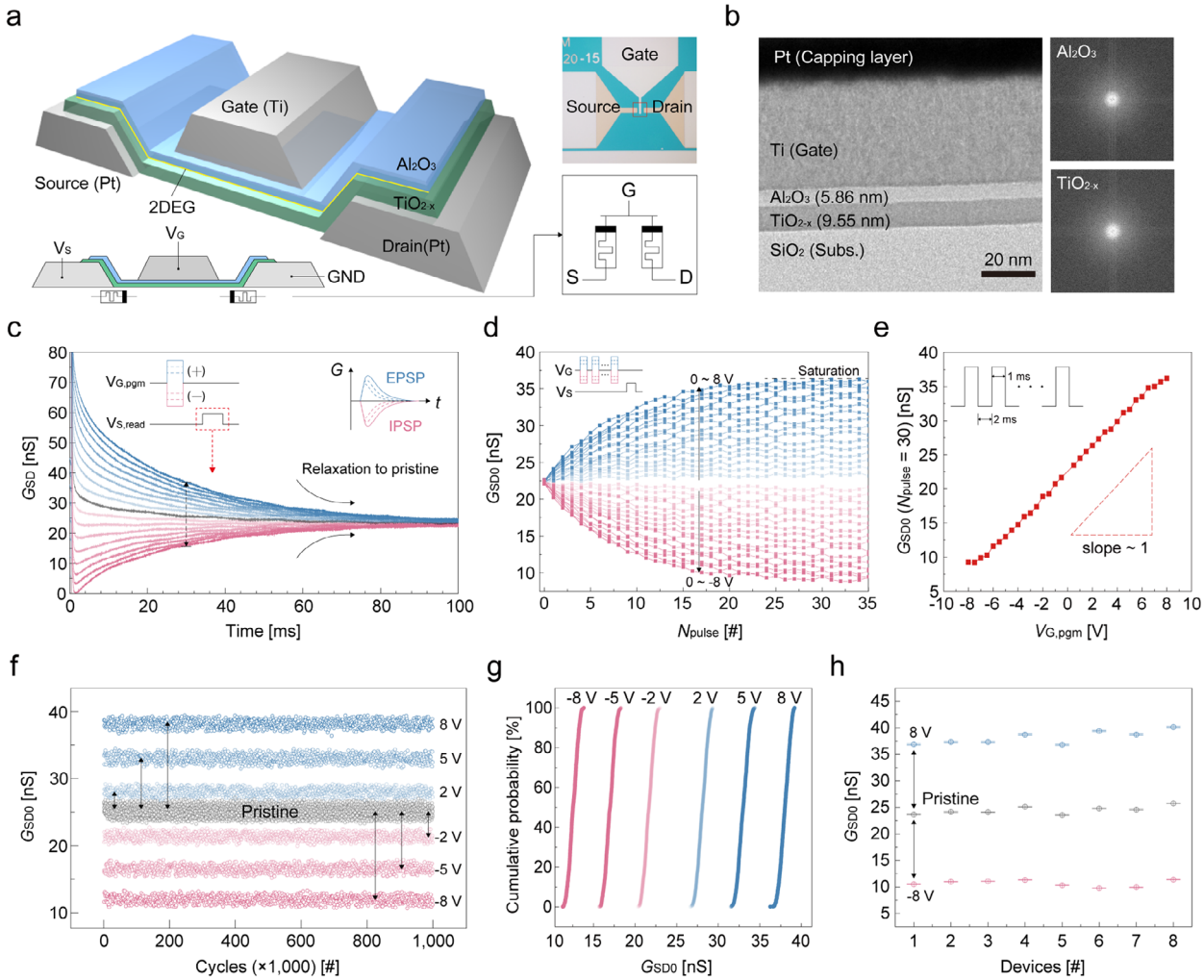

Figure 2. The structure and electrical characteristics of the neuransistor. a) The neurnasistor's structure including a cross-sectional structure (left bottom), a top-view optical microscopy image (right top), and an equivalent circuit diagram (right bottom). b) A cross-sectional TEM image and the FFT diffraction patterns of the amorphous Al_2O_3 and TiO_{2-x} layers. c) Hybrid EPSP and IPSP characteristics of the G_{SD} after $V_{G,pgm}$ application. d) Programmed G_{SD0} as a function of the $V_{G,pgm}$ pulse number (N_{pulse}) for the $V_{G,pgm}$ ranging from −8 to +8 V for 1 ms. e) Linear relationship between the applied $V_{G,pgm}$ and the saturated G_{SD0} when $N_{pulse} = 30$. f) Multi-level endurance characteristics of the G_{SD0} under $V_{G,pgm} = \pm 2$ V, ± 5 V, and ± 8 V for 5 ms. G_{SD0} was read at $V_{S,read} = +1$ V for 40 ms. A 100 ms interval was applied between the programming cycles. g) Cumulative probability of the G_{SD0} of the endurance results in f. h) Device-to-device uniformity of the pristine state and programmed state by ± 8 V $V_{G,pgm}$ conditions using 8 devices with 100 cycles each.

manners, making it applicable to the reservoirs of the LSM, as illustrated in Figure 1c. Furthermore, the neuransistor can encode the time-series inputs into multiple forms by applying an additional bias to the source terminal, generating the masked polarized output signals. This neuransistor device is highly stable and compatible with the CMOS process, demonstrating its strong feasibility as the reservoir hardware of the LSM applications.

2. Results and Discussion

2.1. Device Structure and Electrical Characteristics of the Neuransistor

Figure 2a illustrates the neuransistor device structure, comprising a Pt electrode as a source and drain, an Al_2O_3/TiO_{2-x} bilayer, and a Ti top-gate electrode. The left-bottom inset shows a cross-sectional schematic of the device. A more detailed device fabrication process can be found in the Experimental section. The right-top inset shows a top-view optical microscope image of the device and a contact pad configuration, where the dashed square in the middle indicates the device area. The channel length and width between the source and drain are 20 and 15 μm, respectively, and the gap between the gate and source (or drain) is 2.5 μm. In the device, the 2DEG layer and the source/drain are not directly connected but are separated by the TiO_{2-x} layer, unlike the typical 2DEG-based transistors. Therefore, the equivalent circuit between the source and drain terminals can be a serial connection of the source, TiO_{2-x} layer, 2DEG, TiO_{2-x} layer, and drain, as shown in the right-bottom inset. While the conductivity of the 2DEG layer is high, the TiO_{2-x} dielectric layers are

insulating, resulting in an overall lower I_{SD} level than that of the typical 2DEG-based transistors.[34] Here, the conductivity of the TiO_{2-x} layer could be either increased or decreased from the initial state, making the device exhibit intriguing bi-directional plasticity behaviors.

Figure 2b shows a cross-sectional transmission electron microscopy (TEM) image of the device with its fast Fourier transform (FFT) diffraction patterns, confirming that amorphous TiO_{2-x} and Al_2O_3 layers were uniformly deposited (see Figure S2 in the Supporting Information for energy-dispersive spectroscopy (EDS) results of Al, Si, and Ti elements). For further analysis, we also conducted TEM imaging of the edge structures of the gate and drain electrodes of the device (see Figure S3 in the Supporting Information for the cross-sectional TEM images of the electrode edge structures). The results confirmed that the fabricated electrode structures exhibit a tapered profile in both the gate and drain (or source) regions. Previous studies suggested that during the Al_2O_3 atomic layer deposition (ALD) on TiO_{2-x}, the Al precursor (trimethylaluminum, TMA) acted as a strong reducing agent, creating a high concentration of oxygen vacancies (V_O) on the TiO_{2-x} surface.[34,35] The V_O acts as n-type dopants, donating free electrons to the Ti 3*d* band and increasing the fermi level (E_F) of the TiO_{2-x} layer, resulting in a conductive 2DEG layer formation.[36,37] By fitting the resistance values to the various channel lengths of the fabricated device, the sheet resistance of the 2DEG channel layer was determined to be 5.9 MΩ/sq, which is consistent with the previously reported value[35] (see Figure S4 in the Supporting Information for the sheet resistance fitting result).

The bi-directional short-term plasticity behaviors are shown in Figure 2c. It shows the change of reading conductance between the source and drain (G_{SD}) over time (t) after programming with various conditions through the gate. The applied programming pulse ($V_{G,pgm}$) ranged from −8 to +8 V with a width of 10 ms, while the source and drain were grounded. After programming, the programmed state was then read by applying a read pulse to the source ($V_{S,read}$, +1 V for 100 ms) while the drain was grounded. The interval between $V_{G,pgm}$ and $V_{S,read}$ was 2 ms. The inset shows the pulse scheme. The reading results showed that the initial G_{SD} at $t = 0$ (G_{SD0}) was initially either excited (blue lines) or inhibited (red lines) depending on the polarity of $V_{G,pgm}$, with G_{SD0} being controlled by the $V_{G,pgm}$ amplitude. Over time, the G_{SD} gradually converged to the pristine state, following a typical exponential decay function, $G_{SD}(t) = G_{SD0}\exp(-\lambda t)$, where λ is a decay rate constant. The black line is the reference output when $V_{G,pgm}$ was 0.

Additionally, the device exhibited bi-directional integration characteristics. Figure 2d shows the G_{SD0} as a function of the number (N_{pulse}) of $V_{G,pgm}$ pulses for the $V_{G,pgm}$ ranging from −8 V to +8 V for 1 ms. Here, we plotted G_{SD0} to accurately compare the time-varying values in a non-time domain. The conductance was read using a $V_{S,read}$ of +1 V for 10 ms. All pulse intervals were 2 ms. The results indicated that the G_{SD0} gradually increased and then saturated as the N_{pulse} increased. The $V_{G,pgm}$ amplitude versus the saturated G_{SD0} (at $N_{pulse} = 30$) plot demonstrated high linearity, as shown in Figure 2e, suggesting that the device can encode input data with high precision suitable for the reservoir application. For additional comparison, we investigated the impact of gate electrode overlap with the source or drain electrode on the device characteristics (see Figure S5 in the Supporting Information for the gate overlap effect). When evaluating the memory margin of this modified device, we observed nearly identical characteristics to those of the original neuransistor device, indicating that gate overlap does not significantly affect the device's performance. This behavior can be attributed to the fact that the 2DEG layer functions as a floating gate, ensuring that a sufficient electric field is established between the source/drain electrodes and the 2DEG layer, regardless of the gate overlap.

Figure 2f shows the device's multi-level endurance characteristics of the G_{SD0} for 10^6 cycles under various $V_{G,pgm}$ conditions, showing the uniformity and stability of the devices. After each programming and reading cycle, a subsequent cycle was processed after a 100 ms interval to ensure complete relaxation to the pristine state (see Figure S6 in the Supporting Information for the detailed pulse scheme and the obtained endurance sample for 10^6 cycles at $V_{G,pgm} = +8$ V). At this point, the memory margin of the current device is less than one order of magnitude, which is relatively small compared to conventional memristors and memtransistors. However, while stable multi-bit operation is crucial for non-volatile synaptic devices, the significance of memory margin is relatively lower for dynamic reservoir devices. This is because the primary function of reservoir computing (RC) systems is signal transformation, where transient signal processing plays a more critical role than long-term data retention. In this context, we found that dynamic memristors and memtransistors used as RC hardware exhibit excellent performance as RC hardware even with a low memory margin of approximately one order of magnitude, similar to the current device.[32,38,39] Figure 2g summarizes the variation in the G_{SD0}, confirming high uniformity. The device-to-device variation is also highly uniform. Figure 2h shows the G_{SD0} uniformity among 8 different devices over 100 cycles at $V_{G,pgm}$ of +8 V and −8 V (see Figure S7 in the Supporting Information for the raw endurance data of all devices). We anticipate that this high uniformity is related to the non-filament type mechanism, which does not require the electroforming process, as reported in other studies.[40–43]

2.2. Operation Mechanism of the Neuransistor

To identify the mechanism, it is first necessary to locate where the conductance change occurs in the device. **Figure 3a** depicts the cross-sectional structure of the device, magnifying the edges of the gate (G) and source/drain (S/D) regions. While the gate region is similar to the classical gate structure of the 2DEG-based transistor, in the S/D region, the 2DEG layer covers the S/D, acting as a floating electrode. As a result, the 2DEG/TiO_{2-x}/Pt stack dominates the overall conduction of the device (see Figures S8 and S9 in the Supporting Information for the electric field simulation results using COMSOL). Additionally, to verify the operating mechanism between the 2DEG layer and the TiO_{2-x} layer, we compared the memory margin of the device with a longer 2DEG channel length, where the proportion of the 2DEG layer is higher (see Figure S10 in the Supporting Information for the memory margin result with a 100 μm channel length). The results showed no significant difference in memory margin. This finding supports that the memory effect in the neuransistor device is primarily determined by the operating mechanism of the

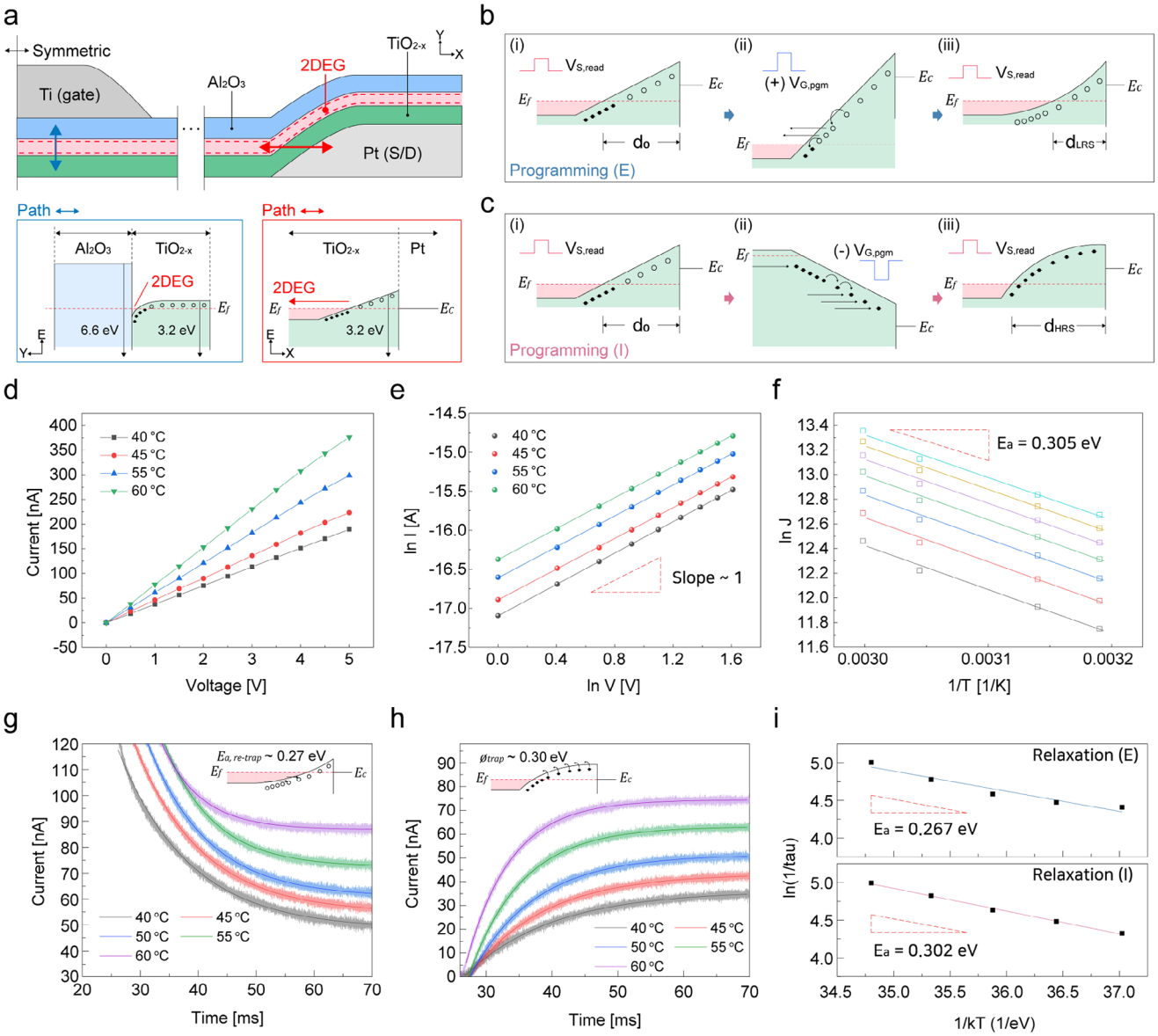

Figure 3. The operation mechanism of the neuransistor. a) A schematic cross-section and the energy band diagrams at the gate side (indicated by the blue arrow) and the drain (or source) side (red arrow). The bandgap of the dielectric layers was assumed to be 6.6 eV for Al_2O_3 and 3.2 eV for the TiO_{2-x} layer. b, c) Operation model of the neuransistor. At the drain side, the traps of the TiO_{2-x} layer are partially filled at the pristine state due to the E_F alignment. Then, by the excitatory operation with positive $V_{G,pgm}$, the traps are detrapped, leading to a higher conductance state (b). Conversely, under inhibitory operation with negative $V_{G,pgm}$, more traps are filled, resulting in a lower conductance state (c). d) I_{SD}-V_{SD} curves measured at different temperatures ranging from 40 °C to 60 °C. e) ln I versus ln V plot of d. f) Arrhenius fitting plots (ln J versus $1/T$) for the voltages ranging from +2 V (black) to +5 V (cyan). The average slopes indicate that the activation energy (E_a) is 0.305 eV. g,h) The read currents ($V_{S,read}$ = +1 V) with after positive input pulse ($V_{G,pgm}$ = +4 V, 10 ms) (g) and after negative input pulse ($V_{G,pgm}$ = −4 V, 10 ms) h) as a function of time at various temperatures ranging from 40 °C to 60 °C. i) Arrhenius fitting plots (ln($1/\tau$) versus $1/kT$) for the excitatory and inhibitory states. The E_a are 0.267 eV and 0.302 eV, respectively, which is consistent with the E_a obtained in f.

TiO_{2-x} layer rather than by resistance changes in the 2DEG layer. Consequently, the structure in Figure 3a can be approximated to a Ti(G)/Al_2O_3/2DEG/TiO_{2-x}/Pt(S/D) structure when programming (blue box) and a Pt(S)/TiO_{2-x} /2DEG/TiO_{2-x}/Pt(D) structure when reading (red box) (see Figure S11 in the Supporting Information) for the equivalent stacks in programming and reading). In this structure, the conductivity of the TiO_{2-x} layer can be increased or decreased depending on the $V_{G,pgm}$ polarity, which can be explained by the charge trapping/detrapping model between 2DEG and TiO_{2-x}.[44,45] During this process, unintended charge trapping and detrapping may occur in the region beneath the gate electrode, and the formation of fixed charges could lead to degradation of the device's operational characteristics.[43] However, as observed in Figure 2f, the device exhibited no noticeable performance degradation over multiple switching cycles. This suggests that potential unintended charge

trapping during operation has a minimal impact on the switching characteristics.

Figure 3b,c show the electronic band structure of the 2DEG/TiO_{2-x}/Pt stack in excitatory programming under positive $V_{G,pgm}$ and inhibitory programming under negative $V_{G,pgm}$, respectively. At the pristine state (panel i), the TiO_{2-x} embodies $V_{O,}$ providing the trap sites.[46,47] The energy level of some trap sites near the 2DEG interface can be lower than the Fermi energy (E_F), thus those traps are filled initially. When a positive $V_{G,pgm}$ is applied (panel ii, Figure 3b), the trapped electrons in the pristine state are released into the 2DEG layer, emptying the traps and inducing an additional internal positive potential (panel iii, Figure 3b). This lowers the effective thickness of hopping conduction (from d_0 to d_{LRS}) and leads the TiO_{2-x} layer to a low resistance state (LRS). This LRS cannot be monitored through the gate-to-drain current due to the high resistance of the Al_2O_3 layer. Therefore, this device cannot operate in a two-terminal manner. However, the LRS can be identified through monitoring the I_{SD}. When a negative $V_{G,pgm}$ is applied (panel ii, Figure 3c), more traps in the TiO_{2-x} layer are filled, increasing the hopping thickness (from d_0 to d_{HRS}) and leading the TiO_{2-x} layer to a high resistance state (HRS). Both the LRS and HRS are energetically unstable states, so they returned to their pristine state over time (repolarization), resulting in the bi-directional short-term plasticity characteristics.

This switching mechanism, associated with charge trapping/detrapping, is supported by the temperature-dependent conduction behavior. Figure 3d shows the temperature-dependent current–voltage (I–V) curves between the source and drain, ranging from 40 °C to 60 °C, under a +5 V of $V_{S,read}$. Figure 3e shows a log–log plot of Figure 3d, and Figure 3f shows the Arrhenius fitting results, giving an activation energy (E_a) of 0.305 eV. This value aligns well with the trap energy levels in TiO_2[48–50] and the Ea obtained from impedance measurements.[51] Therefore, such behavior with the Ea suggests the conduction mechanism is associated with trap-assisted hopping conduction through the TiO_{2-x} layer.[41,52]

Additionally, the temperature-dependent relaxation characteristics confirm the mechanism. Figure 3g,h shows the relaxation characteristics after excitatory ($V_{G,pgm}$ = +8 V) and inhibitory ($V_{G,pgm}$ = −8 V) pulses were applied at various temperatures. The relaxation characteristics were fitted with an exponential relaxation equation, and the time constants (τ) were obtained for each curve. Figure 3i shows an Arrhenius plot ($\ln(1/\tau)$ vs $1/kT$), confirming the relaxation E_a values of 0.267 eV for excitation and 0.302 eV for inhibition, which are very similar to the trap level of the TiO_{2-x} bulk region extracted in Figure 3f. These results further support that the switching mechanism of the neuransistor is due to charge trapping and detrapping in the serially connected TiO_{2-x} dielectric layers.

2.3. Neuransistor-Based Physical Liquid State Reservoir Computing

In reservoir computing, masks allow the reservoir to generate richer temporal dynamics from time-series input data.[32,53,54] These encoded signals are then input to a neural network for training and inference. Various methods have been proposed for applying masks on the reservoirs, which involve preprocessing the input signals with complex mask filtering, making them inefficient.[55,56] In this regard, utilizing a three-terminal structure offers an efficient way to implement the mask. While programming is conducted through two terminals, the third terminal may interfere with the programming process. However, this interference can be leveraged by designating the third terminal as the masking terminal.[57]

In the neuransistor, such mask functions can be implemented in two ways. The first method is to use EPSP or IPSP itself as a mask, which we call an E/I mask. This E/I mask can be applied as follows: When time-series data is received, the signal converter (SC) converts them into input voltage signals. At this stage, the SC may incorporate both a non-inverting amplifier and an inverting amplifier, generating EPSP and IPSP input signals, respectively. These signals are then selectively routed to the gate terminal of the neuransistor as voltage inputs ($V_{G,E/I}$) through a multiplexer. Second, when the gate is biased to $V_{G,E/I}$ and the drain is grounded, the source bias affects the gate-to-source potential. It can, therefore, influence the programming of the memristor at the source side. While this does not change the overall E/I mode, it allows for additional excitation or inhibition of the source-side memristor depending on the additional source bias polarity and amplitude. Therefore, it is termed the regulation (RG) mask, and the source bias is defined as $V_{S,RG}$. $V_{S,RG}$ is used to enhance the discriminability of input signals and is randomly selected in 1 V increments within the ±3 V range. This random selection occurs at each time step, ensuring that the system does not rely on a fixed bias pattern. In software simulations, different $V_{S,RG}$ do not significantly impact performance, but in hardware experiments, the voltage range was carefully set to ensure stable device operation. Additionally, the E/I mask and RG mask are applied together. Unlike conventional binary masking methods, the RG mask adjusts the input signal's amplitude, enabling an analog masking process. This allows input patterns to be mapped to a broader range of states within the reservoir, improving the model's learning and prediction performance. **Figure** 4a shows the overall process for the masked output signal generation in the neuransistor for the encoding process. At the masked programming process (①), combining the $V_{G,E/I}$ and $V_{S,RG}$ can program the neuransistor diversely. The input signal influences changes in the neuransistor's G_{SD}, and various states are formed through hardware-based masking. Subsequently, during the reading process (②), the read voltage (Vread) is applied, generating an output current. The resulting state vector is then compared with the target data through the readout process, reflecting the dynamic properties of the neuransistor. The conductance changes in the neuransistor serve as a key mechanism for learning temporal patterns in the LSM, and model optimization is achieved through linear regression. Combining these two masks can offer multiple masking options, providing sufficient memory capacity to operate physical LSM hardware. Unlike conventional software-based random masking methods, this approach implements masking directly at the hardware level by adjusting the gate voltage polarity and modulating the source voltage, reducing computational overhead and enabling a more hardware-friendly architecture.

Figure 4b shows the G_{SD} for various masking options when $V_{G,pgm}$ = +4 V (blue lines) and −4 V (red lines), while $V_{S,RG}$ is from −3 V to +3 V. Figure 4c magnifies G_{SD} and the conductance

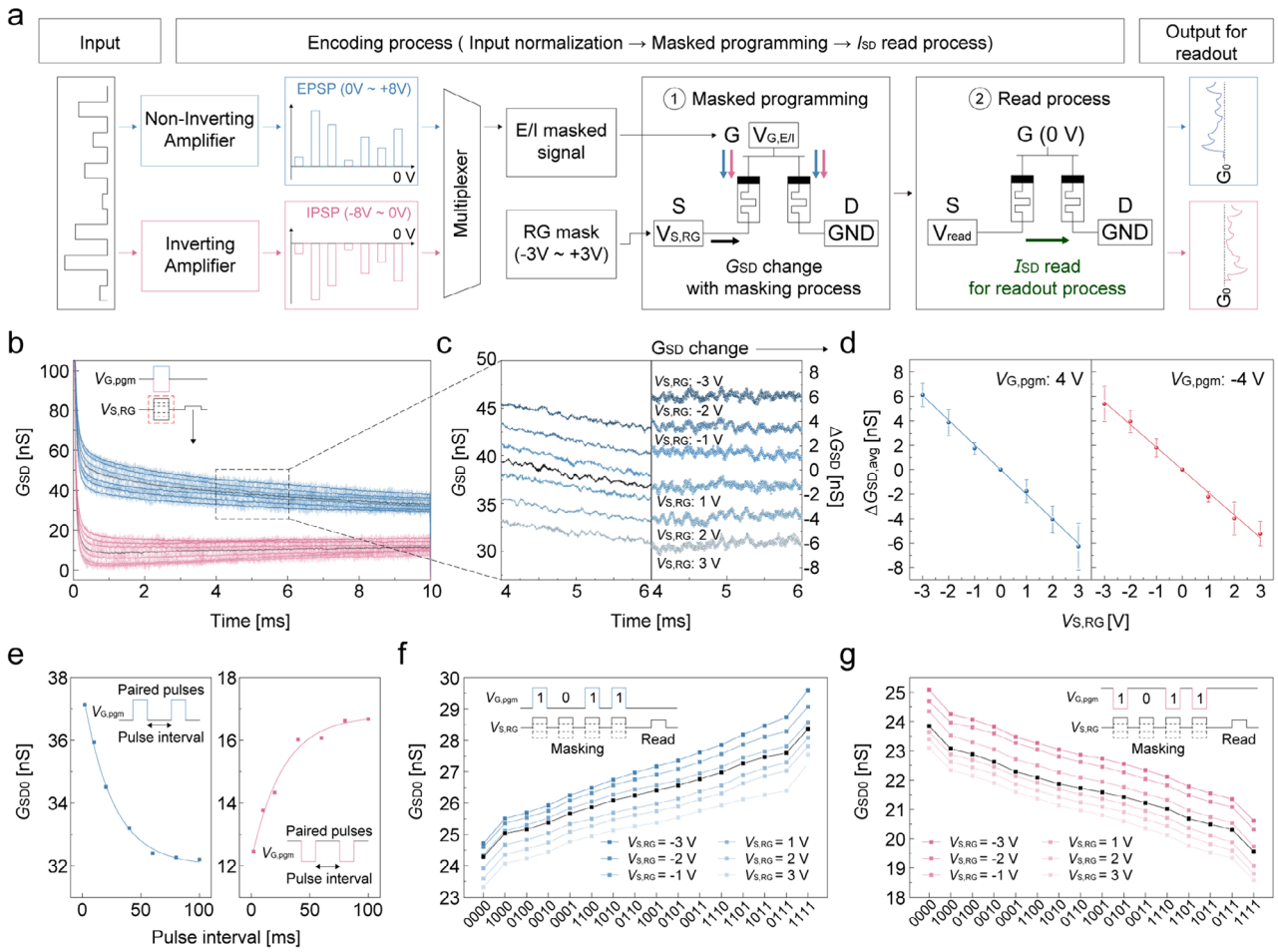

Figure 4. Masking method and reservoir characteristics in the neuransistor for LSM. a) Schematic diagram of the encoding process, including a block diagram for input normalization, masked programming (①) and read process (②) for the output generation. During the masked programming process, the E/I masked input signal ($V_{G,E/I}$) after the normalization process is applied to the gate, while the RG mask signal ($V_{S,RG}$) is applied to the source. $V_{S,RG}$ is randomly selected in 1 V increments within the ±3 V range. This random selection occurs at each time step, ensuring that the system does not rely on a fixed bias pattern. With the masked programming process, G_{SD} of the neuransistor device changes. Subsequently, the programmed state is read by reading the I_{SD} by applying V_{read} to the source. The output results are utilized in the readout process for the linear regression. b) G_{SD} for various $V_{S,RG}$ ranging from −3 V to +3 V for $V_{G,E/I}$ = +4 V (blue lines) and $V_{G,E/I}$ = −4 V (red lines). c) Magnified ΔG_{SD} for various $V_{S,RG}$ ranging from −3 V to +3 V for $V_{G,E/I}$ = +4 V. d) Linear relationship between ΔG_{SD} as a function of the $V_{S,RG}$ in the E/I modes. e) Paired-pulse facilitation (PPF) characteristics in the E/I modes. ($V_{G,pgm}$ = +8 V or = −8 V). f,g) Reservoir behaviors converting 4-bit temporal input to analog output (G_{SD0}) for various $V_{S,RG}$ conditions in the E/I modes.

changes (ΔG_{SD}) of EPSP spanning from 4 to 6 ms. This result clearly confirms that each signal is well distinguished, and the six RG masks provide sufficient encoding resolution. Figure 4d plots the averaged ΔG_{SD} of Figure 4c, showing the linear relationship between ΔG_{SD} and $V_{S,RG}$ in both EPSP and IPSP modes. This linear relationship highlights the high controllability of the proposed masking method.

Additionally, for reservoir computing, the device must be able to encode time-series inputs effectively. For this, optimization of the input pulse duration (t_d, i.e., pulse on time) and the inter-pulse interval (t_v, i.e., pulse off time) is necessary. Figure 4e shows the paired-pulse facilitation (PPF) characteristics in EPSP ($V_{G,pgm}$ = +8 V) and IPSP ($V_{G,pgm}$ = −8 V) modes as a function of the t_v ranging from 5 ms to 100 ms with a fixed t_d of 5 ms. The results exhibit ideal PPF characteristics fitted well with exponential curves, showing promise for nonlinearly converting temporal information. Figure 4f,g presents the results of encoding 4-bit EPSP and IPSP temporal inputs, with various RG mask conditions for each. The t_d and t_v were 1 ms and 4 ms, respectively, which are optimized conditions to achieve optimal encoding (see Figure S12 in the Supporting Information for the additional results with various t_v). In summary, the neuransistor can encode the 4-bit temporal input into distinguishable analog outputs under the masking conditions, making it suitable for LSM applications.

2.4. Neuransistor-Based LSM Simulation and Evaluation

The neurons in LSM can operate in both EPSP and IPSP modes, continuously changing over time.[13,15,58,59] This feature distinguishes LSMs from other RC systems, making them ideal for

neuromorphic computing. The neuransistor can be utilized to realize such EPSP and IPSP hybrid reservoir behaviors in LSM. **Figure** 5a schematically shows the reservoir constructed on a 1×*N* neuransistor array. Here, all neuransistor devices are essentially identical (black symbol), but each device operates differently due to the application of specific masking signals ($V_{G,E/I}$ and $V_{S,RG}$). In this system, continuous input signals are first processed through a hardware-based masking stage, where they are transformed into *N* masked inputs for each device (Mask #1 ∼ Mask #*N*). Each neuransistor undergoes a time multiplexing process, generating *ML* different reservoir states for a single input, where *ML* stands for the masking length. Here, the combination of masking signals (i.e., mask set) at a given time step defines the identity of the reservoir. For example, at a time step of T_1, the mask set is defined as {($V_{G,E/I}^{(T1,\,1)}$, $V_{S,RG}^{(T1,\,1)}$), ($V_{G,E/I}^{(T1,\,2)}$, $V_{S,RG}^{(T1,\,2)}$), ... ($V_{G,E/I}^{(T1,\,N)}$, $V_{S,RG}^{(T1,\,N)}$)} where $V_{G,E/I}$ is E/I masked input signals and $V_{S,RG}$ is the RG signal ($V_{S,RG}$ ∈{−3 V, −2 V, −1 V, 0 V, +1 V, +2 V, +3 V}). By applying the different mask sets, each neuransistor produces different outputs depending on the applied mask, which are combined to form the reservoir output. This masking process is repeated *ML* times for T_{ML}. In other words, a single input undergoes hardware-based masking, resulting in *ML* distinct output states. In this process, individual neurons in the liquid state reservoir (i.e., neuransistor array) exhibit different reservoir states (Reservoir #1, #2, ..., #*N*). Also, while the mask set is applied during T_{ML}, the E/I mask is randomly selected. As a result, the E/I ratio (Ratio R_1%, R_2%, ..., R_N%) during T_{ML} appears random at the individual neuron level due to the limited number of *ML*. However, throughout the entire training process, the overall E/I ratio across *N* neurons (thus, a total number of masks is *N* × *ML*) ultimately converges to 50% due to the law of large numbers. This random but overall balanced E/I ratio ensures high network diversity and maintains E/I balance. Next, the output signals generated by the *N* neurons undergo a readout process. These sequences repeat in alignment with the input signal's time steps, allowing each neuron to exhibit richer temporal dynamics.

Reflecting the reservoir characteristics of the neuransistor array, we evaluated the applicability of our device in LSM through simulations. To highlight the advantages of the EPSP and IPSP hybrid neuransistor in the LSM, we compared it with a conventional echo state network (ESN) that utilizes only EPSP or IPSP neurons. Figure 5b,c compares the prediction results of the reservoir system of ESN (red) and LSM (blue) with the prediction target (black) of the Henon dataset in a two-dimensional representation. Training and prediction were conducted for 1000 time-series data points each, with setting *ML* = 2 and *N* = 6. The result was evident that the prediction results for the LSM were more closely aligned with the target compared to the ESN. To quantitatively assess prediction accuracy, we calculated the normalized root mean square error (NRMSE) values, which are ≈0.1020 for ESN and ≈0.0097 for LSM, indicating an error difference of more than tenfold. Figure 5d summarizes the NRMSE as a function of *ML* under identical reservoir dimensions (*RD*; *RD* = *ML* ×*N*). The performance superiority of the LSM was consistently observed, and its exceptional characteristics, particularly with compact *ML*, further highlight its advantages in the context of lightweight neuromorphic computing (see Figures S13 and S14 in the Supporting Information for the time step representation results and model-related parameters for the Henon dataset). This performance comparison was conducted using a relatively shallow network with *RD* = 12. Generally, in reservoir computing models such as ESN, increasing the *RD* can potentially improve prediction performance. However, in resource-constrained environments such as edge computing, LSM offers a significant advantage in energy efficiency by achieving high performance even with a smaller reservoir size.

Subsequently, we compared the prediction capabilities for complex tasks by examining periodic and chaotic solutions using the Lorenz attractor to assess the LSM's nonlinear mapping capability.[60–62] This simulation evaluates sensitivity to initial conditions, model robustness, and noise handling capability, which are crucial for verifying whether RC models can effectively address various challenges encountered in real-world environments. Figure 5e shows the predicted state trajectory and the ground truth target (*black*) in 3-dimensions for the ESN (top) and LSM (bottom), respectively. Each emulation involved training the dataset for the initial 10 000 time steps, followed by prediction over 10 000 time steps. The *RD* was set to *ML* = 2 and *N* = 6. In the analysis of the Lorenz attractor predictions, we compared the absolute error values for each axis during prediction for 10 000 test time steps in Figure 5f. The LSM (blue) shows much lower prediction error results compared to the ESN (red).

Figure 5g compares the NRMSE as a function of the *N* with a fixed *ML* (*ML* = 2). Overall, the LSM exhibited lower error values compared to the ESN in all cases. Consistent with previous results, this suggests that the LSM using the neuransistor positively impacts time-series prediction, especially in more compact environments. Additionally, Figure 5h compares the NRMSE values as a function of the training time steps (from 1 000 to 50 000) at *ML* = 2 and *N* = 6. The results indicate that the LSM can be trained approximately three times faster than the ESN, highlighting the superior efficiency of the LSM over the ESN.

3. Conclusion

In this study, we proposed the neuransistor, a device capable of implementing the hybrid characteristics of EPSP and IPSP in brain neurons. Additionally, we demonstrated its applicability to the LSM. The operating mechanism of the neuransistor is explained by charge trapping and detrapping between the 2DEG layer formed at the Al_2O_3/TiO_{2-x} interface and the TiO_{2-x} layer. The device features a three-terminal structure, which facilitates a simplified mask implementation essential for its use as a reservoir. The neuransistor effectively mimics the excitatory and inhibitory behaviors of biological neurons by adjusting bidirectional conductivity through external voltage control. This capability enables the hardware implementation of the E/I balance in neural circuits and contributes to the stability of the LSM network.

The LSM proposed in this study has not directly processed event-driven data, as reported in previous studies; however, it dynamically regulates excitatory and inhibitory responses using neuransistors and facilitates learning based on neuron interactions.[63] The PPF and 4-bit temporal input processing methods are related to spike-based approaches and hold significant potential for future expansion into event-driven data processing. Through simulations of time-series data prediction tasks, we verified that the neuransistor can serve as an excellent

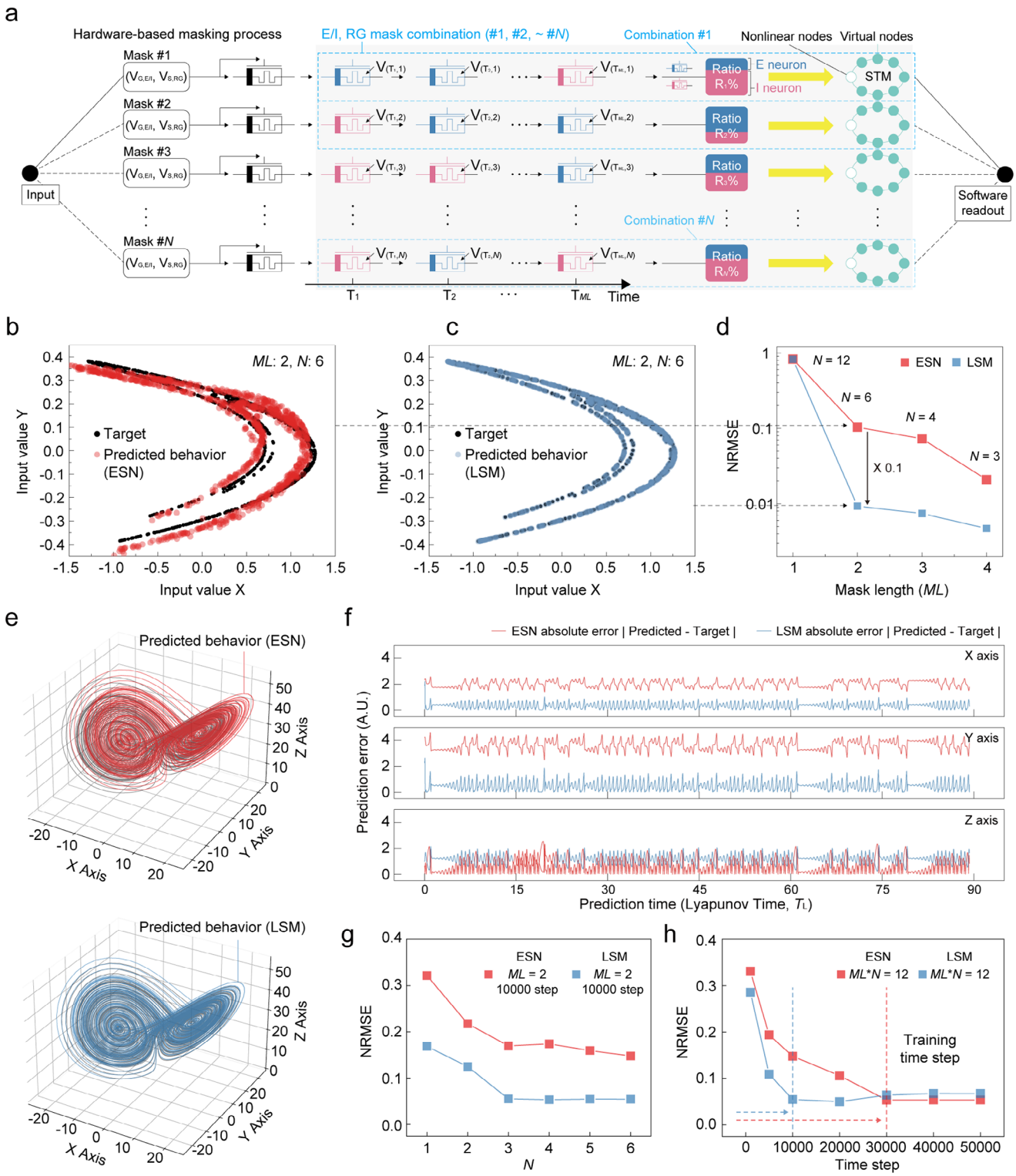

Figure 5. The neuransistor-based LSM simulation. a) Configuration of the reservoir using a 1×*N* neuransistor array with *ML* time-multiplexed input signals. Each *ML* time step is associated with a distinct E/I and RG mask combination, influencing the conductance modulation of the neuransistor array. The E/I ratio at each time step is determined by the E/I mask combination in the reservoir system. b,c) Prediction comparison between the ESN (b) and the LSM (c) using the Henon dataset target. d) NRMSE values for the ESN (red) and LSM (blue) across various *ML* values. e) Predicted 3D state trajectories for the ESN (red, top) and LSM (blue, bottom) using the Lorenz attractor. f) Prediction error values for each axis over time steps for the ESN (red) and LSM (blue). The x-axis represents the prediction time in Lyapunov time units (T_L), where $T_L = 1.12$ seconds, corresponding to approximately 112 time steps in our simulation. g) NRMSE values across various *N* (*ML* = 2, 10 two-dimensional electron000 time steps). h) NRMSE values under varying time step conditions (*ML* = 2, *N* = 6).

reservoir in the LSM, highlighting its potential for more efficient and biologically inspired neuromorphic computing applications.

4. Experimental Section

Device Fabrication: A Pt electrode (40 nm) on a Ti adhesion layer (5 nm) was deposited by e-beam evaporation on a SiO_2/Si substrate for the source and drain. The source and drain patterns were formed via the lift-off process. Next, the TiO_{2-x} layer (≈10 nm) was deposited by plasma-enhanced atomic layer deposition (PEALD) at 225 °C using tetrakis(dimethylamido)titanium (TDMATi) and O_2 plasma as the Ti precursor and reactant, respectively. Then, the Al_2O_3 layer (≈6 nm) was deposited by thermal atomic layer deposition (ALD) at 250 °C using trimethylaluminum (TMA) and H_2O as the Al precursor and oxygen source, respectively. Finally, for the top gate, the Ti (40 nm) electrode, followed by the Pt encapsulation layer (20 nm) was deposited by e-beam evaporation. The gate was also patterned via the lift-off process.

Electrical Measurements: The electrical characterization was performed using Keithley 4200A-SCS and a hot chuck controller (MST-1000H) was used for ambient temperature control. The pulse measurements were conducted using Keithley 4200A-SCS. During the measurement, pulse measurement units were connected to the source and gate of the neuransistor while the drain was grounded.

Material Imaging: The cross-section of the device and FFT results were obtained using a field emission transmission electron microscope (FE-TEM) (Titan cubed G2 60–300).

Reservoir Computing Emulation: To implement the neuransistor's characteristics in software-based emulation, its short-term characteristics were modeled by exponential, nonlinear curve fitting as follows.

$$G_{P,t} = G_{P,t-1} \exp\left(-\frac{T}{\tau_P}\right) + G_{sat}\left(1 - \exp\left(-\frac{T}{\tau_P}\right)\right) \quad (1)$$

represents potentiation by $V_{G,pgm}$, and

$$G_{R,t} = G_{R,t-1} \exp\left(-\frac{T}{\tau_R}\right) + G_0\left(1 - \exp\left(-\frac{T}{\tau_R}\right)\right) \quad (2)$$

represents relaxation. Equations (1) and (2) describe the change in conductance from time $t-1$ to time t for both $G_{P,t}$ and $G_{R,t}$, based on a unit time T, where τ_P and τ_R denote the time constants for potentiation and relaxation, respectively. The unit time T includes the interval between $V_{G,pgm}$ and subsequent pulses, considering the operational scheme of the neuransistor. Consequently, the term G_{sat} in potentiation represents the saturation conductance in Figure 2e as a function proportional to the magnitude of the input pulse voltage (see Figure S14, Supporting Information, for the detailed fitting results of computing emulation).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2DEG, charge trapping, liquid state machine, memtransistor, reservoir computing

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[1] M. S. Bretscher, M. C. Raff, *Nature* **1975**, *258*, 43.
[2] E. T. Kavalali, *Nat. Rev. Neurosci.* **2015**, *16*, 5.
[3] N. C. Spitzer, *Nat. Rev. Neurosci.* **2012**, *13*, 94.
[4] R. A. Nicoll, *Science* **1988**, *241*, 545.
[5] M. Segal, *Nat. Rev. Neurosci.* **2005**, *6*, 277.
[6] D. M. Kullmann, K. P. Lamsa, *Nat. Rev. Neurosci.* **2007**, *8*, 687.
[7] M. Galarreta, S. Hestrin, *Nat. Rev. Neurosci.* **2001**, *2*, 425.
[8] H. C. Hartzell, *Nature* **1981**, *291*, 539.
[9] W. Rall, *Exp. Neurol.* **1960**, *2*, 503.
[10] J. F. Storm, *J. Physiol.* **1987**, *385*, 733.
[11] S. Denève, C. K. Machens, *Nat. Neurosci.* **2016**, *19*, 375.
[12] C. Van Vreeswijk, H. Sompolinsky, *Science* **1996**, *274*, 1724.
[13] N. Brunel, *J. Comput. Neurosci.* **2000**, *8*, 183.
[14] Y. Shu, A. Hasenstaub, D. A. McCormick, *Nature* **2003**, *423*, 288.
[15] W. Maass, in *Computability in Context: Computation and Logic in the Real World* (Eds: S. B. Cooper, A. Sorbi), Imperial College Press, London, UK **2011**, p. 275.
[16] W. Maass, T. Natschläger, H. Markram, *Neural Comput.* **2002**, *14*, 2531.
[17] D. V. Buonomano, W. Maass, *Nat. Rev. Neurosci.* **2009**, *10*, 113.
[18] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, H.-S. P. Wong, *IEEE Trans. Electron Devices* **2011**, *58*, 2729.
[19] Z. Wang, M. Yin, T. Zhang, Y. Cai, Y. Wang, Y. Yang, R. Huang, *Nanoscale* **2016**, *8*, 14015.
[20] W. Huh, D. Lee, S. Jang, J. H. Kang, T. H. Yoon, J.-P. So, Y. H. Kim, J. C. Kim, H.-G. Park, H. Y. Jeong, G. Wang, C.-H. Lee, *Adv. Mater.* **2023**, *35*, 2211525.
[21] T. Chang, S.-H. Jo, W. Lu, *ACS Nano* **2011**, *5*, 7669.
[22] S. Yun, C. Mahata, M.-H. Kim, S. Kim, *Appl. Surf. Sci.* **2022**, *579*, 152164.
[23] S. G. Sarwat, B. Kersting, T. Moraitis, V. P. Jonnalagadda, A. Sebastian, *Nat. Nanotechnol.* **2022**, *17*, 507.
[24] X. Zhang, S. Liu, X. Zhao, F. Wu, Q. Wu, W. Wang, R. Cao, Y. Fang, H. Lv, S. Long, Q. Liu, M. Liu, *IEEE Electron Device Lett.* **2017**, *38*, 1208.
[25] S. Luo, K. Liao, P. Lei, T. Jiang, S. Chen, Q. Xie, W. Luo, W. Huang, S. Yuan, W. Jie, J. Hao, *Nanoscale* **2021**, *13*, 6654.
[26] S.-O. Park, H. Jeong, J. Park, J. Bae, S. Choi, *Nat. Commun.* **2022**, *13*, 2888.
[27] S. Chen, T. Zhang, S. Tappertzhofen, Y. Yang, I. Valov, *Adv. Mater.* **2023**, *35*, 2301924.
[28] G. Kim, J. H. In, Y. Lee, H. Rhee, W. Park, H. Song, J. Park, J. B. Jeon, T. D. Brown, A. A. Talin, S. Kumar, K. M. Kim, *Nat. Mater.* **2024**, *23*, 1237.

[29] T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, B. Linares-Barranco, *Front. Neurosci.* **2013**, *7*, 2.
[30] G. Kim, Y. Lee, J. B. Jeon, W. H. Cheong, W. Park, H. Song, K. M. Kim, *Adv. Mater.* **2023**, *35*, 2304148.
[31] X. Liang, Y. Zhong, X. Li, H. Huang, T. Li, J. Tang, B. Gao, H. Qian, H. Wu, H. Heidari, in 2022 29th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS), IEEE, Glasgow, UK **2022**, p. 1–4.
[32] Y. Zhong, J. Tang, X. Li, B. Gao, H. Qian, H. Wu, *Nat. Commun.* **2021**, *12*, 408.
[33] Y. Zhong, J. Tang, X. Li, X. Liang, Z. Liu, Y. Li, Y. Xi, P. Yao, Z. Hao, B. Gao, *Nat. Electron.* **2022**, *5*, 672.
[34] T. J. Seok, Y. Liu, H. J. Jung, S. B. Kim, D. H. Kim, S. M. Kim, J. H. Jang, D.-Y. Cho, S. W. Lee, T. J. Park, *ACS Nano* **2018**, *12*, 10403.
[35] T. J. Seok, Y. Liu, J. H. Choi, H. J. Kim, D. H. Kim, S. M. Kim, J. H. Jang, D.-Y. Cho, S. W. Lee, T. J. Park, *Chem. Mater.* **2020**, *32*, 7662.
[36] Y. Chen, N. Pryds, J. E. Kleibeuker, G. Koster, J. Sun, E. Stamate, B. Shen, G. Rijnders, S. Linderoth, *Nano Lett.* **2011**, *11*, 3774.
[37] C. Di Valentin, G. Pacchioni, A. Selloni, *J. Phys. Chem. C* **2009**, *113*, 20543.
[38] K. Liu, T. Zhang, B. Dang, L. Bao, L. Xu, C. Cheng, Z. Yang, R. Huang, Y. Yang, *Nat. Electron.* **2022**, *5*, 761.
[39] M. Farronato, P. Mannocci, M. Melegari, S. Ricci, C. M. Compagnoni, D. Ielmini, *Adv. Mater.* **2023**, *35*, 2205381.
[40] K. M. Kim, J. Zhang, C. Graves, J. J. Yang, B. J. Choi, C. S. Hwang, Z. Li, R. S. Williams, *Nano Lett.* **2016**, *16*, 6724.
[41] J. H. Yoon, S. J. Song, I. H. Yoo, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park, C. S. Hwang, *Adv. Funct. Mater.* **2014**, *24*, 5086.
[42] J. H. Yoon, K. M. Kim, S. J. Song, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park, Y. J. Kwon, X. Shao, C. S. Hwang, *Adv. Mater.* **2015**, *27*, 3811.
[43] G. Kim, S. Son, H. Song, J. B. Jeon, J. Lee, W. H. Cheong, S. Choi, K. M. Kim, *Adv. Sci.* **2023**, *10*, 2205654.
[44] K. M. Kim, B. J. Choi, M. H. Lee, G. H. Kim, S. J. Song, J. Y. Seok, J. H. Yoon, S. Han, C. S. Hwang, *Nanotechnology* **2011**, *22*, 254010.
[45] K. M. Kim, S. Han, C. S. Hwang, *Nanotechnology* **2012**, *23*, 035201.
[46] M. Ramamoorthy, R. King-Smith, D. Vanderbilt, *Phys. Rev. B* **1994**, *49*, 7709.
[47] R. E. Rex, Y. Yang, F. J. Knorr, J. Z. Zhang, Y. Li, J. L. McHale, *J. Phys. Chem. C* **2016**, *120*, 3530.
[48] C. Di Valentin, G. Pacchioni, A. Selloni, *J. Phys. Chem. C* **2009**, *113*, 20543.
[49] S. Wendt, P. T. Sprunger, E. Lira, G. K. H. Madsen, Z. Li, J. Ø. Hansen, J. Matthiesen, A. Blekinge-Rasmussen, E. Lægsgaard, B. Hammer, F. Besenbacher, *Science* **2008**, *320*, 1755.
[50] G. Mattioli, F. Filippone, P. Alippi, A. A. Bonapasta, *Phys. Rev. B* **2008**, *78*, 241201.
[51] M. H. Lee, K. M. Kim, G. H. Kim, J. Y. Seok, S. J. Song, J. H. Yoon, C. S. Hwang, *Appl. Phys. Lett.* **2010**, *96*, 152909.
[52] E. W. Lim, R. Ismail, *Electronics* **2015**, *4*, 586.
[53] M. Barahona, C.-S. Poon, *Nature* **1996**, *381*, 215.
[54] X. Liang, J. Tang, Y. Zhong, B. Gao, H. Qian, H. Wu, *Nat. Electron.* **2024**, *7*, 193.
[55] J. Cao, X. Zhang, H. Cheng, J. Qiu, X. Liu, M. Wang, Q. Liu, *Nanoscale* **2022**, *14*, 289.
[56] M. Cucchi, S. Abreu, G. Ciccone, D. Brunner, H. Kleemann, *Neuromorphic Comput. Eng.* **2022**, *2*, 032002.
[57] K. Liu, T. Zhang, B. Dang, L. Bao, L. Xu, C. Cheng, Z. Yang, R. Huang, Y. Yang, *Nat. Electron.* **2022**, *5*, 761.
[58] W. Ponghiran, G. Srinivasan, K. Roy, *Front. Neurosci.* **2019**, *13*, 883.
[59] P. Wijesinghe, G. Srinivasan, P. Panda, K. Roy, *Front. Neurosci.* **2019**, *13*, 504.
[60] W. Tucker, *C. R. Acad. Sci.,-Ser. I-Math.* **1999**, *328*, 1197.
[61] L.-W. Kong, G. A. Brewer, Y.-C. Lai, *Nat. Commun.* **2024**, *15*, 4840.
[62] J. Z. Kim, Z. Lu, E. Nozari, G. J. Pappas, D. S. Bassett, *Nat. Mach. Intell.* **2021**, *3*, 316.
[63] N. Lin, S. Wang, Y. Li, B. Wang, S. Shi, Y. He, W. Zhang, Y. Yu, Y. Zhang, X. Zhang, K. Wong, S. Wang, X. Chen, H. Jiang, X. Zhang, P. Lin, X. Xu, X. Qi, Z. Wang, D. Shang, Q. Liu, M. Liu, *Nat. Comput. Sci.* **2025**, *5*, 37.