



Article

# Fabrication of Low Cost and Low Temperature Poly-Silicon Nanowire Sensor Arrays for Monolithic Three-Dimensional Integrated Circuits Applications

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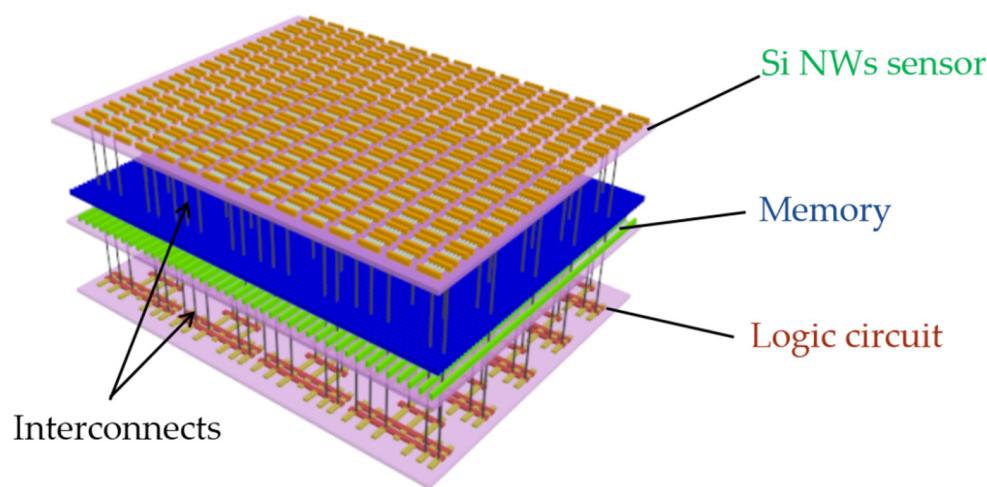
**Abstract:** In this paper, the poly-Si nanowire (NW) field-effect transistor (FET) sensor arrays were fabricated by adopting low-temperature annealing (600 °C/30 s) and feasible spacer image transfer (SIT) processes for future monolithic three-dimensional integrated circuits (3D-ICs) applications. Compared with other fabrication methods of poly-Si NW sensors, the SIT process exhibits the characteristics of highly uniform poly-Si NW arrays with well-controlled morphology (about 25 nm in width and 35 nm in length). Conventional metal silicide and implantation techniques were introduced to reduce the parasitic resistance of source and drain (SD) and improve the conductivity. Therefore, the obtained sensors exhibit  $>10^6$  switching ratios and 965 mV/dec subthreshold swing (SS), which exhibits similar results compared with that of SOI Si NW sensors. However, the poly-Si NW FET sensors show the  $V_{th}$  shift as high as about  $178 \pm 1$  mV/pH, which is five times larger than that of the SOI Si NW sensors. The fabricated poly-Si NW sensors with 600 °C/30 s processing temperature and good device performance provide feasibility for future monolithic three-dimensional integrated circuit (3D-IC) applications.

**Keywords:** silicon nanowire (Si NW); monolithic three-dimensional integrated circuits (M3D-ICs); spacer image transfer (SIT); sensitivity

## 1. Introduction

In recent years, the application of semiconductor field-effect transistors (FET) sensors have attracted a lot of attention because of their ability to translate the interaction with target molecules on the FET surface to an electrical signal directly [1–4]. Silicon nanowires (Si NW) sensors have been considered as one of the most promising candidates for biochemical sensors [5–9], due to their large surface to volume (S/V) ratio, high sensitivity, and good biocompatibility [10,11]. In recent years,

Si NW field-effect-transistor (FET) sensors have been used for the very high sensitivity detection of pH [12–14], gases [15–17] and DNA [18–20]. However, the conventional fabrication process with silicon-on-insulator (SOI) materials is complex and high-cost, and the nanometer patterns are usually formed by traditional low-efficiency electron beam lithography (EBL) process, which does not meet the demands of future mass production with a low cost and low efficiency. The spacer image transfer (SIT) process (also named self-aligned double or quadruple patterning) could achieve nanometer array with high efficiency and low cost, which are widely used in foundries [21–23]. In addition, there are no reports on the design or fabrication of Si NW sensors for monolithic three-dimensional integrated circuits (3D-ICs) application, which is one of the most convincing candidates for future application (see Figure 1). In order to achieve better performance of the system, the fabrication of top devices (Si NW sensor) usually need low-temperature processes to avoid a degradation on characteristics of bottom circuits (logic circuits and memory in Figure 1) [24]. However, there are no reports on the design or fabrication of Si NW sensor for monolithic 3D-ICs application.



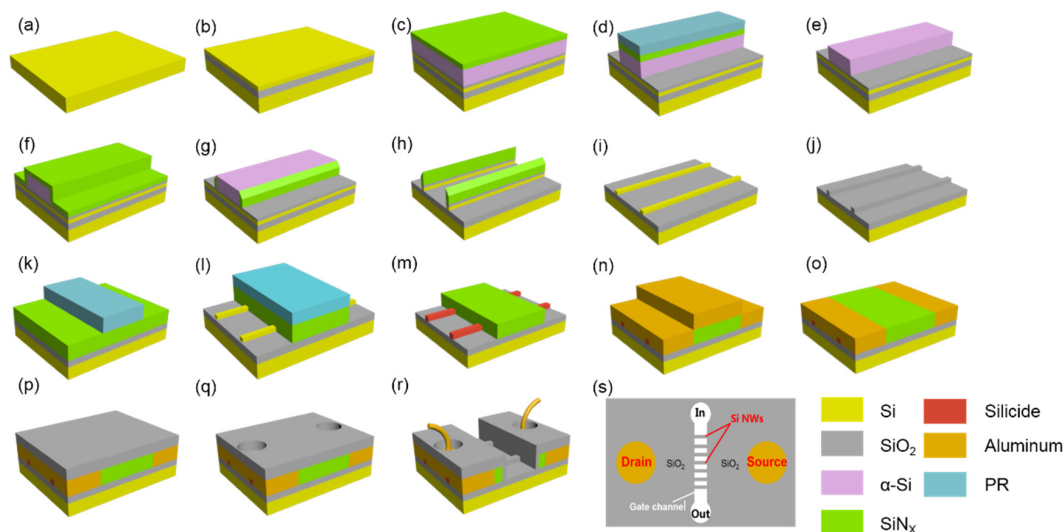
**Figure 1.** Illustration of monolithic three-dimensional integrated circuits (3D-ICs): bottom logic circuits; middle memory and top silicon nanowire (Si NW) sensors.

In this paper, poly-silicon NW sensors with low cost and high efficiency are designed and fabricated using advanced spacer image transfer (SIT) [22–24] and low-temperature silicide techniques for monolithic 3D-IC application. The highest annealing temperature is not over 600 °C, which overcomes the problems of overheating the bottom transistor and the wires. The achieved poly-silicon NW sensors have good electrical properties, such as over six orders of magnitude in on-off ratio and 932 mV/dec of subthreshold swing (SS) by bias back-gate voltages.

## 2. Materials and Methods

Two types of Si NW sensors (poly-silicon and silicon-on-insulator (SOI)) were designed and fabricated, and the detailed fabrication flow is illustrated in Figure 2. The poly-silicon NW sensors were manufactured on p-type 200 mm Si (100) silicon wafers (see Figure 2a): Firstly, 145 nm SiO<sub>2</sub> and 40 nm poly-silicon were deposited, respectively (see Figure 2b). The SOI Si NW sensors were manufactured on 200 mm SOI wafers featured with a 145-nm-thick buried oxide layer (BOX) and a 40-nm-thick top silicon layer. The fabrication process of the two types of devices was all the same in the following steps. During the fabrication of the Si NWs, a spacer image transfer (SIT) technology was chosen to form NW arrays patterns with high efficiency [25–27], and the detailed fabrication process flow is described as follows: sequential multi-layer SiO<sub>2</sub>/amorphous Si ( $\alpha$ -Si)/Si<sub>3</sub>N<sub>4</sub> films were deposited (see Figure 2c). Next, the conventional photolithography process (i-line) and dry etching processes were used to form rectangular arrays of Si<sub>3</sub>N<sub>4</sub> and  $\alpha$ -Si films (see Figure 2d). The top Si<sub>3</sub>N<sub>4</sub> hard masks (HMs) were removed by a hot H<sub>3</sub>PO<sub>4</sub> solution at 140 °C (see Figure 2e). A 30 nm Si<sub>3</sub>N<sub>4</sub> film was deposited by

plasma-enhanced chemical vapor deposition (PECVD) approach and then the corresponding  $\text{Si}_3\text{N}_4$  reactive ion etching (RIE) was performed to form two  $\text{SiN}_x$  spacers on both sides of  $\alpha$ -Si (see Figure 2f,g). The  $\alpha$ -Si material between two  $\text{Si}_3\text{N}_4$  spacers was removed by tetramethylammonium hydroxide (TMAH) (see Figure 2h). In order to obtain Si NW arrays, dry etching processes of  $\text{SiO}_2$  and Si were carried out, respectively (see Figure 2h). Afterward, the top HMs were removed using hot phosphoric acid and diluted hydrofluoroacid (DHF) solution, respectively (see Figure 2i). After the Si NW formation, a 5-nm-thick  $\text{SiO}_2$  was deposited on the Si NW followed by the deposition of a thick layer of  $\text{Si}_3\text{N}_4$  (see Figure 2j,k). The  $\text{Si}_3\text{N}_4$  film was etched by dry etching processes. A nickel platinum alloy ( $\text{Ni}_{0.95}\text{Pt}_{0.05}$ ) was used to form metal silicide in the source and drain regions to reduce the parasitic of Si nanowires (see Figure 2l,m). Afterward,  $\text{BF}^{2+}$  ions with a heavy dose and low energy were implanted into the top silicided Si NWs and activated by low temperature rapid thermal annealing (RTA) to form Schottky barrier source and drain (SBSD) (about  $600\text{ }^\circ\text{C}/30\text{ s}$  annealing). For a better combination, the aluminum electrode was prepared by a sputtering process and the RIE process was performed (see Figure 2n,o). Subsequently, a layer of thick  $\text{SiO}_2$  was deposited, and the source drain contact holes were opened by photolithography and etching processes (see Figure 2p,q). Finally, the gate with different channel lengths (5, 10 and  $15\text{ }\mu\text{m}$ ) was defined by photolithography and the open gate trench of the sensor to expose the sensitive area was achieved by RIE processes. The bounding of SD contact was carried out and a layer of 20-nm-thick  $\text{HfO}_2$  was deposited on the surface of the device (see Figure 2r). Figure 2s is a schematic top view of the device. Except for the source drain and gate trench of the devices, other areas were covered by a thick  $\text{SiO}_2$ , which helps to improve the stability and reliability of the solution.



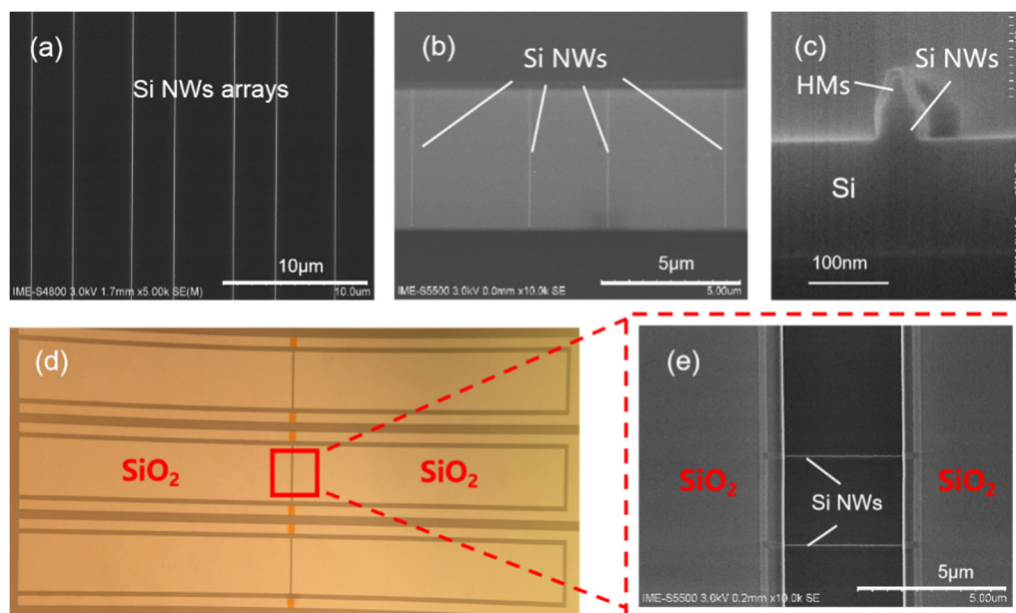
**Figure 2.** Fabrication flow of Si NW sensors. (a) 200 mm a p-type (100) silicon wafers, (b) deposition of  $\text{SiO}_2$  and  $\alpha$ -Si films, (c) deposition of multi-layer  $\text{SiO}_2/\alpha$ -Si/ $\text{Si}_3\text{N}_4$  films, (d) conventional lithography and reactive ion etching (RIE) of  $\text{Si}_3\text{N}_4/\alpha$ -Si, (e) removal of photoresist (PR) and  $\text{Si}_3\text{N}_4$  hard mask, (f) deposited of  $\text{Si}_3\text{N}_4$  thin film, (g) anisotropic RIE of  $\text{Si}_3\text{N}_4$  to form nanometer  $\text{Si}_3\text{N}_4$  spacers, (h) remove the  $\alpha$ -Si and RIE  $\text{SiO}_2$  and Si films, (i) removal of top hard masks (HMs), (j) deposition of 5 nm  $\text{SiO}_2$  film, (k) deposition of  $\text{Si}_3\text{N}_4$  and i-line lithography, (l) RIE of  $\text{Si}_3\text{N}_4$ , (m) RIE of  $\text{Si}_3\text{N}_4$  and forms metal silicide, (n) sputter metal, (o) RIE of metal, (p) deposition of  $\text{HfO}_2$  film, (q) formation of source and drain contact hole, (r) formation of Si NW channel and bonding and (s) top view of the designed Si NW sensors.

The cross-sectional views and top views of the device's structures were observed using S-5500 and S-4800 scanning electron microscopes (SEM, Hitachi, Tokyo, Japan), respectively. The cross-sectional profiles of the final device were performed using transmission electron microscopy (TEM, FEI Talos, Brno, Czech) and energy-dispersive X-ray spectroscopy (EDX, FEI Talos, Brno, Czech). The electrical

characterization was performed using a B1500A (Keysight, Santa Rosa, CA, USA) semiconductor parameter analyzer.

### 3. Results and Discussion

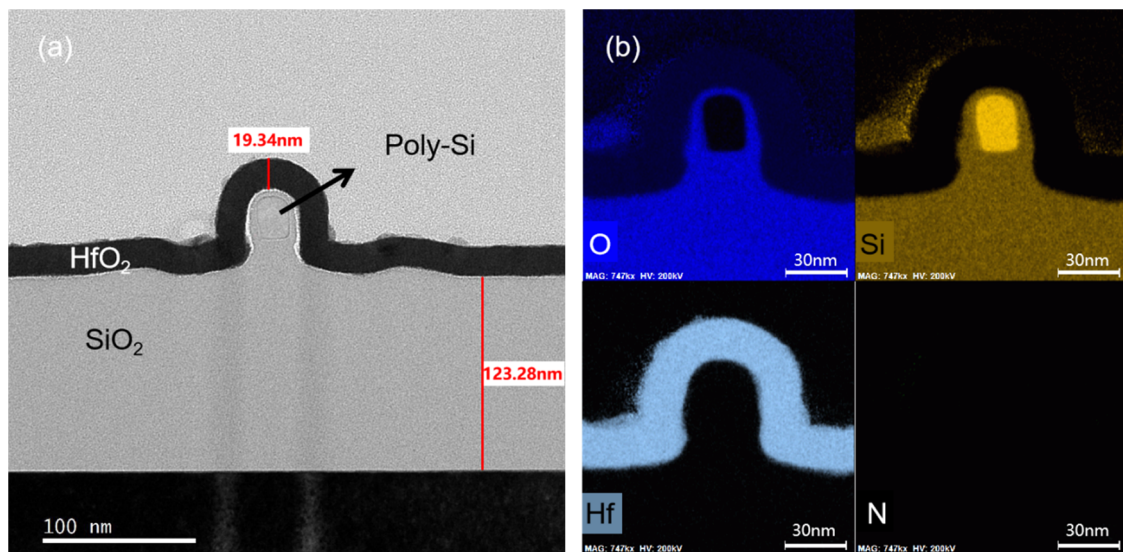
The images of the fabricated poly-Si NWs sensors by the SIT process are shown in Figure 3. Figure 3a,b shows top views of poly-Si NW arrays by SEM measurement. As can be seen from the images, highly uniform poly-Si NW arrays without any landing pads are achieved. The achieved poly-Si NW arrays using the SIT approach have high efficiency, low cost and smaller sizes compared with that of fabricated using the EBL process. Figure 3c shows a cross-sectional view of poly-Si NWs. Contrasted with previous work [28,29], the dimensions and the morphology of the fabricated Si NW arrays are well controlled and extraordinarily small, theoretically providing higher sensitivity for the fabricated poly-Si NW sensor. Figure 3d,e shows top views of poly-Si NW sensors arrays. The length of the electrode is 2 mm; the gate lengths ( $L_{GS}$ ) of poly-Si NW FETs are 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , and 15  $\mu\text{m}$ , respectively. The sensor current is increased and the device's variations are reduced for the multi-channel poly-Si NW sensors.



**Figure 3.** Images of poly-Si NW sensors. (a,b) SEM images of poly-Si NW array in top view, (c) cross-sectional SEM image of poly-Si NWs, (d) top view of poly-Si NW arrays sensor by optical microscope, (e) SEM image of the final poly-Si NW arrays sensor in top view.

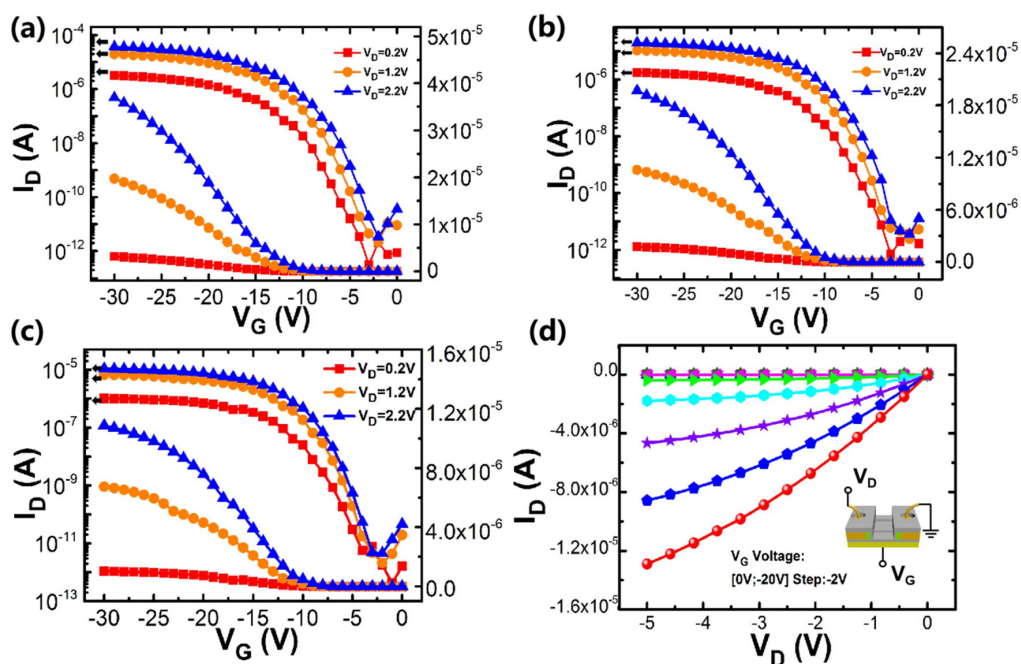
Figure 4 shows the cross-sectional TEM image and the electron scattering spectrum (EDS) elemental mappings of the poly-Si NWs channel. According to the TEM image, the thicknesses of  $\text{HfO}_2/\text{SiO}_2$  layers are 19.34 nm and 5.25 nm, respectively. The sizes of the well-controlled regular rectangle poly-Si NW is about 25 nm in width and 35 nm in length. Furthermore, the EDS analysis of Hf, O, poly-Si, and N elements demonstrates that the  $\text{HfO}_2$  and  $\text{SiO}_2$  films are very uniform and the interfaces are clear and flat without inter-diffusion. The well-controlled insulation layer could reduce the leakage current from liquid to device, providing a robust detection environment in the liquid.

Initial measurements of transfer and output curves ( $I_D-V_G$  and  $I_D-V_D$ ) were performed by applying a bias gate voltage. In the measurement of the  $I_D-V_G$  curve,  $I_D$  was measured at constant drain voltages ( $V_D = -0.2 \text{ V}, -1.2 \text{ V}, -2.2 \text{ V}$ ), and the gate voltage was swept from 0 to  $-30 \text{ V}$ . In the measurement of the  $I_D-V_D$  curves, the drain current was measured at constant gate voltages ( $V_G$  from 0 to  $-20 \text{ V}$  with a  $-2 \text{ V}$  step), and the  $V_D$  was swept from 0 to  $-5 \text{ V}$  with a  $-0.2 \text{ V}$  step.



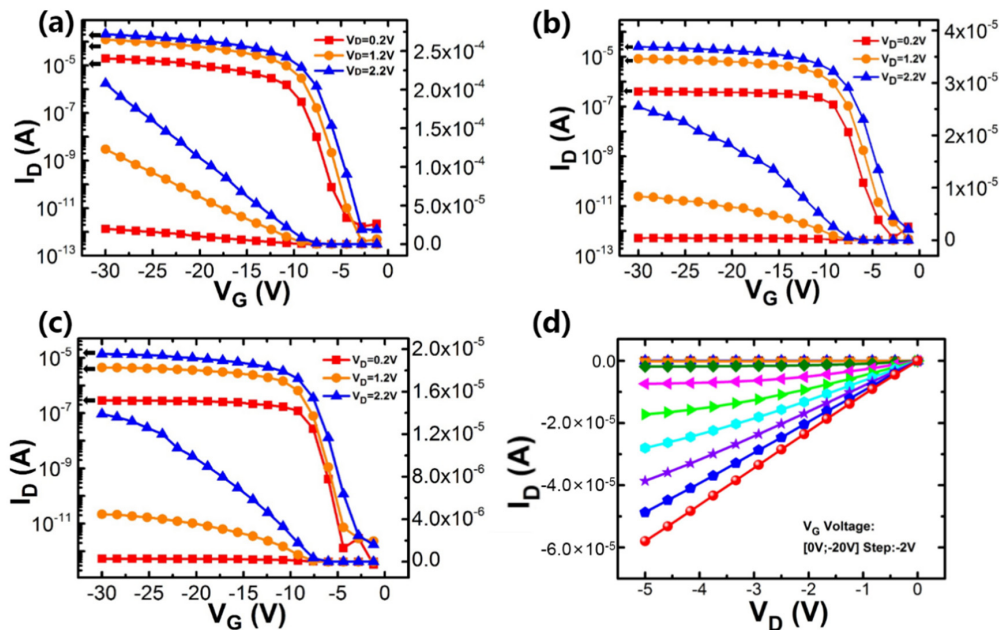
**Figure 4.** (a) TEM image of poly-Si NW channel of the device, (b) EDS elemental mappings of O, Si, Hf and N, respectively.

The  $I_D$ - $V_G$  and  $I_D$ - $V_D$  curves by bias gate voltages of the p-type poly-Si NW sensors are shown in Figure 5. Figure 5a–c shows typical  $I_D$ - $V_G$  curves of 5- $\mu\text{m-L}_G$ , 10- $\mu\text{m-L}_G$  and 15- $\mu\text{m-L}_G$  poly-Si NW devices, respectively. As can be seen from the images, smooth and uniform p-type MOSFET curves were achieved for the sensors fabricated at low temperature. The  $I_{\text{on}}/I_{\text{off}}$  ratios of poly-Si NW devices with the 5- $\mu\text{m-L}_G$ , 10- $\mu\text{m-L}_G$  and 15- $\mu\text{m-L}_G$  are  $5.68 \times 10^6$ ,  $2.84 \times 10^6$  and  $2.31 \times 10^6$ , respectively. The corresponding extracted values of subthreshold swing (SS) are estimated to be 1070 mV/dec, 965 mV/dec and 956 mV/dec, respectively. Figure 5d depicts the  $I_D$ - $V_D$  curves of poly-Si NW device 10- $\mu\text{m-L}_G$ . The drain current increases with increasing  $V_G$  bias, implying that the carrier's concentration inside Si NWs can be linearly adjusted, and devices prepared at low temperatures exhibit good FET electrical performance.



**Figure 5.** (a–c)  $I_D$ - $V_G$  curves of the fabricated 5- $\mu\text{m-L}_G$ , 10- $\mu\text{m-L}_G$  and 15- $\mu\text{m-L}_G$  p-type poly-Si NW sensors by back bias gate voltage, (d) typical  $I_D$ - $V_D$  of the fabricated 10- $\mu\text{m-L}_G$  p-type poly-Si NW sensors.

The  $I_D$ - $V_G$  and  $I_D$ - $V_D$  curves of the SOI Si NW for 5- $\mu\text{m}$ - $L_G$ , 10- $\mu\text{m}$ - $L_G$  and 15- $\mu\text{m}$ - $L_G$  are shown in Figure 6, respectively. As can be seen from the images, smooth p-type MOSFET curves are achieved for the sensors fabricated at low temperature. The  $I_{\text{on}}/I_{\text{off}}$  ratios of 5- $\mu\text{m}$ - $L_G$ , 10- $\mu\text{m}$ - $L_G$  and 15- $\mu\text{m}$ - $L_G$  SOI Si NW devices are  $1.47 \times 10^8$ ,  $1.29 \times 10^7$  and  $6.34 \times 10^4$ , respectively, and extracted values of SSs are estimated to be 686 mV/dec, 767 mV/dec and 1120 mV/dec, respectively. Figure 6d depicts the  $I_D$ - $V_D$  curves of the 10- $\mu\text{m}$ - $L_G$  poly-Si NW device.



**Figure 6.** (a–c) typical  $I_D$ - $V_G$  curves of the fabricated 5- $\mu\text{m}$ - $L_G$ , 10- $\mu\text{m}$ - $L_G$  and 15- $\mu\text{m}$ - $L_G$  p-type SOI Si NW sensors by back gate bias, respectively, (d) typical  $I_D$ - $V_D$  curves of the fabricated 10- $\mu\text{m}$ - $L_G$  p-type SOI Si NW sensors.

Figure 7 shows the extracted typical parameter comparison between the poly-Si NW and SOI Si NW sensors, e.g., the threshold voltage ( $V_{\text{th}}$ ), SS, on-stage current ( $I_{\text{on}}$ ) and  $I_{\text{on}}/I_{\text{off}}$  ratio, respectively. The  $V_{\text{th}}$ s of 5- $\mu\text{m}$ - $L_G$ , 10- $\mu\text{m}$ - $L_G$  and 15- $\mu\text{m}$ - $L_G$  poly-Si NW devices are  $-8.06$  V,  $-8.125$  V and  $-7.87$  V, respectively. The  $V_{\text{th}}$  of 5- $\mu\text{m}$ - $L_G$ , 10- $\mu\text{m}$ - $L_G$  and 15- $\mu\text{m}$ - $L_G$  SOI Si NW devices are  $-7.67$  V,  $-7.95$  V and  $-7.8$  V, respectively. The values of  $V_{\text{th}}$ s of poly-silicon devices with different  $L_G$ s are similar to those of the SOI devices. The values of SSs of SOI devices are smaller than those of poly-Si devices and the  $I_{\text{on}}/I_{\text{off}}$  is also larger. The performance of SOI devices is slightly better than that of low-temperature poly-silicon devices, which is caused by the monocrystalline silicon channel with a low channel resistance. The achieved results imply that the poly-Si NW sensors could be applied for future monolithic 3D-IC application.

Figure 8 shows the typical sensing characteristics of the poly-silicon nanowire sensors by analyzing different stranded pH solutions. In the measurement of the  $I_D$ - $V_G$  curve and the gate voltage was swept from 0 to  $-10$  V by top solution (see Figure 8a inserted image). The detection principle is to convert the sensor surface potential change introduced by a different pH solution into the current change in the semiconductor Si NW channel. The actual amount of charges depends on the concentration of specific ions in the solution (the concentration of  $\text{H}^+$  ion in the manuscripts). Therefore, the pH of the solutions could modulate the surface charge of the insulator/semiconducting interface consequently, resulting in a shift of the threshold voltage. The scheme of the test using the top liquid gate is shown in the inserted figure of Figure 8a. Due to the change of film surface potential of the channel, the poly-silicon nanowire sensors exhibit  $V_{\text{th}}$  shifts (see Figure 8a). If the added solution is acidic (alkaline), the  $I_D$ - $V_G$  curve will shift to the right (left). After adding different pH buffers, the real-time response of  $I_D$  is shown in Figure 8b. Taking the buffer solution with pH = 7 as a reference, when the pH buffer is acidic, a positive

charge is introduced and the current of the p-type poly-silicon nanowire sensor increases. When the pH buffer is alkaline, a negative charge is introduced and the current decreases. The results are consistent with the transfer curve of the p-type poly-silicon nanowire sensor increases. The extracted change values of  $V_{th}$  and  $I_D$  as a function of pH values are shown in Figure 8c,d, respectively. The changes of  $V_{th}$  and  $I_D$  have approximate linearity with the pH values, and the sensitivity as high as about  $178 \pm 1$  mV/pH, which is caused by the small size in Si NW and large surface to volume ratio.

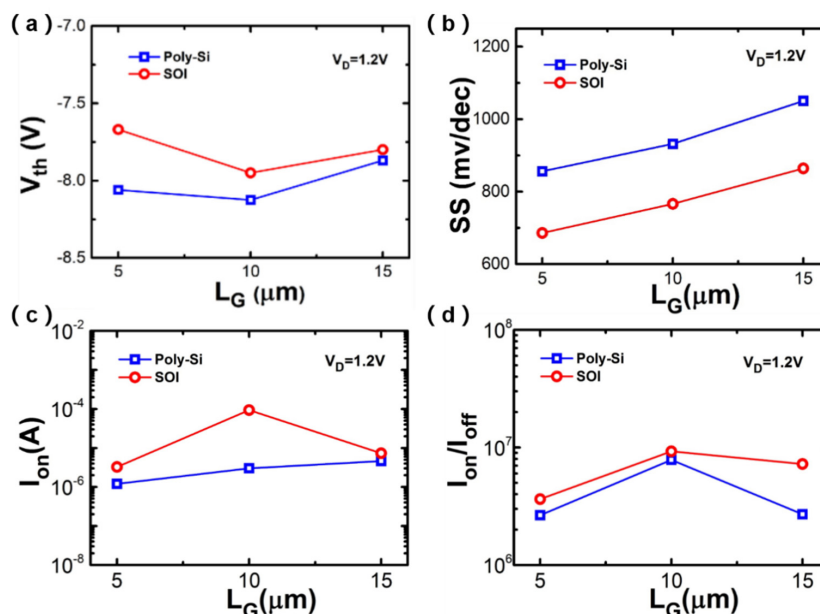


Figure 7. Comparison between low-temperature poly-silicon devices and SOI Si NW devices. (a) SS, (b)  $V_{th}$ , (c)  $I_{on}$  and (d)  $I_{on}/I_{off}$  ratio.

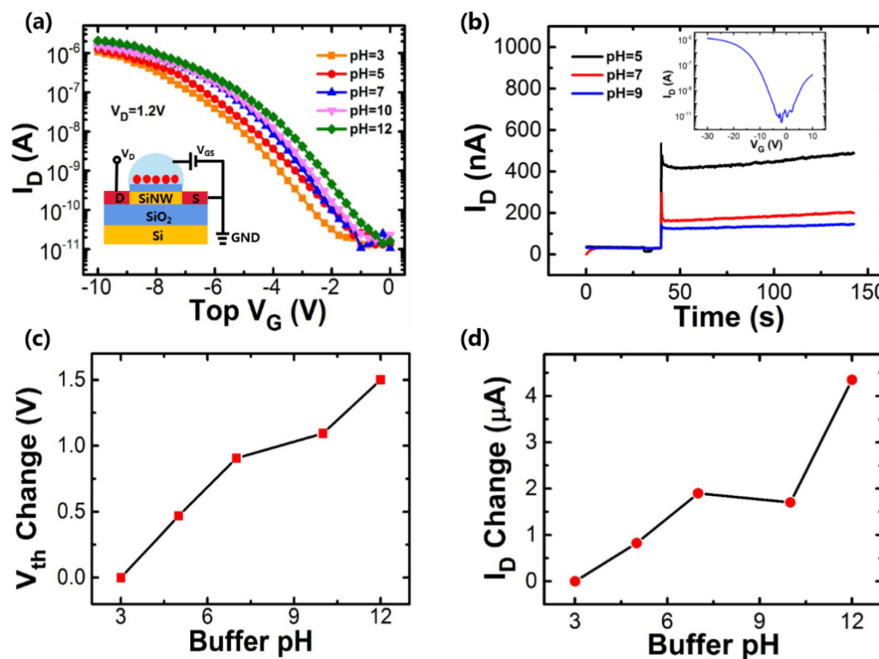
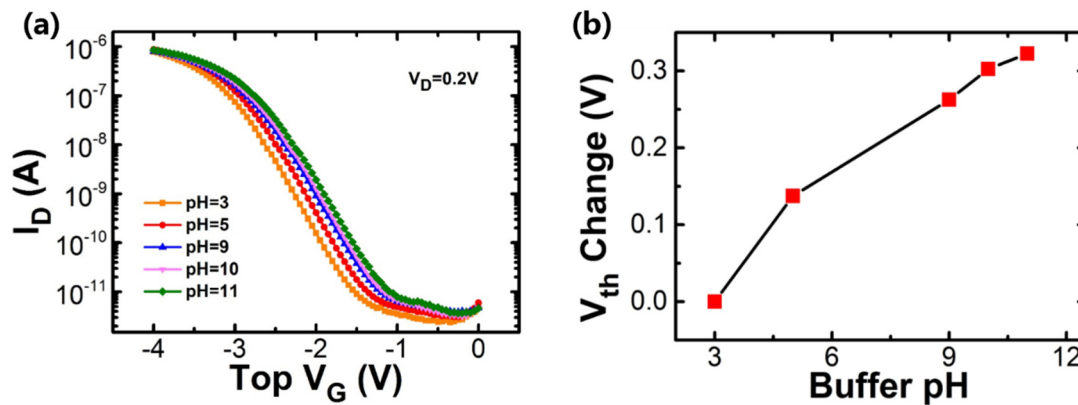


Figure 8. (a) The transfer curves of the poly-Si NW sensor by analyzing different pH solutions, (b) real-time response of  $I_D$  when adding different pH solutions, the inserted figure the transfer curves of the bias back gate voltage, (c,d) threshold voltage and drain current change under different pH solutions.

Figure 9 shows the typical sensing characteristics of the SOI nanowire sensors by analyzing different stranded pH solutions. In the measurement of the  $I_D$ - $V_G$  curve, the gate voltage was swept from 0 to  $-4$  V by the top solution. Figure 9a shows that the threshold voltage shifts with the pH of the solution. The extracted threshold change is linear with the pH of the solution (see Figure 9b). A similar trend of  $V_{th}$  shift is obtained, but the values of changes are only about a fifth of the poly-silicon nanowire.



**Figure 9.** (a) The transfer curves of the silicon-on-insulator (SOI) sensor with different pH solutions, (b) threshold voltage under different pH solutions.

Table 1 shows system parameters comparison of the relevant reported results in recent years and our fabricated poly-silicon nanowire sensors. The SIT technique is used to form poly-silicon NW sensor arrays with 25 nm in width and 35 nm in length, which exhibits high efficiency and low cost than that of formed by EBL. Furthermore, the resistance and the device performance- the poly-silicon NW sensor is greatly improved by introducing SBSB techniques, which is attributed to achieve a larger  $I_{on}/I_{off}$  ratio and smaller values of SSs. The results indicate that the poly-silicon NWs sensor fabricated by low-temperature annealing has much better characteristics than those of the sensors prepared by other methods, which attributed to its application for future monolithic 3D-IC applications.

**Table 1.** A comparison of silicon nanowire sensors in recent years.

	2011 [30]	2012 [31]	2014 [32]	2016 [33]	2020 [34]	This Work	
Insulation material	SiO <sub>2</sub>	SiN <sub>x</sub>	SiO <sub>2</sub>	SiO <sub>2</sub> /Si <sub>3</sub> N <sub>4</sub>	SiO <sub>2</sub> /Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub>	SiO <sub>2</sub>	SOI
Insulation thickness	100 nm	-	80 nm	50/65 nm	-/150/7 nm	145 nm	
NWs material	Si	Si	poly-Si	poly-Si	poly-Si	poly-Si	Si
Si NWs fabrication approach	VLS	RIE	sidewall spacer	RIE	EBL	SIT	SIT
Processing temperature	-	-	-	600 °C	1050 °C	600 °C	600 °C
NWs size	~90 nm	-	-	~40 nm	40~50 nm	~30 nm	~30 nm
L <sub>G</sub>	-	-	100 nm	10 μm	400 nm	10 μm	10 μm
I <sub>on</sub> /I <sub>off</sub>	~10 <sup>5</sup>	~10 <sup>4</sup>	-	2.03 × 10 <sup>5</sup>	2.5 × 10 <sup>5</sup>	2.84 × 10 <sup>6</sup>	1.29 × 10 <sup>7</sup>
SS (mV/dec)	2500	2300–3000	-	975	1030	965	767
V <sub>th</sub> change (V)	-	-	0.087	0.0437	-	0.178	0.0688

#### 4. Conclusions

In summary, low cost poly-Si NW sensors arrays are fabricated through an advanced SIT process with high efficiency than that formed by electron beam lithography, and the morphology of Si NW is well controlled with small sizes. Furthermore, a low-temperature flow (600 °C) with silicide and implantation is designed and carried out. Benefiting from the silicide and isolation processes, the poly-Si NW FET sensors show six orders of magnitude in switching ratio and a SS of 965 mV/dec, which is similar to the counterpart of the SOI Si NW sensor. In addition, the poly-Si NW FET sensors



show the  $V_{th}$  shift as high as about  $178 \pm 1$  mV/pH, which is five times larger than that of the SOI Si NW sensors. Therefore, the design and fabricated poly-Si NW sensor arrays approach provides a good option for its potential application of the monolithic 3D-ICs in the future.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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