




Article

Channel Shape Effects on Device Instability of Amorphous Indium–Gallium–Zinc Oxide Thin Film Transistors

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Abstract: Channel shape dependency on device instability for amorphous indium–gallium–zinc oxide (a-IGZO) thin film transistors (TFTs) is investigated by using various channel shape devices along with systematic electrical characterization including DC I-V characteristics and bias temperature stress tests. a-IGZO TFTs with various channel shapes such as zigzag, circular, and U-type channels are implemented and their vertical and lateral electric field stress (E-field) effects are systematically tested and analyzed by using an experimental and modeling study. Source and drain (S/D) electrode asymmetry and vertical E-field effects on device instability are negligible, whereas the lateral E-field effects significantly affect device instability, particularly for zigzag channel shape, compared to circular and U-type TFTs. Moreover, charge trapping time (τ) for zigzag-type a-IGZO TFTs is extracted as 3.8×10^4 , which is at least three-times smaller than those of other channel-type a-IGZO TFTs, hinting that local E-field enhancement can critically affect the device reliability. The Technology Computer Aided Design (TCAD) simulation results reveal the locally enhanced E-field at both corner region in the channel in a quantitative mode and its correlation with hemisphere radius (ρ) values.



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Keywords: InGaZnO; thin-film transistor; instability; channel shape; electric field

1. Introduction

Recently, the requirement on ultra-low power-based driving of thin film transistors has soared due to significant demand on IoT applications, in particular, mobile devices such as smart-phones, smart-watches, and others. Moreover, the newly conceived thin film transistors with high field effect mobility, along with the capability of mass production and full compatibility with the previously setup manufacturing lines, have been welcomed for fulfilling all requirements for the future electronic applications, including flat panel displays [1–3]. In this perspective, among a variety of candidates for active materials which could be immediately applied toward the backplanes for flat panel displays (FPDs), amorphous indium–gallium–zinc oxide (a-IGZO) thin film transistors (TFTs) have attracted tremendous attention because they have high current drivability for an ultra-high definition (UHD) flat panel display beyond the advanced a-Si:H TFT technology. Furthermore, high electron mobility ($\mu_{\text{eff}} > 10 \text{ cm}^2/\text{Vs}$), process compatibility with the previously set-up lines, process capability toward large area (>100 inch), high transparency of a-IGZO film are fundamental merits for the future applications of flexible and transparent electronics [4–6].

Even though a-IGZO TFTs has been developed to such an extent that they can be applied to commercialized backplanes in flat panel displays such as active-matrix liquid-crystal display (AMLCD) and active-matrix organic light-emitting diode (AMOLED) [7,8], the reliability issues associated with electrical field, temperature, and light induced instabilities are still challenging issues for the mass production of reliable active-matrix flatpanel displays (AMFPDs) based on a-IGZO TFTs [9–14]. Among the various parameters that determine the reliability of a-IGZO TFTs, the geometrical shape of the channel for a-IGZO

TFTs can be one of the key design parameters to determine the electrical reliability of a-IGZO TFTs [15–20]. Up until now, comb-shaped electrodes for amorphous silicon solar cells and interdigitated (e.g., fork-shaped) electrodes in TFTs have been predominantly studied for reduction of gate-to-source capacitance which is one of the key requirements for reduction of kick-back voltage. This is one of the core parameters in determining image quality in FPDs during operation [18]. In addition, ring-shaped (or circular type) electrodes, which are one of the variations in the family of Corbino TFTs, were also studied for the enhancement on insights related to device reliability, which might have the strong dependency on asymmetrical electrical characteristics associated with geometrical configuration on electrodes in TFTs [15,18]. Thus, among a variety of channel shapes, U-type channel for pixel transistors in flat panel display backplanes, do have strong merits for achieving low gate-to-source capacitance (C_{gs}) per area, thereby, the U-shape of channel in pixel transistors has been predominately adopted in AMFPD pixel designs, compared with that of the I-type channel [21–23]. Beyond reduction of area dependent C_{gs} for pixel transistors, device reliability for TFTs has been one of the long-standing problems in the field of FPDs, even for future TFT-based applications, bio-imaging, X-ray detectors, gas sensors, and others. Until now, even though there were several reports on a-IGZO TFT reliability issues from the perspective of device geometry, interestingly it has been rarely studied for device reliability issues, in particular, channel shapes and their correlation in reliability, which is one of the most critical parameters for determination of electrical performance of a-IGZO TFTs. Furthermore, with only experimental data from implemented TFTs, it is very complicated and picky to identify net effects on device instability, which is purely engaged in device configuration and its geometry driven electric field strength among a variety of processes, materials, and physical dimension issues. The aforementioned parameters are correlated with physical dimension and their materials' properties. Thus, there is still a lot of room for improvement in understanding of channel geometries and their effects on device reliability via device implementation and electrical measurements, followed by their direct comparison, analytical modeling, their simulation-based analysis, and others.

Herein, we implemented a-IGZO TFTs based on representative channel designs such as: (i) circular type, (ii) zig-zag type, and (iii) U-type. Moreover, device instability characteristics associated with vertical and later electric field effects are evaluated independently, and furthermore, among a variety of factors such as device configuration, channel shapes, physical dimension of TFTs, and others, pure channel shape effects are systematically analyzed with the help of TCAD simulators (SILVACO, Inc.). With this platform, we identified that electric field strength associated with channel shape is highly contributed to device instability. Moreover, the net effects on device instability corresponding to field enhancement factor are quantitatively analyzed through only geometrical variation via TCAD platform, which leads to insight on channel shape and its geometrical variation effects to determine overall device reliability of a-IGZO TFTs. In a word, beyond simple study of academically interesting issues in terms of reliability of TFTs, we expect that this work can be beneficial for the provision of practical guidelines of device design rules in terms of channel shape determination, minimization of parasitic capacitance, and their correlated effects on the enhancement of device reliability in a-IGZO TFTs

2. Materials and Methods

The a-IGZO TFTs in this study have an inverted-staggered configuration, as shown in Figure 1d. First, 100 nm-thick Mo was deposited by using an RF-sputtering process at 100 W under a chamber pressure of 5×10^{-3} Torr in ambient Ar, followed by photolithographically patterned and etched in Mo etchant, forming gate electrodes. Thereafter, SiN_x (400 nm) were deposited by plasma-enhanced chemical vapor deposition (PECVD), immediately followed by deposition of SiO_x (50 nm) in the same PECVD chamber under 300 °C without vacuum break. A 50 nm-thick a-IGZO channel layer was RF-sputtered from IGZO targets (In:Ga:Zn = 1:1:1) for 20 min at 50 W under a chamber pressure of 5×10^{-3} Torr in Ar gas. After channel deposition, Mo (70 nm) was deposited and patterned,

forming source and drain (S/D) electrodes. For back-channel passivation, a 50 nm-thick SiO_x layer was deposited by the PECVD process. Finally contact holes were opened by the reactive ion etching (RIE) process for addressing electrical contact pads.

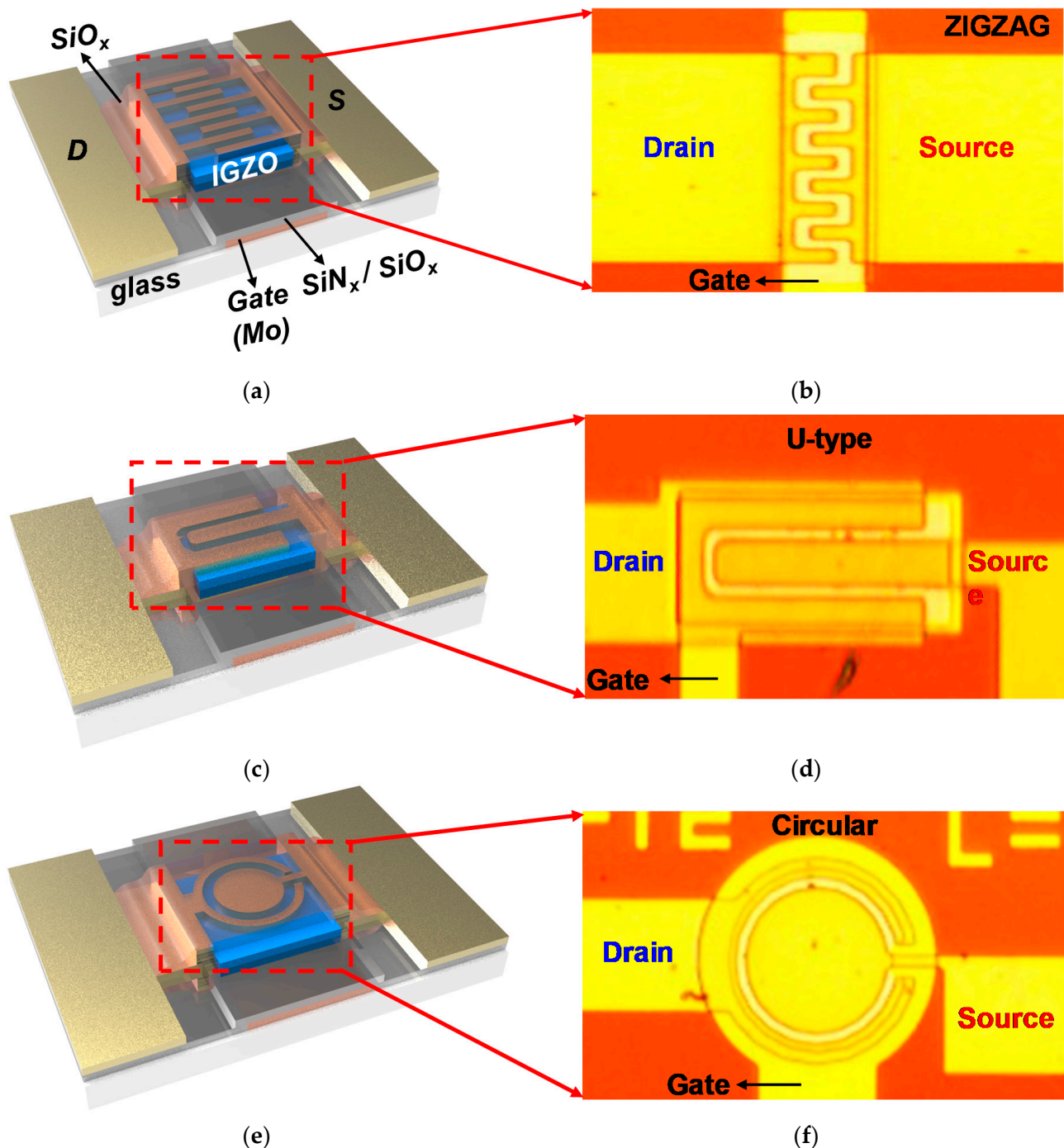


Figure 1. Schematic cartoons for the device configuration corresponding to (a) zigzag, (b) U-type, and (c) circular amorphous indium–gallium–zinc oxide (a-IGZO) thin film transistors (TFTs) and their optical microscope images for the implemented (d) zigzag, (e) U-type, and (f) circular a-IGZO TFTs, respectively.

The channel width and length for all a-IGZO TFTs are 200 and 4 μm , respectively. The electrical characterization of TFTs performance were carried out using Agilent 4155B in a dark and electrically shielded environment. All of the electrical stresses were performed on the thermal chuck at the substrate temperature 60 $^\circ\text{C}$.

3. Results and Discussion

3.1. S/D Asymmetry Effects for 3-Types a-IGZO TFTs

For understanding of channel shape effects on device reliability for a-IGZO TFTs, transfer characteristics depending on configuration of source and drain (S/D) electrodes were evaluated.

Figure 2a–c show the transfer characteristics of 3-types a-IGZO TFTs with two bias configurations: (i) Original and (ii) S/D change. As shown in inset figures, for ‘Original’ configuration, drain bias (V_{DS}) was applied to drain electrode, and for ‘S/D change’ configuration, drain bias was applied to the source electrode to investigate the effect of asymmetry in the S/D shape. Transfer characteristics were measured for a different drain bias condition of $V_{DS} = 0.1$ V and $V_{DS} = 10.1$ V, respectively. As shown in Figure 2a–c, transfer characteristics were almost identical regardless of channel shape for gate bias (V_{GS}) ranging from $V_{GS} = -20$ to 20 V. The slight deviation in the sub-threshold regime were within experimental error range. Furthermore, output characteristics of 3-types a-IGZO TFTs were measured to confirm asymmetry effects according to variation of V_{DS} . The V_{GS} sweeps from -10 to 20 V with 5-V step and output curves at $V_{GS} = 20$, 10, and 0 V were representatively displayed in Figure 2d–e. The output characteristics of all the devices show decent ohmic properties and negligible difference between the ‘original’ and the ‘S/D change’ configuration. thus, the electrical characteristics were proven to have the same electrical properties irrespective of S/D configuration for all channel shapes. These results indicate that S/D asymmetry effects are negligibly observed, hinting that transfer length (L_T) in the channel regime is large enough compared with the width of gate electrodes associated with full gate overlapped structures. In addition, electrical parameters for each channel shape were evaluated from transfer characteristics at $V_{DS} = 0.1$ V. The field-effect mobility for zigzag, U-type, circular a-IGZO TFTs were extracted as 2.77, 4.57, and 5.32 cm^2/Vs , respectively. Threshold voltage (V_{th}) based on constant current method [24], which is defined at the drain-to-source current ($\sim W/L \times 10^{-8}$ A), was extracted as -1.3 , -1.9 , and -2.8 V for zigzag, U-type, and circular a-IGZO TFTs, respectively. Subthreshold swing and On–off ratio were around 2.6 V/dec and 10^7 for all devices, respectively. All of the electrical properties for the three device configurations are within similar values except for field effect mobility.

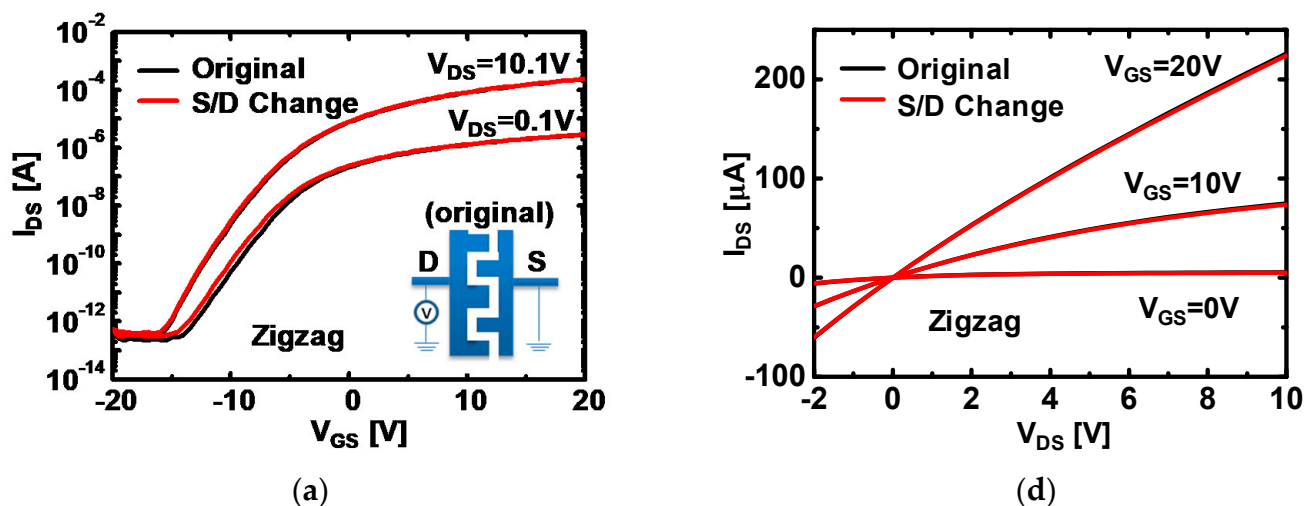


Figure 2. Cont.

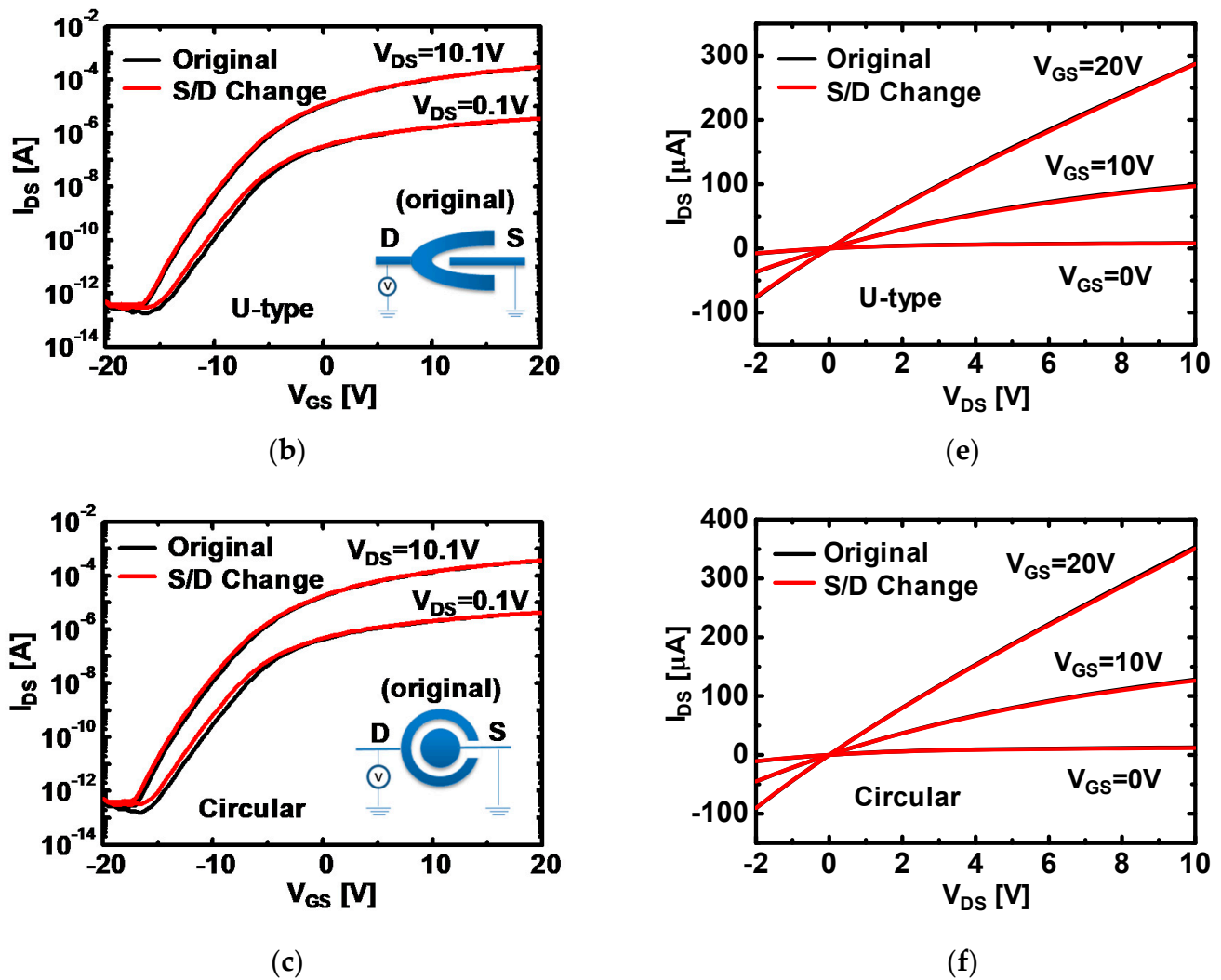


Figure 2. Transfer characteristics of (a) zigzag, (b) U-type, and (c) circular-type a-IGZO TFTs depending on bias configuration. The original is the bias configuration as shown in the inset. Source and drain (S/D) change is a reversed S/D configuration for the same bias value. Output characteristics, corresponding to each channel shape of (c) zigzag, (d) U-type, and (e) circular-type a-IGZO TFTs according to bias configuration. The channel width and length for a-IGZO is 200 and 4 μm , respectively.

3.2. Bias Temperature Stress Instability of 3-Types a-IGZO TFTs

For evaluation of device instability depending on channel shape, we performed a bias temperature stress for a-IGZO TFTs with different channel shapes. For monitoring of vertical field effects, V_{GS} of 25 V and V_{DS} of 0.1 V in the linear regime were applied to each device with the substrate temperature of 60 $^{\circ}\text{C}$ for 3600 s. Figure 3a–c shows the evolution of transfer characteristics under bias temperature stress. After the stress, shifts of V_{th} and transfer curves for each device were analogous and the variation is within experimental error range, which indicates the vertical field effects on device instability were negligibly observed. The results are thought to have come from the same device configuration of all the devices, particularly for vertical direction. Moreover, without any degradation of electrical properties such as subthreshold swing or on–off ratio, the parallel shift of V_{th} implies the simple charge trapping between the channel and insulator is associated with device instability. Furthermore, in most of the previous studies of the instability of a-IGZO TFTs under positive bias stress, it has been concluded that electron trapping at the interface and/or in the bulk region of the insulator is the mechanism responsible for a threshold voltage shift (ΔV_{th}) [24–32]. In this study, ambient effects were excluded for the origin of bias stress instability by existence of the passivation layer.

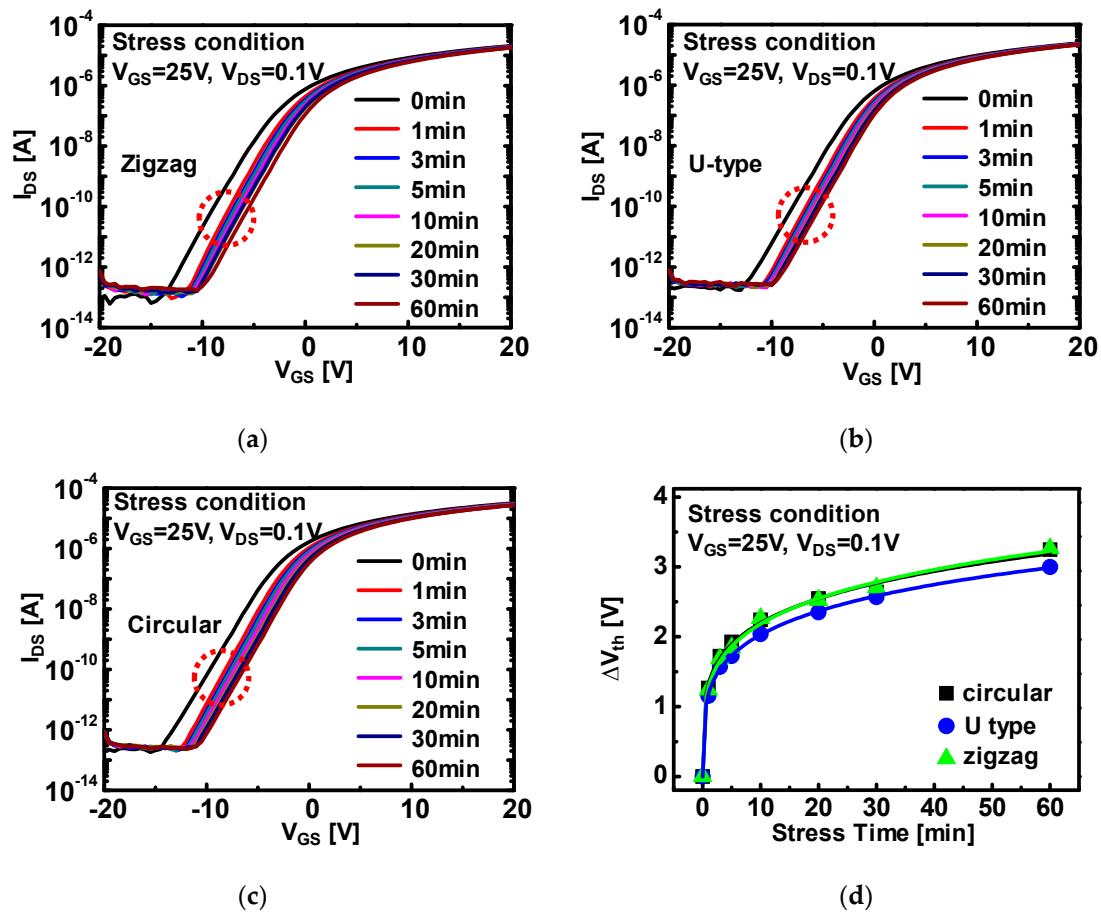


Figure 3. Transfer characteristics of (a) zigzag, (b) U-type, and (c) circular a-IGZO TFTs under bias stress condition of $V_{GS} = 25\text{ V}$ and $V_{DS} = 0.1\text{ V}$. All of the bias stress tests were executed under $60\text{ }^{\circ}\text{C}$ substrate temperature for 60 min. Evolutions of threshold voltage shift depending on bias stress time under stress condition of (d) $V_{GS} = 25\text{ V}$ and $V_{DS} = 0.1\text{ V}$.

For analytical understanding of device instability, the model of ΔV_{th} by the charge-trapping mechanism was employed in this study. The stretched-exponential equation for the ΔV_{th} is defined by the following equation [25,33]:

$$\Delta V_{th}(t) = \Delta V_{th0} [1 - \exp\{-(t/\tau)\}^{\beta}] \quad (1)$$

where ΔV_{th0} is the ΔV_{th} at infinite time, $\tau = \tau_0 \exp(E_{\tau}/kT)$ represents the characteristic trapping time of carriers where the thermal activation energy is given by $E_a = E_{\tau}\beta$. β is the stretched-exponential exponent and E_{τ} is the average effective energy barrier that electrons in the a-IGZO need to overcome before they move into the insulator, and τ_0 is the thermal prefactor for emission over the barrier. Figure 3d shows evolution of ΔV_{th} (scatter) according to bias stress time for vertical electric field stress (E-field) effect and fitting line from Equation (1). As a result, ΔV_{th} is well fitted with Equation (1), which can be attributed to the emission of trapped charges toward deep states in the bulk dielectric for longer stress time ($t > \tau$). Table 1 shows that extracted fitting parameters for a-IGZO TFTs under bias temperature stress in the linear regime. The extracted values for trapping time constant are in the similar range from 1.1×10^4 to 2.8×10^4 . Moreover, stretched-exponential fitting parameters (β) are about ~ 0.35 . Therefore, these results support the fact that 3-types a-IGZO TFTs, which have exactly the same device structure except for the shape of the S/D electrode, have negligible difference for vertical E-field stress between the channel and insulator.

Table 1. Summary of ΔV_{th} and trapping time extracted from stretched exponential equation for 3-types a-IGZO TFTs.

Stress Condition	Parameter	Channel Shape		
		Circular	U-Type	Zigzag
$V_{GS} = 25 \text{ V}, V_{DS} = 0.1 \text{ V}$	$\Delta V_{th,max} \text{ (V)}$	3.32	3.06	3.32
	Trapping time, $\tau \text{ (s)}$	1.6×10^4	2.8×10^4	1.1×10^4
$V_{GS} = 15 \text{ V}, V_{DS} = 15 \text{ V}$	$\Delta V_{th,max} \text{ (V)}$	1.40	1.42	2.10
	Trapping time, $\tau \text{ (s)}$	2.0×10^5	3.4×10^5	5.5×10^4

In parallel, lateral E-field induced instability behaviors for each channel shape were investigated in order to monitor the channel shape dependency on the device instability issue. The V_{GS} of 15 V and V_{DS} of 15 V were applied to each device at the substrate temperature of 60 °C for 3600 s. All of the devices were under saturation regime during the bias temperature stress to enhance the E-field between S/D electrodes. Figure 4a–c display the transfer characteristics under bias temperature stress. Interestingly, zigzag-type a-IGZO TFTs clearly revealed a larger V_{th} shift, compared to U-type and circular-type a-IGZO TFTs. For clear comparison of ΔV_{th} depending on channel shapes, ΔV_{th} versus stress time was evaluated in Figure 4d. The ΔV_{th} for the zigzag-type device was extracted as 2.1 V, whereas ΔV_{th} of the other two devices were 1.4 V at 60 min of stress time. It shows the ΔV_{th} of zigzag-type a-IGZO TFTs have significantly deviated during all the stress time, compared with the other two devices. The distinctive increase of V_{th} shift was attributed to the strong lateral E-field enhancement associated with geometrical corner of zigzag shape. In the structure of zigzag-type a-IGZO TFTs in Figure 1b, the edge region of the source electrode is surrounded by the drain electrode through three directions, thus, E-field from the drain electrode is anticipated to be focused on the edge region of the source electrode, resulting in the higher magnitude of the E-field than the generally expected value, and local instability in the channel. This makes it possible to explain the phenomenon that the instability (i.e., $\Delta V_{th} \sim 1.5 \text{ V}$) was significantly induced in the zigzag-type, compared with those of circular and U-type channel TFTs. The U-type a-IGZO TFTs have one electrode (e.g., drain) which is surrounded by the other electrode (e.g., source). Thus, in the channel region of U-type TFTs, the ratio of the length of straight side to a surrounded channel length between the source and drain and number of corners, together with the curvature of the corner in the channel are critical parameters to determine electric field concentration for the fixed bias voltage. Most regions of the U-type source electrode are closely faced with the drain electrode with only two corners, whereas, in the case of the zigzag-type, it has multiple corners and only edge areas are close to the drain electrode. (As per curvature effects on device instability, it was discussed in the following section) Therefore, U-type a-IGZO TFTs are expected to have relatively less E-field enhancement. As overall comparison for all the bias stress condition and channel shape, ΔV_{th} and trapping characteristics are summarized in Table 1. Trapping time was much smaller at the stress condition of $V_{GS} = 25 \text{ V}$ and $V_{DS} = 0.1 \text{ V}$ for all the devices, leading to the larger ΔV_{th} . On the other hand, when V_{GS} decreases and V_{DS} increases for stress conditions ($V_{GS} = 15 \text{ V}$ and $V_{DS} = 15 \text{ V}$), ΔV_{th} was considerably decreased. Considering the results from Table 1, vertical E-field more strongly affects ΔV_{th} than lateral E-field. In addition, U-type a-IGZO TFTs exhibit relatively better stability for bias temperature stress among devices. As adopted for a-Si TFTs, U-type is known to have lower gate-to-source overlapped capacitance (C_{GS}), thus, this result is well matched with geometrical channel shape effect for electrical instability [23].

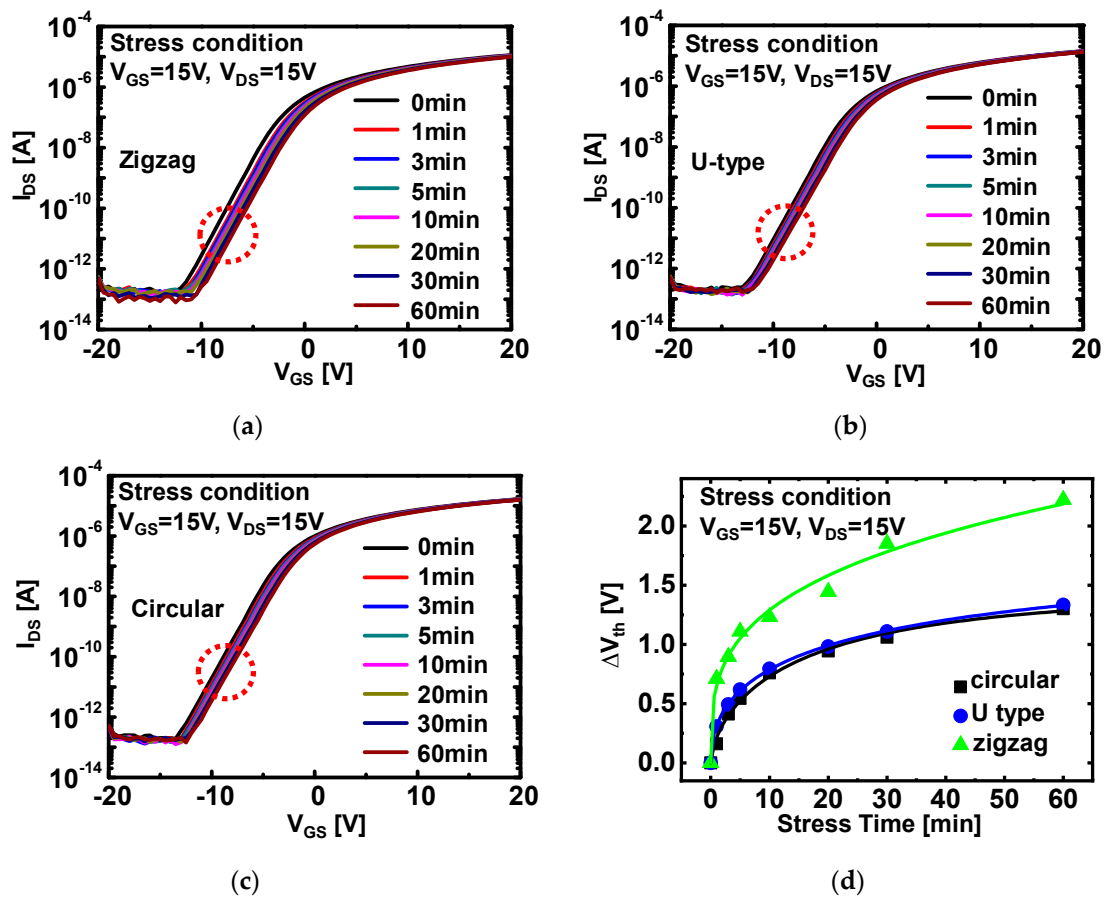


Figure 4. Transfer characteristics of (a) zigzag, (b) U-type, and (c) circular a-IGZO TFTs under bias stress condition of $V_{GS} = 15$ V and $V_{DS} = 15$ V. All of the bias stress tests were executed under 60 °C substrate temperature for 60 min. (d) Evolutions of threshold voltage shift depending on bias stress time under stress condition of $V_{GS} = 15$ V and $V_{DS} = 15$ V.

3.3. Study on E-Field Distribution in the Channel Depending on Channel Shape

For the better understanding of E-field enhancement depending on channel shape, Technology Computer Aided Design (TCAD, Silvaco Inc.) simulation was employed to analyze E-field distribution in the channel in a quantitative mode [34]. Figure 5a–c shows simulated results with device structures depending on different ρ values. In Figure 5, the pink region is the S/D electrode, the blue region is the channel area, the arrow is E-field, and L is the length of electrode. Furthermore, ρ indicates the hemisphere radius, thus, a long ρ represents spherical corner shape at the channel/electrode boundary and a short ρ represents perpendicular corner shape. In Figure 5a, the device with circular corners shows identical color (i.e., identical magnitude of E-field) along the channel region. However, when the ρ is shortened and the corner becomes stiff, E-field is concentrated on the corner region and its magnitude is increased in Figure 5b. Furthermore, when ρ becomes zero as shown in Figure 5c, the E-field is more sharply focused on the corner than in Figure 5b. To quantitatively confirm its effect, enlarged images of simulation and E-field values along the channel toward the x-axis direction were presented in Figure 6. Figure 6a shows an enlarged one-side corner of the structure from Figure 5a. To closely see the difference of E-field between the corner and the common region, scanning areas are divided into three sections. For all of the sections, Figure 6a,b exhibit a relatively uniform distribution of E-field from 8 to 13 kV/cm along the channel. (The data of E-field = 0 indicates the measuring point is in the metal electrode region.) However, in Figure 6c,d, a highly enhanced E-field at Section 1 was shown with a value of 22 kV/cm at both corners. And for Sections 2 and 3, which are slightly separate from the corner, the E-field

is analogous to results from Figure 6a,b, indicating E-field is concentrated at the corner region. In the case of a device structure with $\rho = 0$, as shown in Figure 6e,f, E-field at Section 1 shows a remarkable increase with the value of 45 kV/cm at both corners, which is four-times larger than it is at Section 3. This result indicates the perpendicular shape of the corner induces more E-field enhancement than the spherical shape, thus, the E-field enhancement is directly associated with value of ρ . For the confirmation of ρ dependency, E-field at Section 1 depending on various ρ was extracted in Figure 7. Similarly, the results of Figures 6 and 7a show the two highest E-field peak at both corners. Its maximum value at the corner was gradually increased as ρ decreased. The detailed extracted E-field values depending on ρ were presented in Figure 7b. This result can be meaningfully when combined with results of bias temperature stress instability. In the device structure, ρ is calculated as 1.18 μm for zigzag-type a-IGZO TFTs and calculated as 3.09 μm for U-type a-IGZO TFTs, thus, it is expected to have larger E-field enhancement for the zigzag-type a-IGZO TFTs than the U-type device. Since zigzag-type a-IGZO TFTs show a larger V_{th} shift than U-type device in Figures 4 and 5, this expectation from TCAD simulation is well matched with experimental results. All of the results in this section substantiate the presence of E-field enhancement at the corner region of the channel, and its variation depending on hemisphere radius ρ .

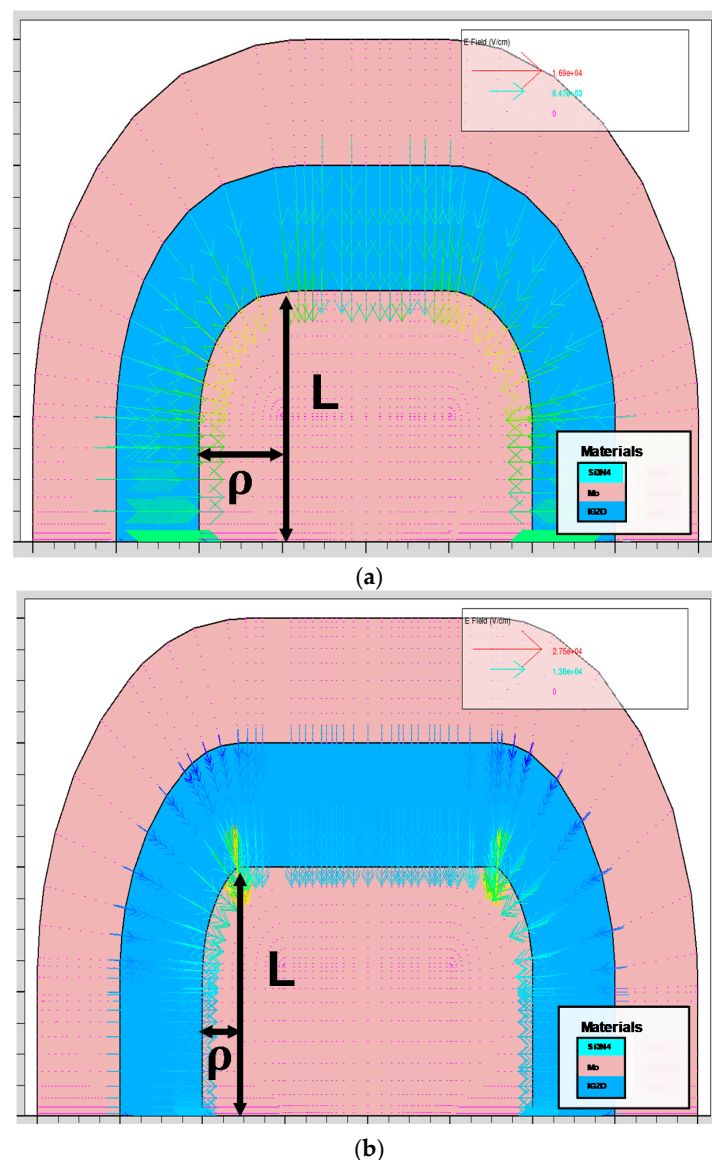


Figure 5. Cont.

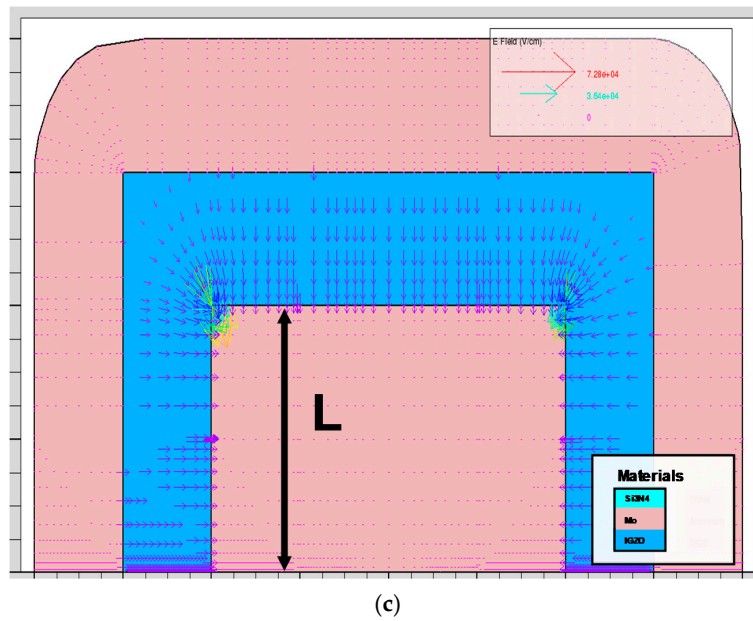


Figure 5. Simulated electric field stress (E-field) distribution from device structures with (a) larger ρ (round corner), (b) small ρ , and (c) $\rho = 0$ (perpendicular corner). The distribution of E-field was focused and the magnitude was enhanced at the corner region of the channel, especially for devices with a smaller ρ .

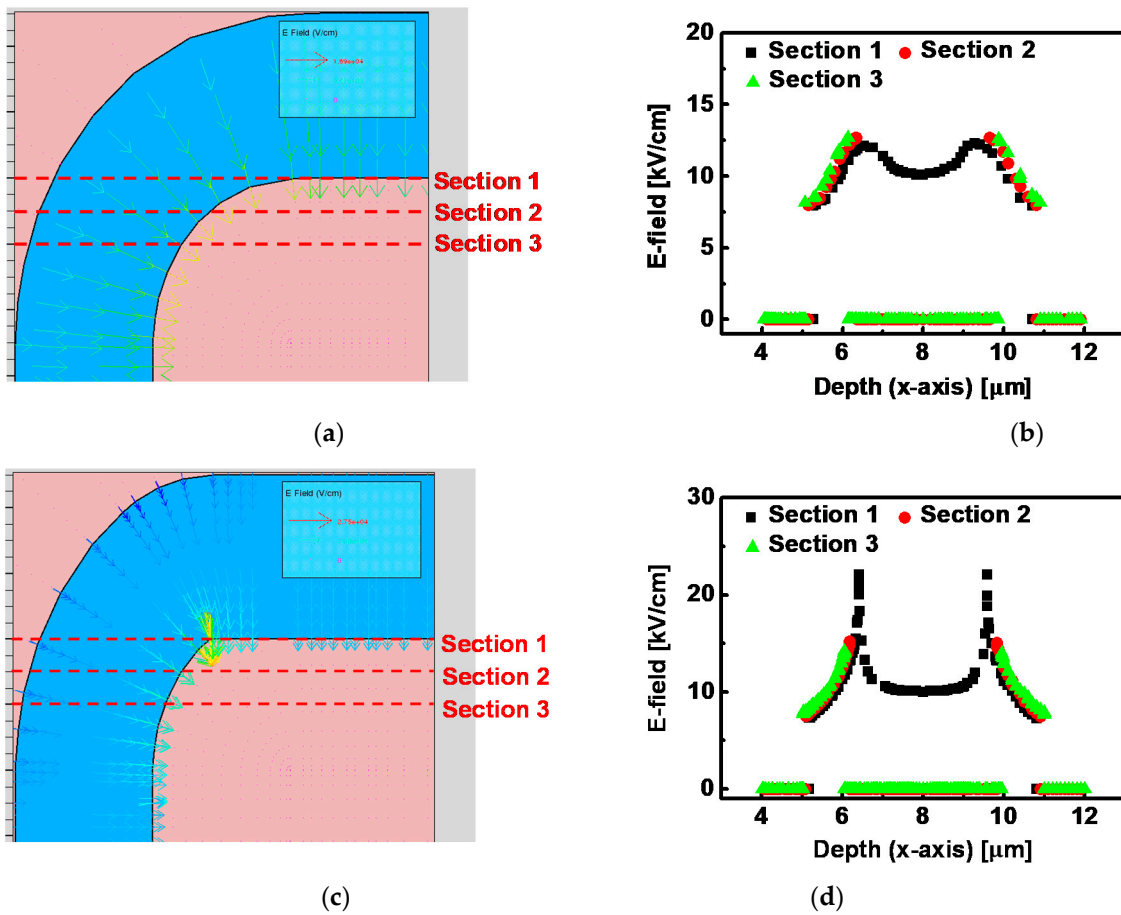


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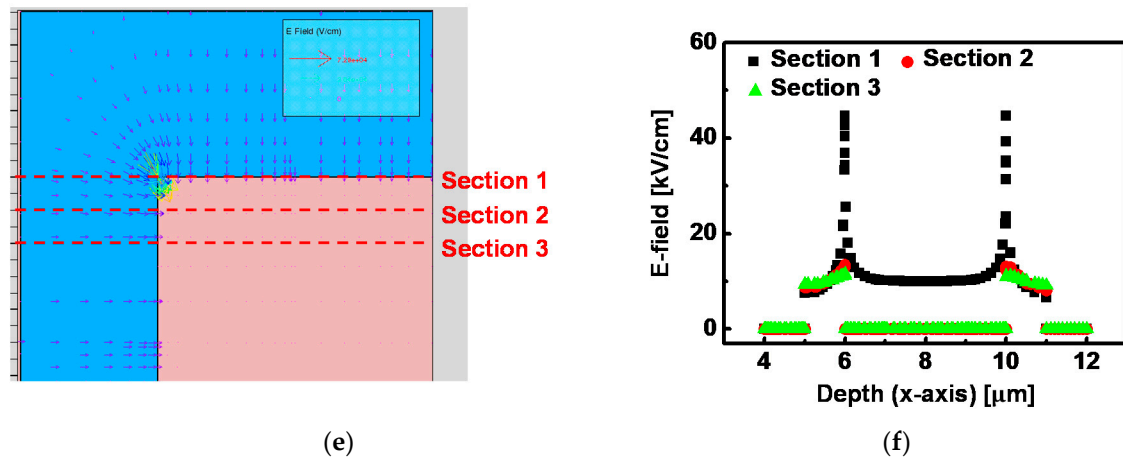


Figure 6. Enlarged device structure and extracted E-field distribution near the corner region with (a,b) larger ρ (round corner), (c,d) small ρ , and (e,f) $\rho = 0$ (perpendicular corner).

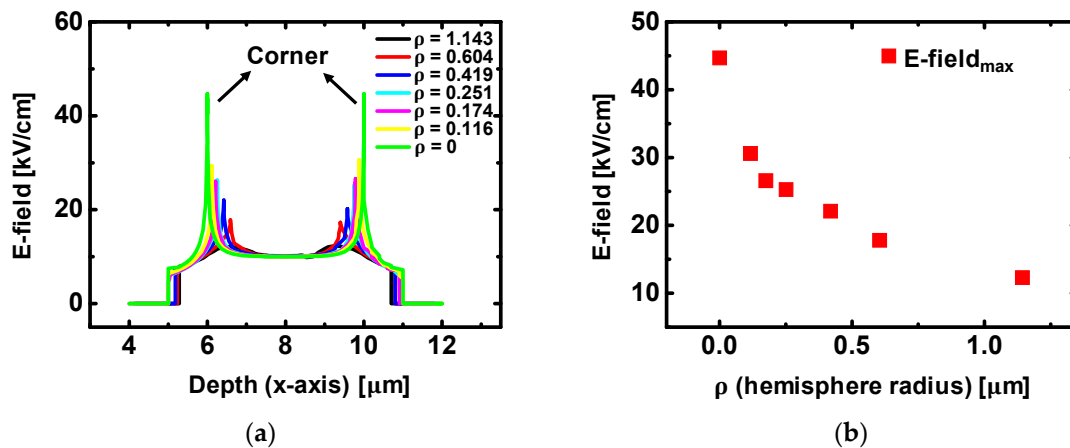


Figure 7. (a) E-field variation at Section 1 depending on hemisphere radius (ρ) of the channel. (b) Extracted maximum E-field values at the different hemisphere radius.

4. Conclusions

In this study, we have investigated channel shape effects on device reliability for a-IGZO TFTs. From the transfer characteristics in linear and saturation regime, the S/D asymmetry effects were hard to be observed due to large transfer length (L_T) compared with the width of gate electrodes associated with full gate overlapped structures. In parallel, regardless of channel shape in a-IGZO TFTs, vertical E-field stress on bias temperature stress instability turned out to be analogous for all of the devices, whereas lateral E-field effects were significantly pronounced for zigzag-type a-IGZO TFTs. Time dependence of ΔV_{th} in a-IGZO TFTs is well fitted with a stretched-exponential equation, which can be derived from the assumption that the origin of threshold voltage shift is attributed to the trapping of charges in the interface and bulk dielectric layers. Furthermore, E-field enhancement effects on the locally sharpened source and the drain edge of the zigzag-type a-IGZO TFT can cause huge degradation of device instability. For elucidation of E-field enhancement at the corner region and its variation depending on hemisphere radius ρ , TCAD simulation was used. The simulation results revealed the locally enhanced E-field at both the corner region and its correlation with ρ values. Furthermore, the simulated results were well matched with experimental device instability tests associated with channel shape. We expect that this work can be beneficial for the provision of practical guidelines of device

design rules in terms of channel shape determination, minimization of parasitic capacitance, and their correlated effects on the enhancement of device reliability in a-IGZO TFTs.

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