Key concepts behind forming-free resistive switching incorporated with rectifying transport properties

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This work reports the effect of Ti diffusion on the bipolar resistive switching in $Au/BiFeO_3/Pt/Ti$ capacitor-like structures. Polycrystalline $BiFeO_3$ thin films are deposited by pulsed laser deposition at different temperatures on $Pt/Ti/SiO_2/Si$ substrates. From the energy filtered transmission electron microscopy and Rutherford backscattering spectrometry it is observed that Ti diffusion occurs if the deposition temperature is above 600°C. The current-voltage (I–V) curves indicate that resistive switching can only be achieved in $Au/BiFeO_3/Pt/Ti$ capacitor-like structures where this Ti diffusion occurs. The effect of Ti diffusion is confirmed by the $BiFeO_3$ thin films deposited on Pt/sapphire and Pt/Ti/sapphire substrates. The resistive switching needs no electroforming process, and is incorporated with rectifying properties which is potentially useful to suppress the sneak current in a crossbar architecture. Those specific features open a promising alternative concept for nonvolatile memory devices as well as for other memristive devices like synapses in neuromorphic circuits.

Resistive switching has been widely studied in recent years due to the potential applications in nonvolatile resistive memory devices. In general, resistive switching can be categorized into two main types: filamentary type[1–4] and interface type[5–8]. It has been accepted that filamentary switching is due to the formation of local conductive filaments, which results from the redistribution of oxygen vacancies[9,10] or the diffusion of metal ions.[11,12] For interface switching, different mechanisms have been proposed, such as migration of oxygen vacancies[13], charge trapping[7], or polarization switching[14,15].

For the interface-related resistive switching, much research work has been focused on the interface where resistive switching takes place. In most cases the stack is designed in a way that this is the interface between top electrode and thin film. For example, Shen et al.[16] reported that significantly improved switching performance has been achieved in $(Ba,Sr)TiO_3$ (BST) thin films by using W as top electrode instead of Pt. They attributed this behavior to a reversible oxidation and reduction process at the W/BST interface. Similarly, Liao et al.[17] proposed that a thin metal-oxide layer between the top electrode and a $Pr_{0.7}Ca_{0.3}MnO_3$ thin film is important for resistive switching. The formation of this metal-oxide layer is dependent on the Gibbs free energy of oxidation of the top electrodes. The influence of top electrode material has also been reported for the resistive switching in NiO[18] and ZrO[19] thin films. In addition, the geometry of the top electrode was identified to play an important role. Fujimot et al.[20] observed resistive switching in an $Ag paste/Pr_{0.7}Ca_{0.3}MnO_3/Pt$ structure, while no switching could be obtained in a $Pt/Pr_{0.7}Ca_{0.3}MnO_3/Pt$ structure, where the Pt top electrode was fabricated by sputtering. They suggested that the Ag paste forms point contacts to the thin film, which induces resistive switching.

Nevertheless, in a metal/oxide/metal capacitor structure, the conductivity is not solely determined by the first electrode/oxide interface. The effect of the second oxide/electrode interface has been studied with less intensity when investigating resistive switching behavior. Especially for perovskite thin films, which are usually deposited at high temperatures, the bottom interface undergoes a high temperature process, thereby the interdiffusion

between the thin film and bottom electrode is inevitable. This was often observed in ferroelectric memory fabrication[21,22]. The interdiffusion between ferroelectric thin film and metal electrode at the bottom interface deteriorates the performance of ferroelectric thin films. In commercially available ferroelectric memory devices the problem is circumvented by the oxide bottom electrode that is required to achieve a high endurance in PZT thin films. Therefore, the investigation of bottom interface is also crucial for resistive switching devices, especially when the insulating oxide layer is deposited onto a metal bottom electrode at rather high temperatures or requires a subsequent annealing step.

The most popular bottom electrode for the deposition of many oxide thin films is Pt. To obtain better adhesion between Pt layer and SiO_2/Si substrates, a Ti layer is usually introduced in between. The resulting substrate with Pt electrode has a structure of $Pt/Ti/SiO_2/Si$. Since Pt is chemically and thermally stable, interdiffusion or reaction between Pt and the oxide thin films is not expected. However, the diffusion of adhesion layer atoms, here Ti atoms, becomes significant if the thin film has a high deposition temperature or is annealed at high temperatures after deposition. This diffusion can influence the electrical properties of the whole capacitor structure considerably. So far, only little work has been performed on this issue. For instance, Yang et al.[23] reported that thermal diffusion of Ti atoms from the adhesion layer takes place throughout the Pt layer when depositing

TiO_2 thin films at 250°C. The diffused Ti acts as the seeds for conductive filaments and controls the resistive switching in TiO_2.

In our previous work, a nonvolatile bipolar resistive switching has been reported in $BiFeO_3$ (BFO) thin films that were deposited on $Pt/Ti/SiO_2/Si$ substrates[24,25]. BFO belongs to the group of perovskite oxides, and the deposition temperature of BFO thin films has to be strictly controlled in order to prevent the formation of impurity phases[26]. The optimized substrate temperature is $550 \sim 650$°C for the growth by pulsed laser deposition (PLD) in a highly automated PLD system from SURFACE. This temperature is much higher than that reported by Yang et al.[23] Therefore, it is necessary to study the effect of Ti diffusion after such a high deposition temperature on the resistive switching in BFO thin films.

Results

I–V curves of all the samples measured at room temperature are presented in Figure 1, together with sketches that depict the corresponding BFO capacitor-like structure of the investigated samples in the insets. The DC voltage is applied to the top Au electrode while the bottom Pt electrode is grounded. The steady time of each voltage point during the DC sweeping is 100 ms in voltage steps of 200 mV, and the voltage sequence is: $0 \rightarrow +7 \text{ V} \rightarrow 0 \rightarrow -7 \text{ V} \rightarrow 0$.

As shown in Figure 1a, the deposition temperature significantly influences the I–V characteristics of the BFO thin films deposited on
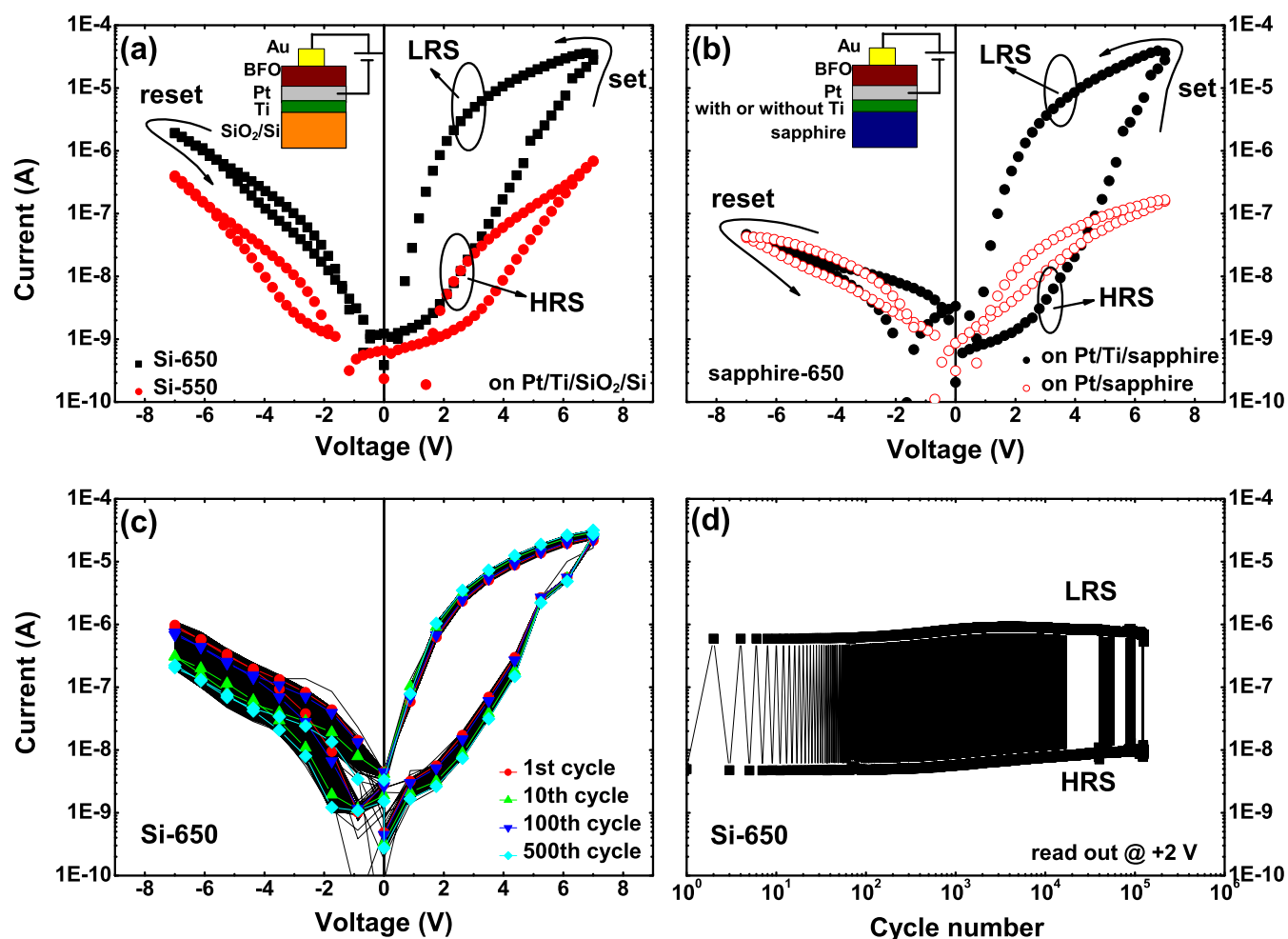

Figure 1 | (a) I–V curves of ca. 500 nm thick BFO thin films on Pt(200 nm)/Ti(100 nm)/SiO$_2$/Si substrates deposited at 650°C (Si-650, black solid squares) and at 550°C (Si-550, red solid circles). (b) I–V curves of ca. 500 nm thick BFO thin films on Pt(100 nm)/Ti(30 nm)/sapphire (Pt/Ti/sapphire, black solid circles) and on Pt(100 nm)/sapphire (Pt/sapphire, red empty circles) substrates deposited at 650°C. (a,b) The size of the top contact amounts to 0.03 cm². (c) I–V curves of Si-650 for ~700 DC cycles. (d) Endurance test on Si-650. The LRS and HRS are set and reset by +6.5 V and -6.5 V voltage pulses, respectively, and the resistance is read out by a +2 V voltage pulse.

Pt/Ti/SiO$_2$/Si substrates. With higher deposition temperature of 650°C, the I–V curve exhibits a typical bipolar resistive switching behavior (Si-650). As indicated by the arrows in Figure 1a, the positive bias induces a set operation that switches the structure from high resistance state (HRS) to low resistance state (LRS), and the negative bias resets the structure from LRS to HRS. The ON/OFF ratio, i.e. R$_{HRS}$/R$_{LRS}$, is ~270 at a voltage of +2 V. The resistive switching is a nonvolatile effect, which has been proved in our previous reports[24,25].

It has to be pointed out that no electroforming at higher voltages is needed before the observation of I–V hysteresis. The electroforming is a destructive process that involves chemical reaction and thermal damage in the device[27], and the randomly formed conductive filaments during the electroforming also deteriorate the uniformity of the device performance[28]. There has been a large amount of work exploring proper electroforming conditions in order to improve the resistive switching properties[29–33]. However, from the point of view for industrial applications, it is favorable that the electroforming step can be eliminated[27]. In the present work, the as-deposited BFO thin film (sample Si-650) is initially at HRS. It can be directly switched to LRS by the first voltage sweeping from 0 to +7 V, then the voltage sweeping from +7 V to 0 produces the hysteresis. Without electroforming, the device shows uniform performance, the I–V curves recorded on different memory cells exhibit similar hysteresis[25]. Moreover, the voltage sweepings on the same capacitor cell yield nearly identical I–V characteristics. As shown in Figure 1c, an endurance test was realized by repeating the DC voltage for more than 500 cycles, the recorded I–V curves show very similar hysteresis behavior, which indicates the switching is reproducible. A more pronounced endurance test is shown in Figure 1d, where the structure is switched by voltage pulses, i.e. + 6.5 V for LRS and −6.5 V for HRS, and the resistance after switching is read out by a small voltage of +2 V. The result indicates that the structure can be switched between HRS and LRS for more than 10^5 cycles without failure.

Note that there is no abrupt drop or jump of resistance during the set and reset processes. This is rather different from most resistive switching systems based on binary oxide thin films, where the set or reset operation induces a sudden change of the resistance[34–37]. To some extent, the gradual modulation of resistance by voltage in the BFO-based structure is consistent with the memristor model proposed by Chua in 1971[38], although the resistance change is not strictly dependent on the charge flowing through the device. A practical guide for validated memristance measurements on the BFO resistive switching device has been introduced recently[39]. Due to the gradual change of resistance, it has been shown that multilevel resistance states can be introduced into each BFO-based memory cell[40]. More interestingly, this switching behavior is potentially useful for mimicking the synapses in artificial neuromorphic circuits. For example, a waveform driven plasticity has been reported recently in our BFO-based memristive devices[41].

In addition to the bipolar resistive switching, another distinguishing feature of Si-650 is its rectifying behavior. The positive bias applied on the Au top electrode is the forward direction of the rectifying junction, while the negative voltage on Au reversely biases the junction. The rectification factor is ~20 at ± 7 V. For resistive switching memory devices, the memory cells are constructed in a crossbar array. It is well known that a passive crossbar suffers from the sneak currents, which cause serious reading interference. To overcome this problem, a diode is serially connected to each memory cell (1D1R)[42]. The rectifying characteristic of Si-650 can omit the implementation of such additional diodes due to the low reverse leakage current. More importantly, the memory window of Si-650 locates in the positive bias range, i.e. the I–V hysteresis appears under positive bias, which means the reading operation is always realized by forward bias. This can effectively prevent the reading interference by suppressing the sneak current. To obtain high signal sensitivity and

high memory density, the reverse leakage current needs to be further decreased[43]. And the reverse leakage current is dependent on the surface roughness of the BFO thin films, which will be shown later.

The rectifying behavior reveals that the transport in Si-650 is remarkably influenced by the electrode/film interfaces. Since BFO thin films show n-type conducting behavior[44] and taking into account the forward direction of the junction, a Schottky contact is likely formed at the Au/BFO top interface. The BFO/Pt bottom interface has a much lower potential barrier and exhibits quasi-ohmic contact characteristics. When the junction is reversely biased (negative bias), the transport of the Au/BFO/Pt capacitor is mainly governed by the Schottky barrier, which gives rise to the non-hysteretic I–V curve under negative bias.

In contrast, it is observed that the rectifying behavior disappears if the deposition temperature is decreased down to 550°C (Si-550), as indicated by the red curve in Figure 1a. The current is reduced by more than one order of magnitude under both voltage polarities as compared to Si-650. More interestingly, after decreasing the deposition temperature, it becomes difficult to switch the structure to LRS under positive bias. Although there is still a hysteresis, the ON/OFF ratio is only ~4 at a voltage of + 2 V, which is much smaller than the 270 observed for the sample Si-650. The absence of an obvious resistive switching in Si-550 by decreasing the deposition temperature is likely due to the high barrier height of the BFO/Pt bottom interface and by the decreased concentration of conduction electrons. The symmetric I–V of Si-550 indicates that the barrier heights of the Au/BFO and BFO/Pt interfaces are comparable. Therefore, the resistive switching in Si-650 is strongly correlated to the rectifying transport property, which is caused by the different barrier heights at the two electrode/BFO interfaces. To obtain bipolar resistive switching in the Au/BFO/Pt capacitors, an asymmetric structure with different barrier heights at the two electrode/BFO interfaces has to be fabricated. In this regard, the substrate temperature during the thin film deposition plays an important role in resistive switching. While the Au/BFO top interface is always rectifying, the barrier at the BFO/Pt bottom interface is significantly influenced by the deposition temperature.

The arising question is the collapse of contact barrier at the BFO/Pt interface in sample Si-650, where a Schottky contact should also have been formed because of the even higher work function of Pt (5.12–5.93 eV) than that of Au (5.10–5.47 eV). To understand the absence of barrier potential at the BFO/Pt interface in Si-650, the EFTEM elemental maps for Ti are shown in Figure 2 for the cross-sections of sample Si-550 (Figure 2a) and Si-650 (Figure 2b). The orange area with higher brightness shows the distribution of the Ti. In Si-550, the Ti layer below the Pt layer can be clearly distinguished. In contrast, the edge of the Ti layer is obscure in the sample Si-650. And a few Ti 'strip-like' regions penetrating through the above lying Pt layer are detected, which gives the clear signature that a certain amount of Ti has diffused to the Pt/BFO interface during the growth of BFO at the temperature of 650°C. These results are further confirmed by RBS measurements of the Pt(200 nm)/Ti(100 nm) layers (without BFO deposition) annealed in the PLD chamber under the same conditions as the BFO deposition processes for sample Si-550 and Si-650. The RBS spectra shown in Figure 3 demonstrate that the Ti signal and Pt signal locate separately in the backscattering energy range 511–626 keV and 713–1088 keV, respectively, for the virgin and annealed Pt/Ti layers at 550°C. However, due to the enhanced Ti diffusion, for the Pt/Ti layers annealed at 650°C the Ti and Pt signal merge and clearly evidence intermixing between Ti and Pt layers. Ti concentration at the BFO/ Pt interface of sample Si-650 is determined to be 30% by fitting the RBS spectrum with SIMNRA simulation code[45].

The EFTEM images indicate that Ti diffuses throughout the Pt layer and reaches the BFO/Pt interface, which produces a heavy n-type doping region near the bottom interface[23]. That is the possible
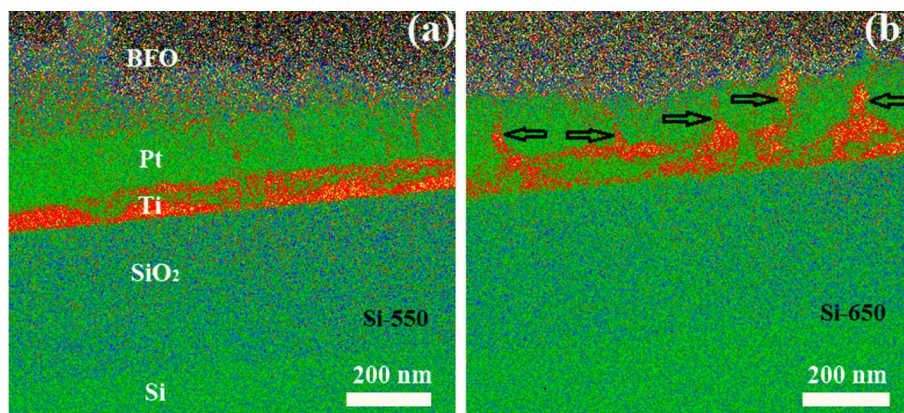
Figure 2 | The EFTEM images in the cross sections of sample Si-550 (a) and Si-650 (b). Ti diffusing through the Pt layer is marked by the arrows in (b).

reason for the low barrier height at the bottom interface, which gives rise to the rectifying I–V curve of Si-650. The role of Ti diffusion is confirmed by another two reference samples as shown in Figure 1b. The film grown on Pt/sapphire without Ti layer (Pt/sapphire) exhibits symmetric I–V curve, and is not resistively switchable. In contrast, after introducing a Ti layer between the Pt and sapphire (Pt/Ti/sapphire), a rectifying and hysteretic I–V curve can be observed. The rectification factor and ON/OFF ratio are ∼800 at ± 7 V and ∼545 at +2 V, respectively, which are both higher than those of Si-650. It can be seen that the current of sample Pt/Ti/sapphire is comparable with that of Si-650 under positive bias (forward bias), but the current under negative bias (reverse leakage current) is suppressed by nearly two orders of magnitude, which produces a larger rectification factor. The larger ON/OFF resistive switching ratio in Au/BFO/Pt/Ti/sapphire as compared to that in Si-650 is likely related to the larger rectification factor, i.e. the lower reverse leakage current.

The suppressed reverse leakage current in Au/BFO/Pt/Ti/sapphire can be explained by the smoother BFO surface before the Au electrode deposition. As shown in Figure 4, the surface roughness of the BFO thin films is much smaller on Pt/sapphire (14.8 nm, Figure 4c) or Pt/Ti/sapphire (16.3 nm, Figure 4d) substrate. The smoother BFO surface helps to establish a higher barrier height at the interface between the top electrode and the BFO thin film, inducing a much lower leakage current under negative bias[46]. In contrast, the thin films on Pt/Ti/SiO$_2$/Si substrates have large surface roughness (20.9 nm of Si-550 and 27 nm of Si-650), consequently the reverse leakage current is increased.

The fundamental mechanism of resistive switching can help to better understand the important role of Ti diffusion. The rectifying transport in those resistively switchable samples (Si-650 & Pt/Ti/sapphire) reveals that the electron injections from both electrodes into the BFO thin film are not equivalent under opposite voltage polarities. Under forward bias (positive bias), because of the low barrier at the BFO/Pt interface caused by the Ti diffusion, a large number of electrons is injected from the bottom Pt electrode into the depletion layer at the Au/BFO interface and trapped by trapping centers. Recently, Luo et al.[47] reported that oxygen vacancies act as electron trapping centers and are responsible for the bipolar resistive switching behavior in their Mn-doped BFO thin films. In our thin films, this trapping process reduces the depletion layer thickness, and sets the structure to LRS (Figure S1(a)). While under reversed bias (negative bias), electrons are blocked by the Au/BFO Schottky interface, a large electric field is thus applied across the depletion layer, which activates the trapped electrons and emits them from the depletion layer into the bottom Pt electrode. This detrapping process extends the depletion layer and therefore resets the structure to HRS (Figure S1(b)). This mechanism also explains the relationship between the rectification factor and the ON/OFF ratio. For the reset operation, larger rectification factor, essentially low reverse leakage current under negative bias, produces larger electric field on the
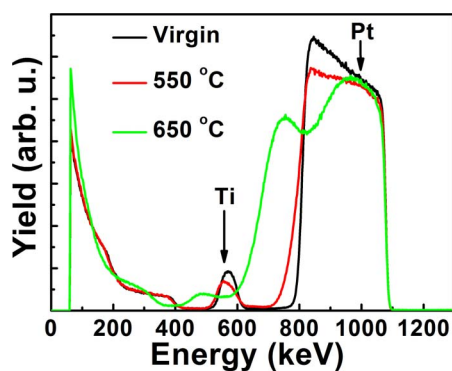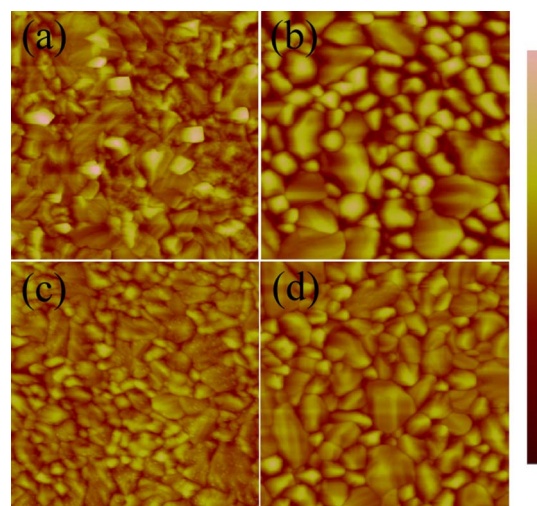

Figure 3 | RBS data revealing that the obvious intermixing of Ti and Pt only occurred in thermally treated Pt(200 nm)/Ti(100 nm)/SiO$_2$/Si-substrates at 650°C. The thermal treatments were the same as applied to sample Si-550 and Si-650 (Figure 2). The arrows mark the energy ranges of backscattering particles for the Ti signal and the Pt signal.

Figure 4 | AFM images showing the surface morphology of BFO thin films deposited on Pt/Ti/SiO$_2$/Si substrates at 550°C (a) and 650°C (b), and on Pt/sapphire (c) and Pt/Ti/sapphire (d) substrates at 650°C. The scanning area is 4×4 μm^2, and the color scale on the right side is 200 nm.

depletion layer, which is capable to ionize more neutral trapping centers and obtain a thicker depletion layer. Therefore, a larger resistance of the HRS at +2 V is obtained in Pt/Ti/sapphire as compared to that in Si-650, which consequently produces a larger ON/OFF ratio in Pt/Ti/sapphire. On the other hand, the BFO/Pt bottom interface needs to have a low barrier height for the set operation, otherwise only few electrons can be injected from the bottom Pt electrode into the BFO thin film under forward bias, as revealed by samples Si-550 and Pt/sapphire, which have a non-ohmic contact at the BFO/Pt bottom interface and show non-hysteretic I–V curves (Figure S1(c) and (d)). It is noteworthy that this charge-trapping model is in accordance with the gradual change of resistance during the switching. Since the depletion thickness is continuously modulated by the external voltage, the resistance state is tuned consecutively without any sudden change. Recently, a charge-transfer effect has also been adopted to interpret the consecutive resistive switching behavior in organic nonvolatile memories[43].

Based on the above analysis, the critical factor to be taken into account for the engineering of resistive switching devices based on the presented Au/BFO/Pt capacitor structure is to obtain a large difference between the barrier heights at the two electrode/film interfaces. For perovskite oxide thin films, such as BFO, the high deposition temperature inevitably gives rise to the diffusion of Ti throughout the Pt layer and induces a quasi-ohmic contact at the bottom interface. Therefore, it is much easier to construct the asymmetric structure with a top Schottky contact and a bottom ohmic contact. The Ti diffusion, which ever was a serious problem in the fabrication of metal/ferroelectric/metal sandwich structures, thus turns out to be a potential advantage for the construction of resistive switching devices.

Note that the Ti diffusion plays an essentially different role in the bipolar resistive switching of our Au/BFO/Pt capacitor from that reported by Yang et al.[23] in a Pt/TiO$_x$/Pt structure. There a pre-electroforming step is needed for the subsequent switching in the TiO$_x$ thin film. The diffused Ti well controls the forming and switching, and a high yield can be achieved. The "counter-eightwise" hysteretic I–V in their structure is due to the migration of oxygen vacancies (OVs), which modulates the Schottky barrier height at the top Pt/TiO$_x$ interface. However, the "eightwise" I–V hysteresis without any pre-electroforming process in our Au/BFO/Pt capacitor is not consistent with the OVs migration model[25]. Moreover, it is worth noting that the samples Si-650 and Pt/Ti/sapphire always show rectifying behavior regardless of their resistance state. That differs from other resistive switching systems with asymmetric barrier distribution, where the I–V shows rectifying behavior at HRS, but symmetry at LRS[27]. The rectifying behavior at LRS is of importance for eliminating the misreading of resistance state in a crossbar array when there is a neighboring memory cell that is at LRS. The rectifying I–V characteristics at LRS in the presented Au/BFO/Pt structure also hint towards the fact that the set operation is unlikely due to the formation of local filaments penetrating the depletion layer at the Au/BFO interface, which should lead to a non-rectifying I–V at LRS[48]. Therefore, the Ti diffusion in our structure only lowers the barrier height at the BFO/Pt bottom interface, but does not promote the formation of conductive paths throughout the BFO layer.

It is important to mention that rhombohedral and orthorhombic/tetragonal BFO is ferroelectric and that the reversal of polarization may modulate the interface barrier height and induce resistive switching[15,49]. Therefore, it is necessary to clarify the role of polarization switching in the resistive switching in the presented Au/BFO/Pt structures. The polarization-voltage (P–V) loops of sample Si-650 on a Pt/Ti bottom electrode and of sample Pt/sapphire on a Pt bottom electrode are shown in Figure 5. The P–V of Si-650 is roundish and asymmetric due to the large leakage current shown in Figure 1a. The asymmetric P–V characteristics and the decreasing polarization
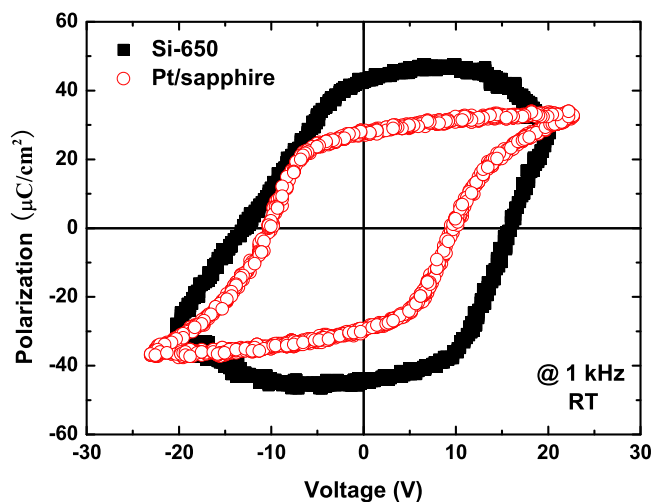

Figure 5 | Polarization-voltage loops of sample Si-650 on Pt/Ti bottom electrode and of sapphire-650 on Pt bottom electrode measured at 1 kHz at room temperature (RT). The polarization measurement of the Si-650 sample is strongly deteriorated by the leakage current.

above ca. 9 V of Si-650 reveal a polarization gradient in this sample[50]. In contrast, sample Pt/sapphire exhibits a symmetric P–V loop and the maximum of polarization at 22 V. This is due to the low leakage current as shown in Figure 1b and from the symmetric I–V curve of the Pt/sapphire sample.

In the sample Si-650 on a Pt/Ti bottom electrode, where resistive switching takes place, the polarization switching is very ineffective due to the large leakage current. But in the insulating sample of Pt/sapphire, where polarization can be switched very well, no resistive switching can be observed. Moreover, the resistive switching occurs at voltages significantly lower than the coercive voltage that can be deduced from Figure 5. Therefore, we conclude that the reversal of polarization does not dominate the resistive switching in our BFO thin films. The lack of resistive switching in the sample Pt/sapphire is likely due to the Schottky contacts formed at both interfaces, consequently the transport of the Au/BFO/Pt stack is always limited by one of the two Schottky interfaces regardless of the voltage polarity.

Discussion

We have shown a forming-free bipolar resistive switching behavior in BiFeO$_3$-based capacitor structures. Without electroforming, the structures show uniform performance and reproducible switching operation by both DC voltage and voltage pulses. The switching is incorporated with a rectifying transport characteristic, this self-rectifying nature enables the fabrication of high-density crossbar arrays with less cross-talk effect caused by the sneak current. The gradual modulation of resistance during the switching process is promising for multilevel data storage and the construction of artificial neuromorphic networks. More importantly, we have demonstrated that the Ti diffusion plays an important role in the formation of an asymmetric interface barrier geometry that is critical for the resistive switching in metal/BiFeO$_3$/metal structures. The proposed electron-trapping model together with the Ti diffusion may be extended to other resistive switching systems and act as a general principle for the design of resistive switching devices based on high-temperature deposited oxide thin films.

Methods

heated by a resistance heater. After the BFO thin film deposition, an Au layer with a thickness of ~100 nm was deposited by DC magnetron sputtering in 2.6 Pa Ar atmosphere. Circular top electrodes with a size of 0.03 mm^2 were achieved by sputtering through a metal shadow mask. The Ti diffusion in the bottom electrode (Pt/Ti layers) of the samples has been analyzed by the energy filtered transmission electron microscopy (EFTEM) and Rutherford backscattering spectrometry (RBS). EFTEM was performed on a FEI Titan 80–300 transmission electron microscope, and RBS was measured with 1.7 MeV He$^+$ ions and detected at a backscattering angle of 170°. The surface morphology of the BFO films has been investigated by atomic force microscopy (AFM) with a multi-mode system from Veeco. The current-voltage (I–V) curves were recorded using a Keithley 2400 source meter, and the polarization-voltage (P–V) loops were monitored by a Sawyer-Tower circuit.

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Author contributions

Y.S. and X.O. designed the work. Y.S., X.O., D.B. and W.L. fabricated the samples and made the electrical measurements, S.Z. made the RBS measurement, X.O. performed the AFM measurement, and A.M. performed the TEM measurement. Y.S., C.W., Y.C., W.Z., and M.H. discussed results, Y.S. wrote the manuscript, T.M., O.G.S., and H.S. revised the text, and all the authors reviewed and approved the manuscript.

Additional information