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High Performance Field-Effect Transistors Based on Partially Suspended 2D Materials via Block Copolymer Lithography

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Abstract: Although various two-dimensional (2D) materials hold great promise in next generation electronic devices, there are many challenges to overcome to be used in practical applications. One of them is the substrate effect, which directly affects the device performance. The large interfacial area and interaction between 2D materials and substrate significantly deteriorate the device performance. Several top-down approaches have been suggested to solve the problem. Unfortunately, however, they have some drawbacks such as a complicated fabrication process, a high production cost, or a poor mechanical property. Here, we suggest the partially suspended 2D materials-based field-effect transistors (FETs) by introducing block copolymer (BCP) lithography to fabricate the substrate effect-free 2D electronic devices. A wide range of nanometer size holes (diameter = 31~43 nm) is successfully realized with a BCP self-assembly nanopatterning process. With this approach, the interaction mechanism between active 2D materials and substrate is elucidated by precisely measuring the device performance at varied feature size. Our strategy can be widely applied to fabricate 2D materials-based high performance electronic, optoelectronic, and energy devices using a versatile self-assembly nanopatterning process.

Keywords: block copolymer lithography; nanopatterning; two-dimensional (2D) materials; substrate effect; suspended structure

Citation: Kim, S.; Lee, S.E.; Park, J.H.; Shin, J.Y.; Lee, B.; Lim, H.Y.; Oh, Y.T.; Hwang, J.P.; Seon, S.W.; Kim, S.H.; et al. High Performance Field-Effect Transistors Based on Partially Suspended 2D Materials via Block Copolymer Lithography. *Polymers* **2021**, *13*, 566. https://doi.org/10.3390/polym13040566

Academic Editor: Oleg V. Borisov
Received: 20 January 2021
Accepted: 10 February 2021
Published: 14 February 2021

1. Introduction

Various two-dimensional (2D) materials, such as graphene, semiconductor transition metal dichalcogenides (TMDs), black phosphorus (BP), insulating hexagonal boron nitride (h-BN), and 2D carbides and nitrides (MXenes) have attracted great interest due to their atomically thin structures and versatile electrical and optoelectronic properties such as high flexibility/transparency and outstanding carrier mobility [1–5]. In particular, many studies attempted to replace conventional silicon semiconductor devices by using atomically layered 2D materials, especially for flexible and stretchable electronics [6–9]. Despite these many advantages of 2D materials as an active layer of electronic devices, they inherently have a huge disadvantage of being extremely sensitive to the surrounding environment, e.g., substrates, due to their single-atom-thickness [10–13]. The charged impurities resulting from surface roughness significantly deteriorate the performance of 2D materials-based electronic devices and become major obstacles for its practical application [14]. To solve the problem induced by the interaction between 2D materials and substrate, several studies have focused on devising methodologies to suspend 2D materials in order to improve device performance towards intrinsic transport properties [15–23]. Usually, they have

used micro-scale trench structures fabricated via a conventional top-down microfabrication process [24,25]. However, these approaches have produced other problems, such as a complicated and expensive fabrication process, a poor mechanical property, and especially a low mass-production yield. In this aspect, a bottom-up nanofabrication process based on self-assembly can be a great alternative to fabricate the substrate effect-free 2D electronic devices.

Here, we demonstrate graphene field-effect transistors (G-FETs) that are partially suspended on a nanoporous silicon substrate using self-assembly of a polystyrene-*block*-poly(methylmethacrylate) (PS-*b*-PMMA) diblock copolymer thin film. Block copolymer (BCP) lithography is an emerging self-assembly technique for the large-area patterning of surfaces with regular nanosized features [26–29]. Unlike the conventional approach where the entire channel area of 2D material-based field-effect transistors (FETs) is suspended, our strategy allows a partial suspension of their channel with a uniform structure and high density. Through this method, we prevent the collapse or degradation of suspended graphene, and obtain excellent structure stability in terms of mechanical properties. The G-FETs with superior performance than conventional graphene transistors are successfully fabricated by minimizing a contact area between graphene and substrate which decreases extrinsic scattering by surface phonons at the SiO_2 substrate, which directly contacts with graphene. In this study, we fabricate nanopatterned substrates with various feature sizes by controlling the etching process and investigate the mechanism of substrate effect on the device performance. As a result, in the nanopatterned substrate with decreased substrate effect, we confirm a maximum of 3.2 times higher field-effect mobility (μ) by measuring the electrical properties of graphene devices.

2. Materials and Methods

2.1. Materials

PS-*b*-PMMA diblock copolymer (M_n = 205,000 g/mol, Polymer Source INC) and poly (styrene-*ran*-methyl methacrylate) (PS-*r*-PMMA) random copolymer brush (M_n = 6400 g/mol, Polymer Source INC) were used to fabricate a BCP nanotemplate on silicon oxide (thickness ~90 nm) wafer (highly p-doped). For 2D materials-based device fabrication, graphene was mechanically exfoliated from highly oriented pyrolytic graphite (HOPG, SPI supplies, Grade SPI-2) [30].

2.2. Fabrication of Paritally Suspended G-FETs

2.2.1. Pre-Treatment of Substrate

A silicon oxide wafer was cleaned with acetone, isopropyl alcohol (IPA), and deionized (DI) water with 20 min sonication for each washing step. Subsequently, silicon oxide wafer was sufficiently oxygen plasma treated in vacuum chamber. This process removed most of the impurities on the substrate and provided a highly dense hydroxyl group (–OH) on silicon oxide wafer (Figure 1a) [31,32].

2.2.2. BCP Self-Assembly Process

The surface of silicon oxide wafer was chemically modified by a PS-*r*-PMMA random copolymer brush to provide identical interfacial tensions for the PS and PMMA blocks [33,34]. The PS-*r*-PMMA brush layer (thickness ~40 nm) was deposited by spin-coating process (1 wt% in toluene, 1000 rpm, 60 s) and subsequent thermally annealed at 160 °C for 48 hrs in a vacuum chamber (Figure 1b) [35]. Then, the un-grafted random brush layer was removed by sonication in toluene for 15 min by 3 times. After surface modification, a symmetric diblock copolymer, PS-*b*-PMMA thin film (thickness ~120 nm) was spin-casted (2 wt% in toluene, 1600 rpm, 60 s). Afterwards, thermal annealing was conducted at 220 °C for 48 hrs in a vacuum chamber to produce the surface perpendicular BCP nanodomain (Figure 1c).

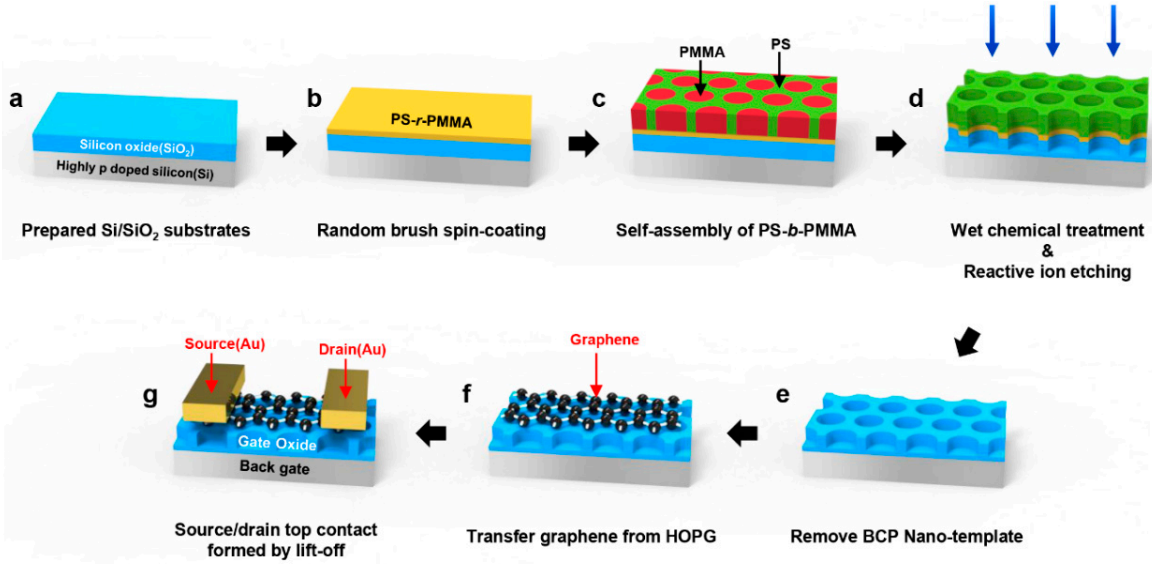


Figure 1. Schematic illustration for the fabrication of partially suspended graphene field-effect transistors (G-FETs) process: (**a**) A silicon oxide wafer is cleaned in sequence with acetone, isopropyl alcohol, and deionized water by sonication. (**b**) A poly(styrene-*ran*-methyl methacrylate) (PS-*r*-PMMA) thin film is spin-coated on a silicon oxide substrate and thermally annealed. (**c**) After washing of the un-grafted PS-*r*-PMMA brush with toluene, a block copolymer (BCP) thin film is spin-coated from solution of the polystyrene-*block*-poly(methylmethacrylate) (PS-*b*-PMMA) diblock copolymer in toluene on a silicon oxide substrate and thermally annealed. (**d**) The BCP nanotemplate is treated in sequence with ultraviolet light, acetic acid, and reactive ion etching process to fabricate a nanopore array on silicon oxide substrate. (**e**) The remaining PS block was removed by sonication in toluene for 60 min by 3 times. (**f**) Graphene is transferred onto nanopatterned silicon oxide substrate. (**g**) Source/drain electrodes are formed with Cr/Au layers.

2.2.3. SiO_2 Layer Etching with BCP Nanotemplates

Exposure of the BCP thin film to UV radiation (365 nm, dose of 7.2 J/cm^2) degraded the PMMA block and induced cross-linking of the PS block [36]. Afterwards, rinsing with dilute acetic acid led to a nanoporous BCP thin film in direct contact with the substrate [37]. For complete removal of PMMA residues, O_2/Ar gas mixture plasma (source power = 150 W, 5 s) was applied (Figure 1d). During plasma treatment, working pressure and gas flow rate was kept at 92 mTorr and 5/50 sccm (O_2/Ar), respectively. After PMMA block was removed, silicon oxide layer was etched with CF_4 gas (source power = 60 W, 30 s, 120 mTorr, 20 sccm) plasma condition [38]. Lastly, the remaining PS block was removed by sonication in toluene for 60 min by 3 times (Figure 1e).

2.2.4. Fabrication of Bottom-Contact G-FETs

The nanopatterned silicon oxide wafer was washed with acetone, IPA, and DI water by sonication for 20 min, sequentially. Monolayer graphene was prepared by mechanically exfoliated HOPG and transferred on the nanopatterned silicon oxide wafer via conventional scotch tape method (Figure 1f) [30]. A thickness of graphene was measured by optical imaging contrast of flakes, and further confirmed by Raman spectroscopy and atomic force microscopy (AFM). Transferred graphene was used to fabricate bottom-contact G-FETs with channel length/width = 2/1 μm using a conventional microfabrication process (Figure 1g) [39].

2.3. Characterization

2.3.1. Surface Morphology of Nanopatterned Silicon Oxide Layer

The nanostructure of silicon oxide layer was characterized by field-emission scanning electron microscopy (FE-SEM, Gemini SEM 300, ZEISS, Jena, Germany) and transmission electron microscopy (TEM, Tecnai F20 G2, FEI INC, Hillsboro, OR, USA), respectively.

2.3.2. Raman Spectroscopy of Graphene

Graphene on a flat and nanopatterned silicon oxide thin film was characterized by Raman spectroscope (2GTE70, RENISHAW INC, Wotton-under-Edge, UK) using 512 nm laser.

2.3.3. Semiconductor Characterization System

Transfer characteristics of G-FETs was measured by Keithley 4200-SCS parameter analyzer with a probe station (ST-500-1-4CX, JANIS) under atmosphere condition. The highly boron doped silicon oxide wafer was used as bottom-gate contact of G-FETs. Transfer characteristics was measured with gate voltage (V_{GS}) in the range of −20~+20 V with 0.05 V interval.

3. Results and Discussion

3.1. Nanopatterning of Substrate Using BCP Self-Assembly

The final morphology of the nanopattern on the substrate greatly depends on the etching gas plasma process time. Figure 2a shows the evolution of hole diameter and depth of nanopattern on the substrate at varied CF_4 gas plasma process time. When CF_4 gas plasma was applied for 20 s, the appropriately etched substrate (AES) has average hole diameter/depth as 31/12 nm, respectively (Figure 2b). Here AES represents the substrate with same size BCP nanopattern that was used as a dry etching mask and nanopattern transferred to the silicon oxide substrate. This is the case where nanopattern on the silicon oxide substrate have a perfect vertical sidewall. We also fabricate over etched substrate (OES) with minimized contact area between substrate and graphene by increasing CF_4 gas plasma etching time (45 s). Here, OES is a substrate with larger size of nanopattern transferred to the silicon oxide substrate than the size of BCP nanopattern by increasing dry etching time. In the case of OES, the substrate has a nanopattern with a thinner sidewall than the that of AES. Figure 2c shows the scanning electron microscope (SEM) image of OES with the average hole diameter/depth of 43/20 nm. The transmission electron microscopy (TEM) image and corresponding height cross-sectional profile of OES are shown in Figure 2d,e, respectively. Figure 2f represents the holes diameter size distribution (average diameter of 31/43 nm for AES/OES) of nanopatterns in a 1 μm × 1 μm area (total number of holes = 300) of AES and OES.

3.2. Transfer of Graphene to the Substrate and G-FETs Fabrication

To investigate the substrate effect regarding 2D materials-based FETs, we transfer mechanically exfoliated graphene on flat silicon oxide substrate (FS), AES, and OES, respectively. Figure 2g shows optical microscopy (OM) image and a representative cross-sectional profile of monolayer graphene transferred to FS with a thickness of 0.42 nm. Considering the thickness of monolayer graphene (0.34 nm), we conclude that the transfer process of graphene to the substrate has a high technical completion.

Figure 2h shows the top and tilted view SEM images of a graphene transfer printed on AES for G-FETs fabrication. Figure 2i represents the Raman spectra of monolayer graphene transferred to FS, AES, and OES, plotted in black, red, and blue colored lines, respectively. In all samples, no D-band is observed while G-band is observed from FS and AES substrates at 1589 cm^{-1}. Interestingly, G-band was left shifted (1585 cm^{-1}) at OES, indicating G-band is shifting left as the porosity of substrate increases. While the 2D-band was observed at 2678 cm^{-1} from FS and AES, the band is observed at 2676 cm^{-1} for OES, meaning the band is left shifted as in the case of G-band. In addition, we found that the intensity ratio of 2D-band to G-band (I_{2D}/I_G) is proportional to the porosity of substrate; 1.73, 2.09, and 2.90 for FS, AES, and OES, respectively.

Because I_{2D}/I_G means the degree of doping on the graphene, the increased value indicates that it reaches a more pristine state [40]. When the pore size of BCP nanopattern increases, the contact area of graphene with substrate decreases and it leads to the minimized substrate effect. Therefore, corresponding graphene shows property close to its

intrinsic state and its I_{2D}/I_G is increased. Figure 3a and b show the optical microscopy and top view SEM images of bottom-contact G-FETs on AES, respectively.

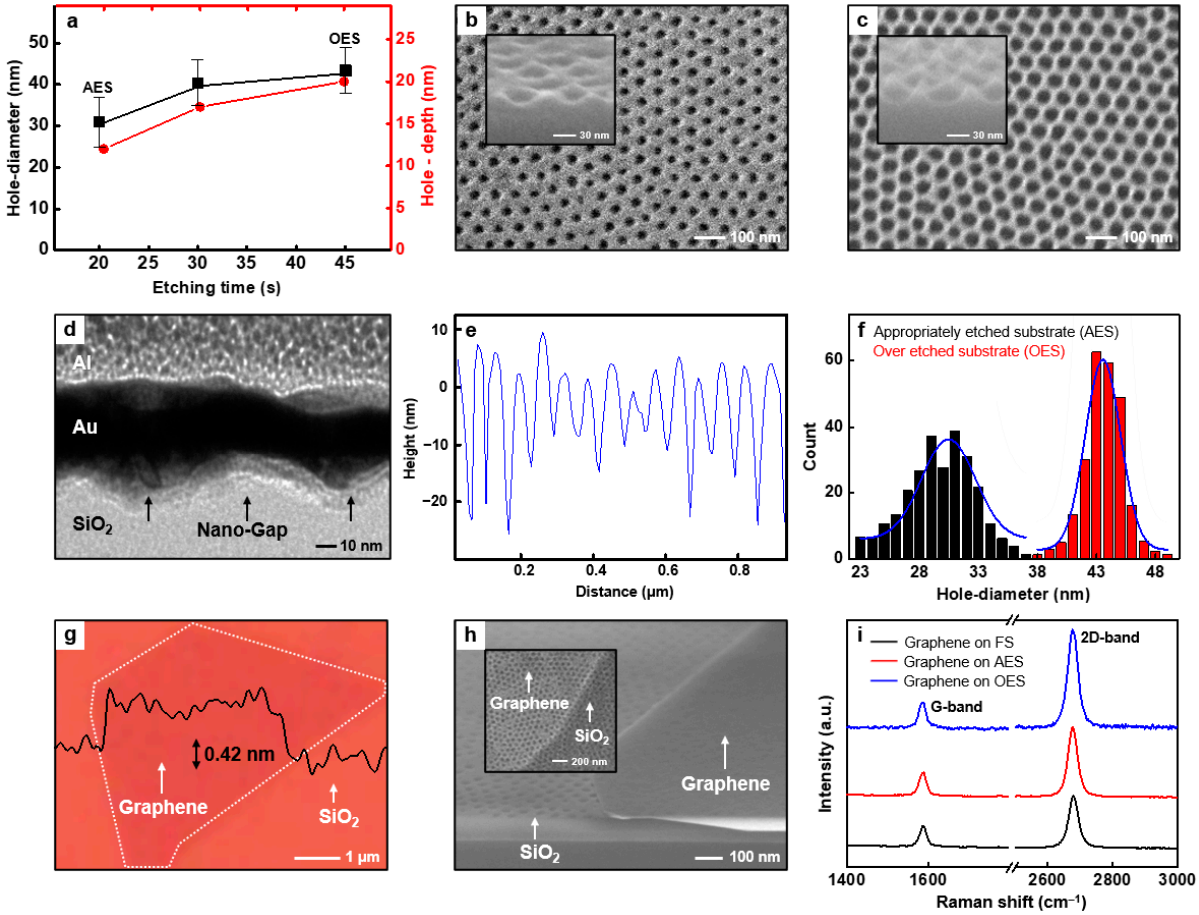


Figure 2. (**a**) A graph for hole diameter/depth vs. etching time. Top view SEM images of (**b**) appropriately etched substrate (AES) and (**c**) over etched substrate (OES). (**d**) A TEM image and (**e**) cross-sectional profile of OES. (**f**) Column chart of hole diameter vs. count of number of holes on the AES and OES in 1 μm^2 area. (**g**) An OM image and cross-sectional profile of transferred monolayer graphene onto flat silicon oxide substrate (FS, thickness of graphene = 0.42 nm). (**h**) Tilted & top view scanning electron microscope (SEM) images of transferred graphene onto AES during G-FETs fabrication. (**i**) Raman spectra of monolayer graphene on FS, AES, and OES.

3.3. Calculation of Capacitance of Insulating Layer

The capacitance of dielectric layer needs to be precisely calculated in order to measure electrical characteristics of G-FETs on nanopatterned substrates. Figure 4a,b show the schematic illustrations and capacitance circuits of dielectric layer from FS and nanopatterned substrates (AES and OES), respectively. In general, the capacitance (C) of metal–insulator–metal (MIM) capacitor structure can be expressed as Equation (1):

$$C = \varepsilon \frac{A}{d} \quad (1)$$

ε, A, and d represent the permittivity of the dielectric material, the surface area of the two plates, and the separation distance between the two plates, respectively. In the case of FS (Figure 4a), it is composed of 90 nm-thick SiO_2 thin film as a dielectric layer. On the other hand, nanopatterned substrates (AES and OES) have dielectric layers of 90 nm-thick SiO_2 layer (blue dotted rectangles) and air-SiO_2 heterostructured layer (red dotted rectangles) connected in parallel (Figure 4b). The thickness of SiO_2 thin film in the heterostructured

layer with suspended graphene on AES and OES are 78 and 70 nm, respectively. The area ratio of hole in this regime is 22% and 43% for AES and OES, respectively. The capacitance of 90 nm-thick SiO_2 is calculated as 38.7 nF cm^{-2} because the capacitance of the 300 nm-thick SiO_2 is well-known as 11.6 nF cm^{-2} and the thickness of SiO_2 and its capacitance are inversely proportional [41]. In the case of nanopatterned substrates (AES and OES), the values of ε_{air} = 1.0 and ε_{SiO2} = 3.9 are used to calculate the capacitance of the air. As a result, the capacitances of the 12/78 nm-thick air/SiO_2 on AES and the 20/70 nm-thick air/SiO_2 on OES are calculated as 74.4/44.6 nF cm^{-2} and 44.6/49.7 nF cm^{-2}, respectively. The capacitance of serially connected capacitors can be calculated as Equation (2):

$$C_{total} = \frac{C_1 C_2}{C_1 + C_2} \quad (2)$$

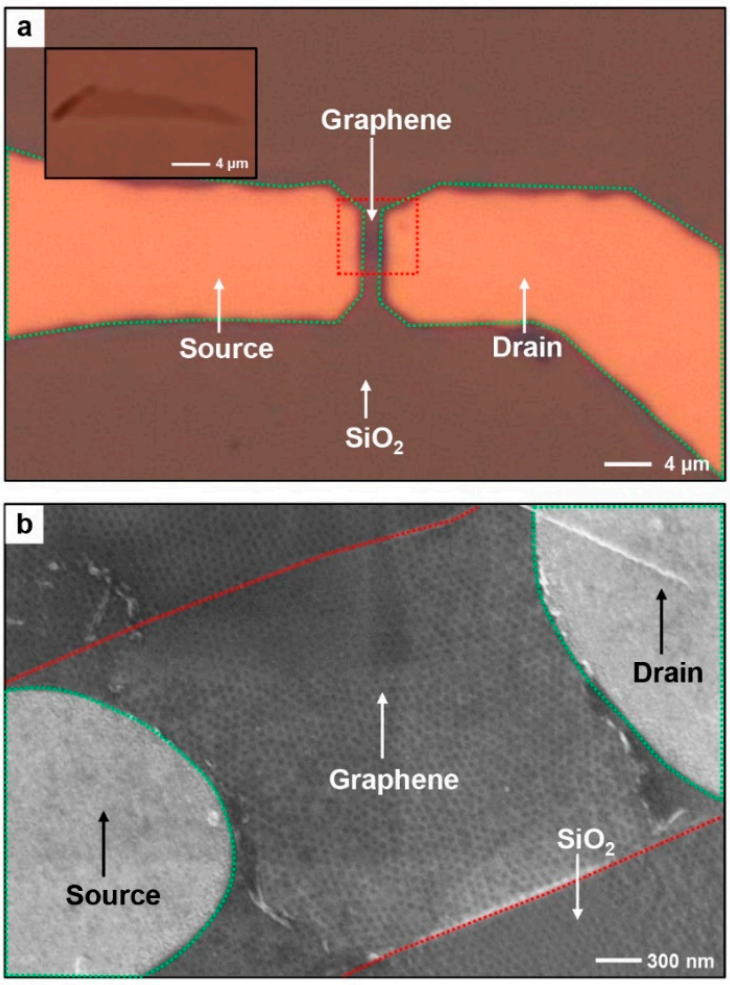
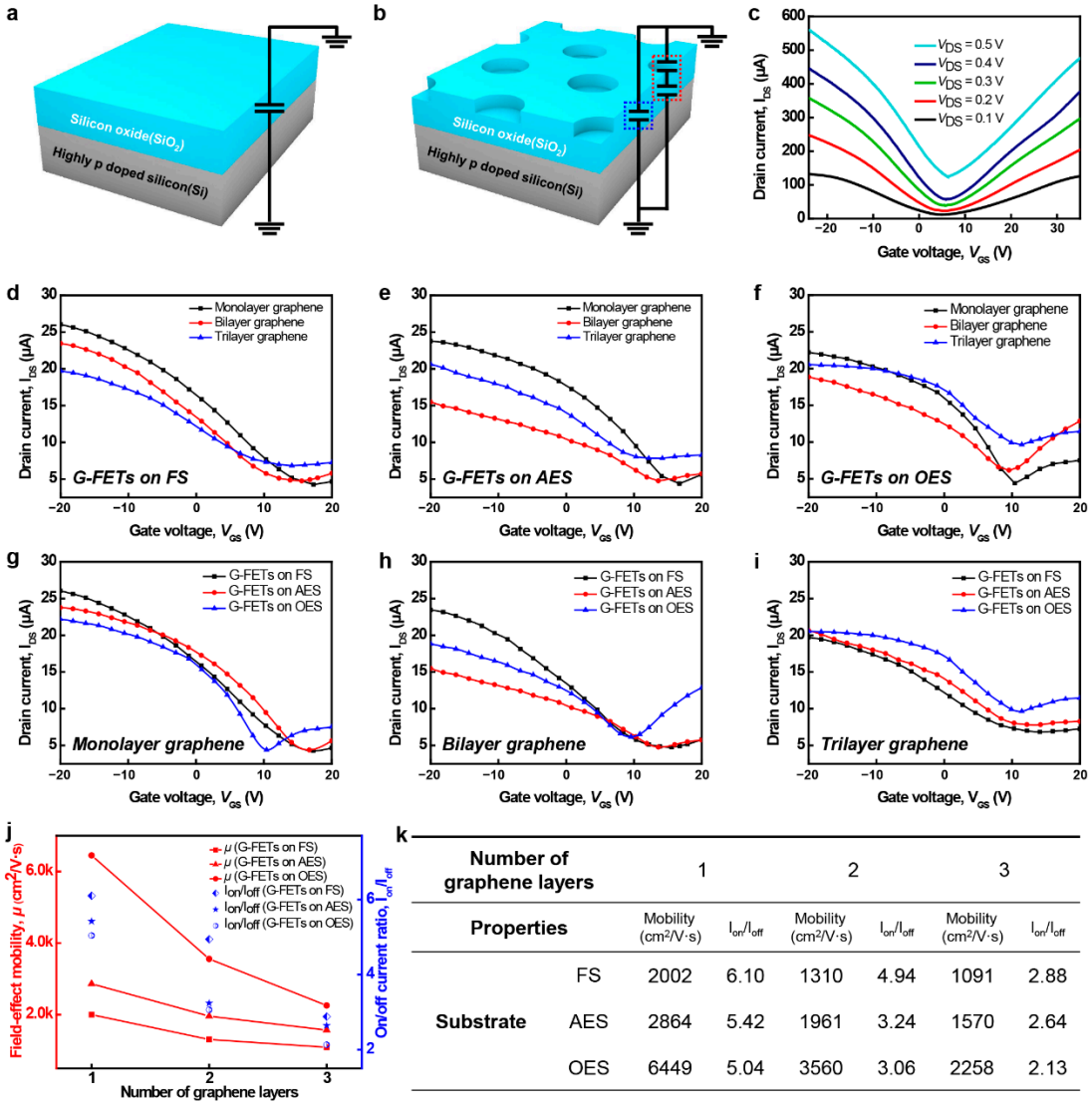


Figure 3. A top view (**a**) OM and (**b**) SEM image of partially suspended G-FETs on AES. Average pore diameter of AES is 31 nm and monolayer graphene is used for the G-FETs fabrication.



k

Number of graphene layers		1		2		3	
Properties		Mobility (cm²/V·s)	I_{on}/I_{off}	Mobility (cm²/V·s)	I_{on}/I_{off}	Mobility (cm²/V·s)	I_{on}/I_{off}
Substrate	FS	2002	6.10	1310	4.94	1091	2.88
	AES	2864	5.42	1961	3.24	1570	2.64
	OES	6449	5.04	3560	3.06	2258	2.13

Figure 4. The schematic illustration of the cross-sectional dielectric layers along with their equivalent capacitor circuits for the (**a**) FS and (**b**) nanopatterned substrates (AES and OES). (**c**) Transfer curves of monolayer G-FETs on OES for different values of V_{DS} (V_{DS} = 0.1~0.5 V, internal = 0.1 V). (**d**–**i**) Transfer curves of G-FETs with different number of graphene layers on various substrates. (**j**,**k**) Field-effect mobility (μ) and on/off current ratio of G-FETs vs. number of graphene layers on various substrates.

On the other hand, the capacitance of parallelly connected capacitors can be obtained from Equation (3):

$$C_{total} = C_1 + C_2 \quad (3)$$

In the case of air-SiO_2 heterostructured dielectric layer on AES, the capacitance $C_{air\text{-}SiO2}$ can be calculated using Equation (2) as 27.9 nF cm^{-2} because 12 nm-thick air and 78 nm-thick SiO_2 are serially connected. Additionally, we consider a parallelly connected 90 nm-thick SiO_2 layer of 38.7 nF cm^{-2} and air-SiO_2 heterostructured dielectric layer of 27.9 nF cm^{-2} in 78:22 ratio, and total capacitance C_{AES} was calculated using Equation (3) as $C_{AES} = 0.78 \times C_{SiO2} + 0.22 \times C_{air\text{-}SiO2}$ = 36.3 nF cm^{-2}. Likewise, in the case of OES, there are parallel connections with 90 nm-thick SiO_2 layer of 38.7 nF cm^{-2} and air-SiO_2 heterostructured dielectric layer of 23.5 nF cm^{-2} in 57:43, and total capacitance C_{OES} was calculated as $C_{OES} = 0.57 \times C_{SiO2} + 0.43 \times C_{air\text{-}SiO2}$ = 32.2 nF cm^{-2}.

3.4. Analysis of G-FETs Electrical Performance

Figure 4c–i show the transfer curves of the G-FETs with different layers of graphenes and types of substrates. Figure 4c represents the transfer characteristics of G-FETs on OES with a single layer graphene at varied drain-source voltage (V_{DS} = 0.1~0.5 V, internal = 0.1 V), indicates that they possess a large working range compatible with diverse power settings (power of device = $I_{DS} \times V_{DS}$). Figure 4d–f show the results of I_{DS}–V_{GS} curves (V_{DS} = 0.1 V) of G-FETs with different graphene layers on FS (Figure 4d), AES (Figure 4e), and OES (Figure 4f), respectively. From these graphs, we found that the increase of number of graphene layers leads to the raise of the minimum drain current (drain current at the Dirac point) as well as the decrease of on/off current ratio of G-FETs. Figure 4g–i represent the graphs of I_{DS}–V_{GS} curves (V_{DS} = 0.1 V) from G-FETs composed of monolayer (Figure 4g), bilayer (Figure 4h), and trilayer (Figure 4i) graphene on different types of substrates. The increase of substrate porosity reduced the contact area between substrate and transferred graphene, which results in the raise of slope in transfer curves as well as the shift of graph towards left. The increase of the slope indicates the increase of dI_{DS}/dV_{GS} (transconductance). This is due to the improvement of devices performance by minimizing extrinsic scattering by surface phonons at the SiO_2 substrate [42]. Also, the left shift of transfer curves at increased substrate porosity represents that G-FETs on OES are more n-doped compared to devices on FS or AES. It is well-known that graphene is slightly p-doped when contacting with silicon oxide layer due to the interfacing effects of the oxygen (O)-terminated substrate [43]. However, in the case of graphene on nanopatterned substrates (AES and OES), the contact area between graphene and substrate is minimized and this is the reason of a graphene with relatively n-doped property compared to a graphene fully contacted with FS. As shown in Figure 4g–i, this phenomenon is universal regardless of number of graphene layers and the effects are getting bigger at fewer graphene layers. Figure 4j shows the comparison of μ and bias current on/off ratio (I_{on}/I_{off}) of G-FETs according to the surface morphology of substrate and number of graphene layers based on transfer curves from Figure 4d–i. The μ was calculated using following equation:

$$\mu = \frac{L g_m}{W C_G V_{DS}} \tag{4}$$

Here, L, G, W, and C_G represents channel length, transconductance, channel width, and gate capacitance of a dielectric layer, respectively. For G, it is calculated from dI_{DS}/dV_{GS} of transfer curves of G-FETs and for C_G, the calculated C_G value at varied substrates were used. In the case of G-FETs composed of monolayer graphene, μ with OES increased more than three folds than that of G-FETs on FS (from 2002 $cm^2/V{\cdot}s$ to 6449 $cm^2/V{\cdot}s$), and the value of I_{on}/I_{off} is decreased from 6.10 to 5.04. Not only monolayer, but also bi- and tri-layer G-FETs show the similar results. Figure 4k summarizes calculated μ and I_{on}/I_{off} of G-FETs with different layers of graphene and types of substrates.

4. Conclusions

The 2D materials were actively used in the next generation electronics/optoelectronics devices [44] due to its promising potential. In some applications, however, there has been innate limitations because such devices performance was significantly deteriorated by interaction between substrate and 2D materials. To overcome this limitation, we engineer the nanostructures of substrate to stably suspend 2D materials and suggested the solution for the performance degradation problems. We demonstrate the partially suspended 2D materials-based FETs by introducing BCP lithography to fabricate the substrate effect-free G-FETs with a high mechanical stability and devices performance. Through nanopatterning of self-assembled BCP, we fabricate various nanoporous substrates (AES and OES) with excellent regularity and large-area uniformity. While the graphene transferred to FS showed a p-doped property due to contact doping with substrate, graphene transferred to nanopatterned substrates (AES and OES) show intrinsic properties because of partial suspension on the substrate. Considering that graphene on AES and OES also showed a relatively

n-doped feature compared to the one transferred to FS, it was found that graphene doping level is severely affected by the geometry of substrates. In addition, G-FETs on OES showed maximum 3.2 folds higher μ compared to devices on FS because of the reduced charged impurities and extrinsic scattering. Therefore, we believe that this strategy can contribute to performance enhancements of future electronic and optoelectronic applications based on 2D materials.

Author Contributions: Investigation, S.K., S.E.L., J.H.P., J.Y.S., B.L., H.Y.L., Y.T.O., J.P.H., S.W.S., S.H.K., T.S.Y.; Supervision, B.H.K.; Writing—review & editing, S.K. and B.H.K. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by (1) The National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2020R1C1C1014980), (2) Creative Materials Discovery Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT (NRF-2018M3D1A1058972), (3) Nanomaterial Technology Development Program (NRF-2016M3A7B4905613) through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning, and (4) Korea Institute for Advancement of Technology (KIAT) grant funded by the Korea Government (MOTIE) (P0012770).

Conflicts of Interest: The authors declare no conflict of interest.

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