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REVIEW ARTICLE

Miniaturization for wearable EEG systems: recording hardware and data processing

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Abstract

As more people desire at-home diagnosis and treatment for their health improvement, healthcare devices have become more wearable, comfortable, and easy to use. In that sense, the miniaturization of electroencephalography (EEG) systems is a major challenge for developing daily-life healthcare devices. Recently, because of the intertwined relationship between EEG recording and processing, co-research of EEG recording hardware and data processing has been emphasized for whole-in-one miniaturized EEG systems. This paper introduces miniaturization techniques in analog-front-end hardware and processing algorithms for such EEG systems. To miniaturize EEG recording hardware, various types of compact electrodes and mm-sized integrated circuits (IC) techniques including artifact rejection are studied to record accurate EEG signals in a much smaller manner. Active electrode and in-ear EEG technologies are also researched to make small-form-factor EEG measurement structures. Furthermore, miniaturization techniques for EEG processing are discussed including channel selection techniques that reduce the number of required electrode channel and hardware implementation of processing algorithms that simplify the EEG processing stage.

Keywords Electroencephalography (EEG) · Miniaturization · Integrated circuits (IC) · Active electrode · In-ear EEG · Channel selection · Hardware implementation · Field-programmable gate array (FPGA)

1 Introduction

Healthcare devices have become more wearable and comfortable as demands for easy-to-use devices in various applications rapidly increase. Over the past few decades, more people have desired at-home diagnosis and treatment for their health improvement [1, 2]. In particular, since the COVID-19 pandemic started in 2020, caring for patients without face-to-face contact has become the main issue. With the development of the self-diagnosis kit, a strong desire for simple, user-friendly, and long-term usable wearable healthcare devices is further increasing [3–5].

In this trend, several comfortable systems are being developed to measure and analyze various kinds of biosignals such as Electrcardiography (ECG), Electromyography (EMG), Photoplethysmography (PPG), and Electroencephalography (EEG). Among them, EEG especially receives huge interest because it can monitor human brain conditions in a non-invasive manner and has a wide range of applications [6–8]. For instance, EEG is applicable for mental disorder management, epilepsy treatment, sleep monitoring, and neurofeedback. Furthermore, EEG enables people with limited mobility to control devices using their thoughts due to a brain-computer interface (BCI) technology [9].

However, most current EEG measurement devices require professional assistance due to their large size and the complex installation procedures [10]. For this reason, most of the devices are used for medical or experimental purposes only, not for everyday life [11, 12]. Therefore, for everyday-use

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EEG systems, the main research goal is to implement miniaturized and easy-to-use EEG hardware by (1) decreasing the size of the electrodes, (2) designing small-form-factor integrated circuits (IC), and (3) simplifying the structures of the EEG device. With the demands for miniaturization in the physical dimension of EEG recording hardware, miniaturization in computational loads in EEG data processing is also essential. For the past few decades, machine learning algorithms such as support vector machines (SVM) [13], linear discriminant analysis (LDA) [14], and deep learning [15] have been used for the BCI system. However, current algorithms for EEG classification are computationally heavy. Therefore, raw data transmission to host computers or data servers that perform heavy data processing is unavoidable, making the overall EEG system bulky, energy-inefficient, and non-portable. As such, for the miniaturized and easy-to-use EEG systems, 1) alleviation of the computational load by channel selection (CS) and 2) hardware implementation of EEG data processing are required.

Several review papers addressing miniaturization in EEG systems by focusing on either EEG recording or EEG data processing have been published [16–18]. However, co-research of EEG recording and data processing is essential for a miniaturized whole-in-one EEG healthcare system [19]. Therefore, this paper reviews methodologies toward EEG miniaturization by focusing on the two perspectives altogether. The rest of the paper is organized as follows. Section 2 describes the miniaturization of EEG recording hardware including electrodes, integrated circuits, and device structures. Section 3 shows channel selection techniques that simplify the EEG processing stage, and hardware implementation of EEG data analysis. Finally, Sect. 4 concludes this review.

2 Miniaturization techniques for EEG recording hardware

2.1 EEG electrodes

The electrode has a role of front-end contact with the skin when recording EEG, so it needs to be minimized preferentially to miniaturize the EEG measurement devices. Since human EEG was first measured by Hans Berger (1873-1941), various types of electrodes have evolved with the change of their shapes and configurations. Early models are bridge electrodes or cup electrodes which fix the position of electrodes firmly on the scalp, and additional electrolyte gel was used to increase skin adhesion [10]. However, these electrodes have difficulty in usage because the size is bulky and additional supporting structures are required. In addition, the conductive gel is not suitable for long-term daily-life usage, because wet electrodes require additional preparation processes such as hair waxing. Furthermore, the gel becomes dried out over time which causes signal distortion [20, 21].

Therefore, attempts to measure EEG with small size dry-contact electrodes have been made. Needle-type electrodes which measure clean EEG signal in very narrow areas have been developed [22, 23]. With the help of flexible substrates such as polydimethyl-siloxane (PDMS), ethylene propylene diene monomer (EPDM), and SU-8, skin adhesion of needle electrodes is increased, resulting in better signal quality [24, 25]. Ultra-small electrodes have also been manufactured in which microneedle-array electrodes (MAEs) penetrate the stratum corneum so that EEG can be measured even on hairy scalp [26, 27]. In addition, major skin-electrode contact type has gradually been changed to a dry fashion without using any conductive gel [28, 29]. Recently, semi-dry electrodes which add a very small amount of paste only when needed, and non-contact electrodes which do not require skin-metal contact are also utilized [30–32].

However, as the area of the electrodes becomes smaller, the electrode-skin impedance (ESI) increases accordingly. Therefore, the input impedance of the following analog-front-end must be increased to avoid signal attenuation [33, 34]. In addition, high electrode-skin resistance makes thermal noise, which makes fatal adverse effects in measuring μV level EEG signal [6, 35]. In order to solve these problems, methods to increase the effective surface area while reducing the geometrical dimension of the entire electrode have been proposed. Surface roughening techniques by utilizing nanoporous platinum, platinum black electro-patterning, Ag-TiN coating, and nano-patterning based on pillar or arch shapes are developed to measure EEG precisely when using extreme small electrodes [36–38]. Such electrodes are actively manufactured in various bio-potential measurement fields and are expected to get more increasing interest in wearable ultra-small EEG measurement.

2.2 EEG integrated circuits

Semiconductor application-specific integrated circuit (ASIC) is a breakthrough technology that integrates analog-front-end and digital-back-end in a single small-form-factor unit. It plays a role of amplifying, filtering, analog-to-digital converting, and complicate signal controlling all at once [39–42]. Metal-oxide-semiconductor field-effect transistor (MOSFET) has continuously decreased in size of a few nano-meter scales over the past few decades. In these days, it is possible to design IC chips with many functional blocks in extremely small areas. Such ultra-small transistor technology has extreme performance in a low power operation and high current-driving characteristics especially on a sub-threshold operation [43]. Therefore, IC chips capable of inserting dozens of channels within a small

area are currently being designed, and those are essential for the miniaturization of EEG measurement devices [44–46].

Unfortunately, lots of problems arise when trying to use EEG recording IC chips. MOS transistor generates a constant value of thermal noise regardless of frequency due to the random motion of electrons. In addition, flicker noise caused by trapped charge carriers between the gate oxide and the silicon substrate also occurs, which shows 1/f characteristics [47, 48]. Since short-channel MOSFET produces hot electron effects and flicker noise is inversely proportional to MOSFET oxide capacitance between gate and channel, smaller MOS transistor has worse intrinsic low-frequency noise. In addition to the problems from the IC chip itself, miniaturized dry-contact electrodes have high electrode-skin impedance near a few MΩ or GΩ levels, which makes the system more vulnerable to motion artifacts due to ESI variation. Furthermore, as the device becomes simpler and rigid fixing architecture has been removed, it is hard to fix the electrode at a certain position, resulting in baseline wander [49]. These lots of noise and artifact components worsen signal-to-noise ratio (SNR) in measuring low-frequency EEG signal in the 0.5-100Hz range.

Ultra-small IC chip design technology reduces such low-frequency interference and many kinds of artifacts within an invisible scale area. First, auto-zeroing, a kind of discrete-time compensation technique, is a method that uses a switched-capacitor to sample an error of an amplifier for one clock phase and then remove it from the subsequent clock phase [50]. Second, chopping, a kind of continuous-time modulation technique, uses a paired chopper made of switches to avoid the intrinsic offset in the amplifier. As shown in Fig. 1a, the first chopper modulates the signal to the high-frequency level. After the following amplifier and the next chopper, the modulated signal is demodulated back, while the offset is modulated to the chopping frequency and its harmonics. A low-pass filter is then used to remove the modulated offset, resulting in a clean EEG signal [51]. Additional ripple reduction loop (RRL) can also be designed to remove extra output triangular ripple wave generated when the chopped offset of the input stage is filtered by the Miller

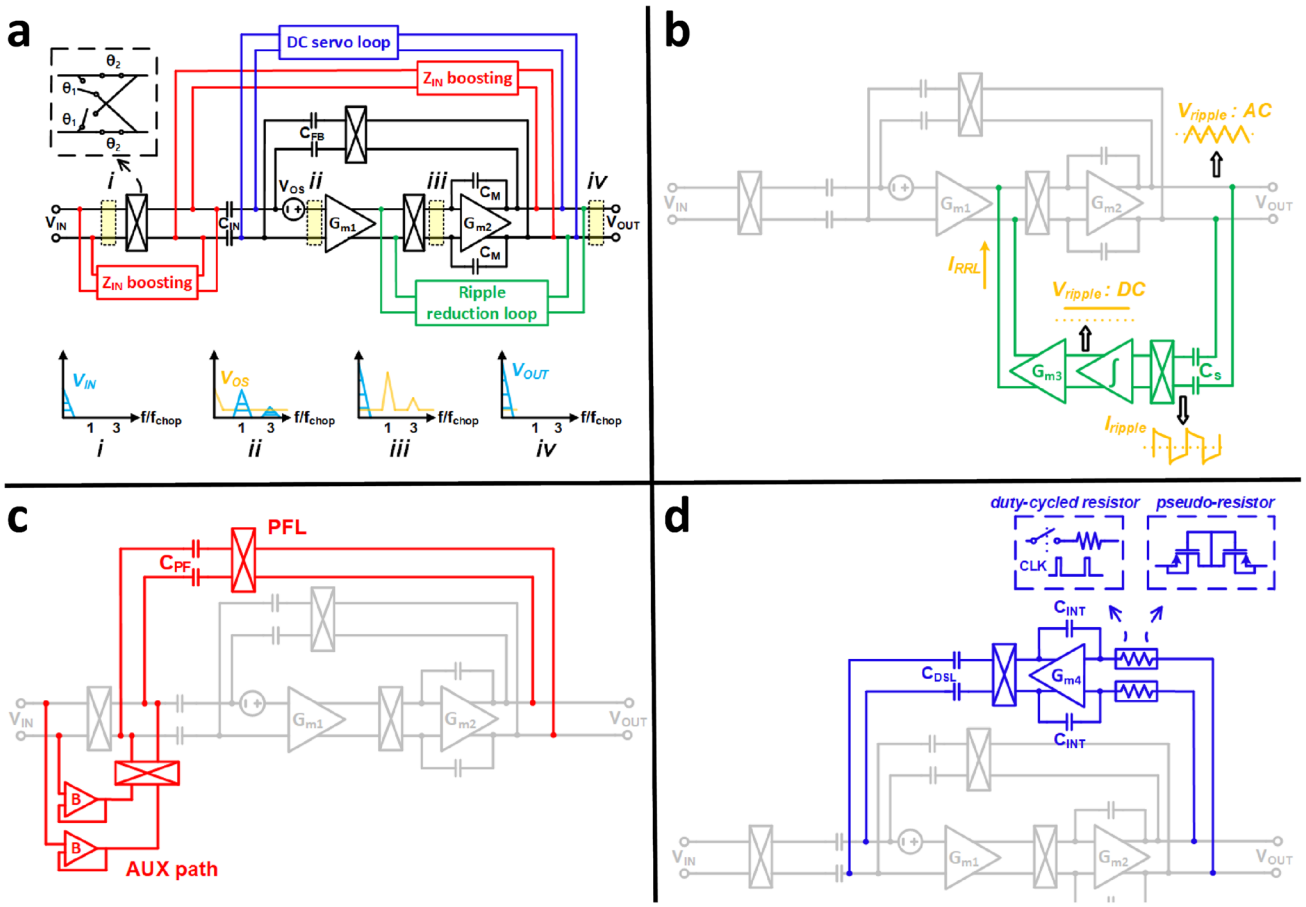

Fig. 1 Various IC techniques for artifacts reduction in EEG recording. **a** Capacitively-coupled chopping instrumentation amplifier (CCIA) with several IC techniques. The graphs (*i-iv*) show how the input signal (V_{IN}) and the offset (V_{OS}) are modulated at each node (yellow box) to generate clean output EEG signal (V_{OUT}); **b** Ripple reduction loop (RRL); **c** Input impedance boosting techniques; **d** DC servo loop (DSL). (Color figure online)

compensation capacitor (Fig. 1b). RRL integrates ripple AC voltage at the output and converts it into current to compensate for DC offset, resulting in nullification of output ripple [52]. Furthermore, switched-capacitor notch filters or multiple-chopping schemes are also applied to reject residual ripples more efficiently [53, 54]. By properly using these IC circuit techniques, inherent circuit noise such as thermal and flicker noise can be significantly reduced.

To reduce the signal distortion due to high ESI mismatch of small dry-contact electrodes, the input impedance of analog-front-end (AFE) is boosted by using several impedance boosting techniques in IC chips. If the input impedance of sensor's AFE is high enough, EEG signal is measured without any voltage drop or attenuation even though ESI has time-varying features. Fig. 1c shows impedance bootstrapping which increases the impedance viewed from the input terminal by injecting current through a positive feedback loop to cancel the current from the input [55]. Unity-gain buffer and active shielding are also used to nullify the MOSFET parasitic capacitance and reject 50/60Hz power line interference (PLI) [56]. Moreover, chopper-stabilized amplifiers switch input coupling capacitors and pre-charge them through the auxiliary path before the chopping phase, which makes input capacitance decreasing [57, 58]. Impedance monitoring sensors based on artificial current injection are also utilized to check ESI change and compensate it for maximizing input impedance [59, 60].

To remove baseline wander due to electrode movement, DC servo loop (DSL) with the integrator in negative feedback loop have been used (Fig. 1d) [39]. It sets the DC voltage level as a stable reference point and removes extremely low-frequency components below cut-off frequency (e.g. 0.1Hz). Recently, on-chip pseudo-resistor or duty-cycled resistor of extremely high resistance are used for fine-tuning of very low cut-off frequency [61, 62]. However, because of the large time-constant of the integrator, DSL has an issue of DC settling time problem. Therefore, thanks to the development of a dynamic comparator and fast signal-tracking ADC, digitally-controlled DC servo loop (DCDSL) are used to stabilize the DC operating point when the output voltage is going out of a certain range [63, 64]. Nowadays, mixed-mode DSL composed of conventional DSL and DCDSL are co-utilized to prevent EEG signal from saturating.

2.3 Structures of EEG hardware

With the development of electrodes and IC technology described above, the entire structure of EEG recording hardware is also getting smaller, making it hard to be seen from the outside. As shown in Fig. 2, an active electrode (AE) made by locating small-form-factor IC chips directly on the electrodes can remove the long wire connection between a bench-top recording unit and electrodes. Two-wired active electrode structures which combine output terminal with a positive supply of operational amplifier into a single wire have been suggested [65, 66]. These active electrodes minimize the number of connecting wires and high impedance connections. To integrated EEG recording IC chips and electrodes, many kinds of flexible and wearable biomedical IC packaging technologies using planar fashionable circuit board (P-FCB) or flexible PCB (FPCB) are studied [67, 68]. These circuit boards allow the device to fit the head flexion so that it adheres well to the skin without additional bulky fixing structures. In addition, 3D packaging such as bottom-up packing and through-silicon via (TSV) with interposer are recently utilized, so that active electrode which have increased functionality density in even small size can be manufactured [69].

Furthermore, wireless communication technology like Bluetooth low energy (BLE) transfers EEG signal from the recording unit to the outside processor without additional wire connections [70, 71]. Therefore, it becomes possible to transmit accurate EEG signal by using miniaturized less-wire equipment without the effects of the artifacts. The shape of the device has also gradually been developed in a form of a headband or a patch which can be used while walking or exercising [72, 73]. Compact flexible joint and bearing structures based on anatomic and ergonomic design are inserted to make robust skin contact [74].

One of the great examples of a miniaturized EEG recording system is ear-EEG technology. Two types of ear-EEG recording methods have actively been studied: (1) in-ear EEG which records EEG within the ear canal using an earpiece-shaped electrodes [75–77]; and (2) cEEGrid which records EEG in the area behind and around the ear using an ear hook-shaped electrodes [78]. Particularly, small size in-ear EEG device has several attractive advantages compared to bulky conventional on-scalp EEG device. Small and lightweight earpiece makes the recording module compact and unobtrusive, leading to wearable easy-to-use in everyday life [79]. In addition, because electrodes contact tightly and firmly with ear skin due to pressure between earpiece and ear canal, some kinds of artifacts such as eye blinking can be reduced [80]. In the near future, EEG recording modules are expected to be integrated with noise cancellation techniques or sound production speakers, which makes it possible to organize an all-in-one healthcare in-ear EEG device collaborated with a wireless earphone or a hearing aids product [81, 82].

Many kinds of researches for precise in-ear EEG recording in a comfortable manner have been performed. In terms of electrode development, several user-generic earpieces are manufactured by using various materials such as carbon-nano-tube/polydimethylsiloxane (CNT/PDMS) [83], viscoelastic memory foam with Ag-coated cloth [84], and silvered glass silicone [85]. All those

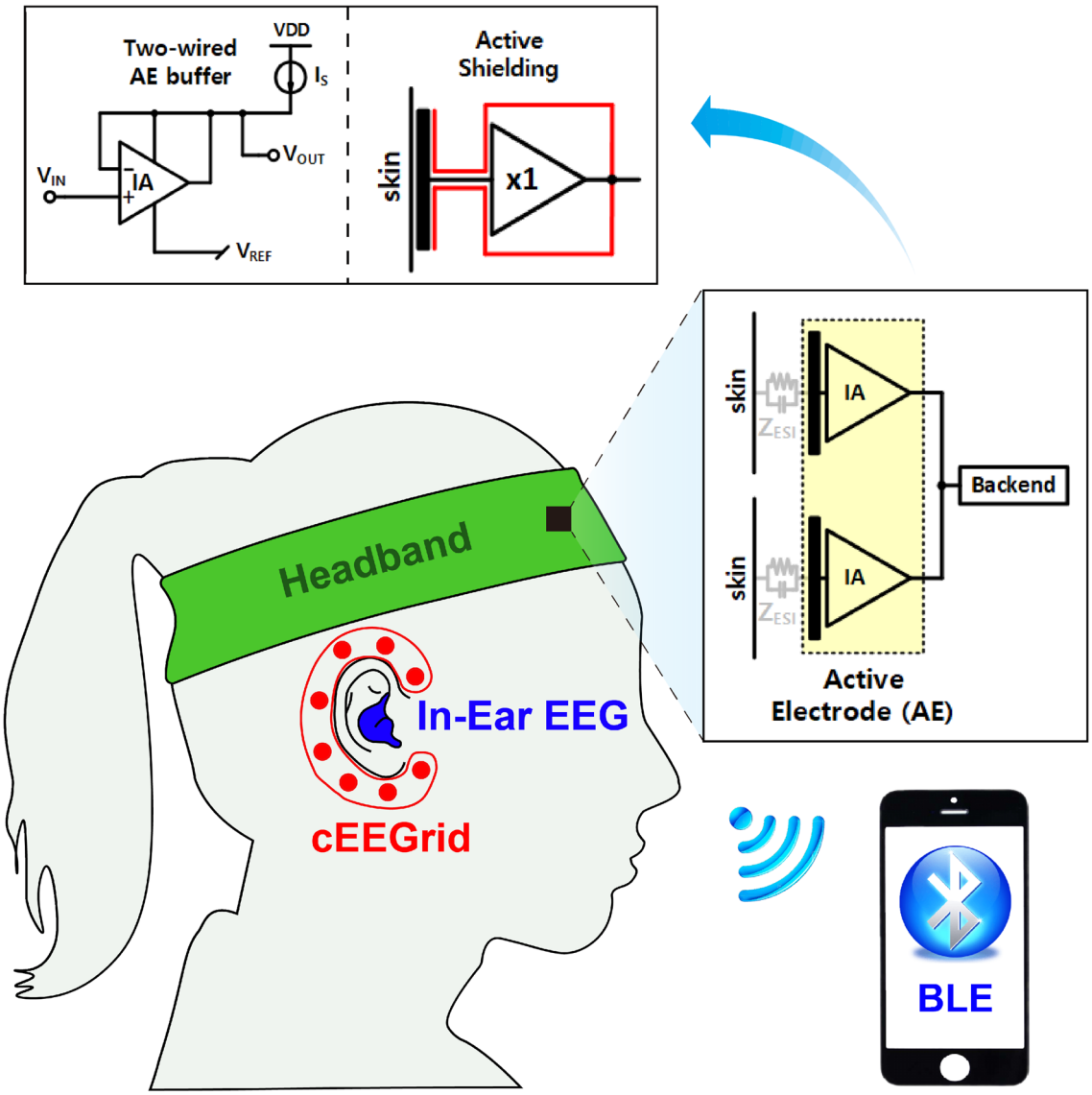

Fig. 2 Miniaturized EEG devices using active electrodes (AE) are shown. Two representative active electrode structures such as two-wired AE buffer and active shielding have widely been used. With the AE techniques, small-form-factor and daily life EEG devices are able to record EEG on the forehead (headband), around the ear (cEEGrid), and in the ear canal (in-ear EEG)

materials have high flexibility, adequate viscoelasticity and biocompatibility, and moderate pressure between earpiece and ear canal. These characteristics make compact devices to be fixed in place softly and firmly. In terms of electrical circuit development, bio-signal readout circuits have been increasingly implemented in developing miniaturized and power-efficient in-ear EEG recording systems [86, 87]. The readout modules utilize a CCIA to reduce the noise level and combine other IC schemes to record exact in-ear EEG signal.

3 Miniaturization techniques for EEG processing

3.1 EEG channel selection

Although the EEG has been recorded with a miniaturized EEG device, extracting meaningful information from multi-channel data is an ongoing challenge. If the crucial channels can be discriminated, the computational

complexity of the following EEG analysis will be significantly reduced. Furthermore, EEG devices can operate with smaller batteries by finding crucial channels only, and small-form-factor devices with minimum wire configuration can be re-manufactured. In that sense, many kinds of research are ongoing to reduce the number of electrodes for certain EEG applications. For example, in [88, 89], motor imagery classification and sleep monitoring were done only using 6 electrodes. In [90], emotion-based EEG classification has been conducted with 13 electrodes.

Channel selection (CS) refers to a series of processes that enables data processing and classification of EEG signals even with a small number of channels by selecting a few crucial channels for analysis. By including the CS process in or before EEG processing algorithms, we can find the critical channels for discriminating EEG patterns and utilize this result to simplify the EEG systems. There are two main approaches of CS: filtering method and wrapper method.

Filtering method is a technique that reduces the number of channels through a specific criterion or channel search algorithm before classification (Fig. 3 Top). Therefore, how well the channel is selected is only determined by the particular criterion or selection algorithm itself. Using variance is one of the strategies for channel selection [91]. The variance of EEG data from each channel is calculated, and only the top three channels with the largest variance are used for subsequent seizure classification. Besides variance, statistical criteria such as entropy are often used for CS [92]. In addition, common spatial patterns (CSP), a widely used algorithm in motor imagery classification [93], is categorized into filtering methods. The CSP algorithm filters the EEG signal by creating a spatial filter that maximizes the variance of one group of data while minimizing the variance of the other data. During this process, the coefficient of each spatial filter is calculated. Finally, only a few filters with a large coefficient are used to reduce the number of channels. Modulations of the CSP such as CSP-rank [94] and L1 norm regulation CSP [95] are also used. After the channel reduction, a subsequent classification algorithm such as support vector machine (SVM), linear discriminate analysis (LDA) is trained.

Wrapper method is a technique that a particular algorithm determines the channel subset and outputs classification results simultaneously. Unlike the filtering method, channel selection is wrapped around by the feedback of classification results. As shown in Fig. 3 (Bottom), both channel selection and classification are trained through a specific algorithm together. The classification algorithm classifies EEG data using only the specific channel subset and outputs classification results. Based on these classification results, the channel subset is updated until there is no accuracy improvement. Machine learning algorithms such as SVM and LDA are used for wrapper methods. SVM was repeatedly applied to several channel subsets and finally reduced 18 channels to 4.6 channels while maintaining 97% seizure detection accuracy [96, 97]. In the case of [98, 99], selecting channels and calculating classification errors were evaluated by LDA training. Besides SVM and LDA, other machine learning algorithms are used for channel selection in a wrapper method [100, 101].

The main difference between filtering and wrapper methods is whether channel selection is trained together with the

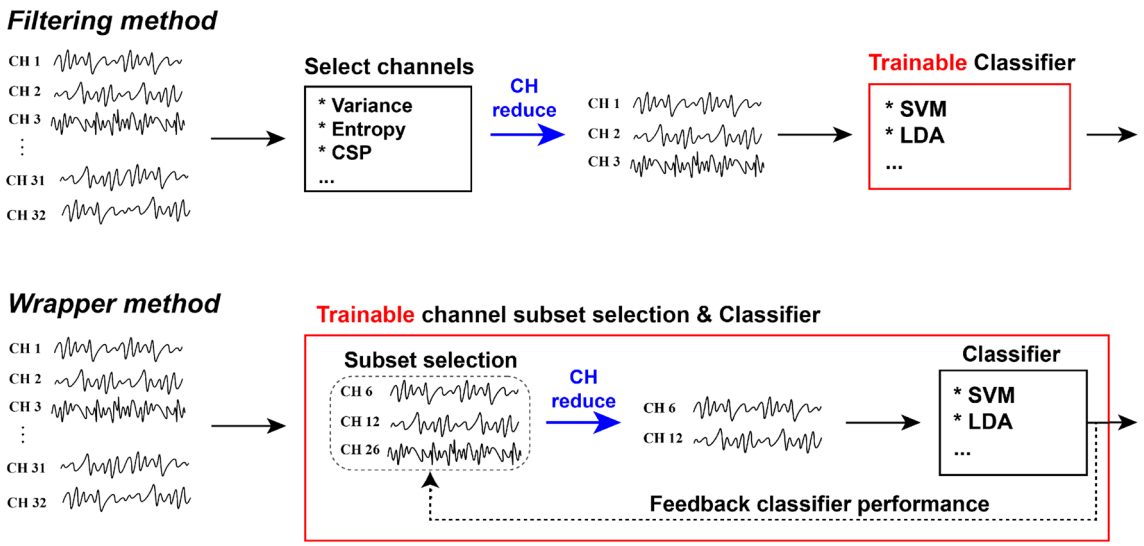

Fig. 3 Two main categories of channel selection. (Top) Filtering method reduces channels according to specific criteria beforehand. The following classifier only uses the reduced data for training. (Bottom) Wrapper method trains the classifier to do both channel selection and classification of EEG. The main difference is whether channel selection is included in classifier training

classification algorithm. As shown in Fig. 3, channel selection of filtering methods is independently performed regardless of the classifier. Thus, filtering method shows faster calculation compared to wrapper method. However, it achieves sub-optimal performance because the channel selection is conducted regardless of classifier output accuracy. On the other hand, wrapper method finds the optimal channel subset through feedback at the expense of expensive computation and over-fitting. By considering the pros and cons of the filtering and wrapper method, applying the appropriate CS technique to raw EEG data can relieve the computational burden, leading to miniaturized EEG systems.

3.2 Hardware implementation of EEG processing

Conventional EEG analysis was conducted by transmitting the EEG signal to the computer, where the processing and classification are performed (Fig. 4 Left). In the case of wired data transmission, the wire itself hinders the mobility of EEG devices. Also, for the case of wireless data transmission, the device needs large batteries, which disturb miniaturization. Referring to [102], 73% of power dissipation in bio-sensor is due to wireless data transmission. Therefore, hardware implementation of EEG classification is in the spotlight to achieve miniaturization and high mobility by minimizing the stage of raw EEG signal transmission (Fig. 4 Right). In particular, field-programmable gate array (FPGA) is drawing attention as a hardware implementation platform. FPGA is more energy-efficient than other processors such as central processing unit (CPU) because of its low-power parallel processing. Also, utilizing short development time and re-programmability, FPGA is a promising platform for EEG processing. Although the device still needs occasional wireless data link to update its parameters such as in initialization stage, it does not need a constant data transmission due to its own processing capability. This stand-alone ability dramatically reduces the overall power consumption.

The paper [103] implemented a motor imagery classifier using a CSP algorithm on various FPGAs and compared the performance of those systems. The EEG classifier implemented on FPGA was 7.5 to 16 times faster than the classifier implemented on CPU and was an order of magnitude more power-efficient. The paper [104] implemented a short-time Fourier transform (STFT) and SVM-based classifier for EEG seizure detection on FPGA. Compared with the conventional method, the hardware classifier shows 1.7x speed up and improved detection sensitivity. The machine learning algorithms with relatively low complexity such as SVM and LDA can be implemented with lower design cost on FPGA. However, the performance and stability of a simple machine learning classifier are usually affected by the data when building the model. Thus, many studies also pay attention to hardware implementation of deep learning, which shows general performance in various applications. The paper [105] implemented a convolutional neural network (CNN) on FPGA and used it for EEG-based emotion detection studies.

There are some common considerations to implementing algorithms on FPGA, such as model compression and hardware optimization for algorithm calculation. First, model compression should be considered to fit the algorithm model on FPGA, which has more limited resources than computers. Quantization of data is one possible strategy of model compression that can reduce the storage requirement of the hardware system. Many research articles implement EEG classifiers on FPGA by using the fixed-point format [106, 107]. Fixed point format is a method of representing fractional numbers with a fixed number of digits in hardware

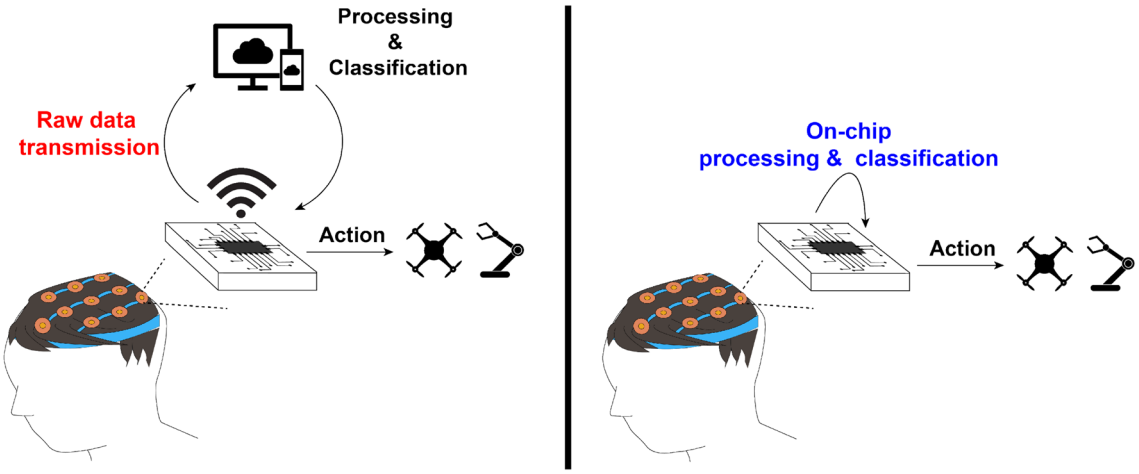

Fig. 4 (Left) A conventional system for EEG processing. Raw data transmission is inevitable because of processing algorithms running on computers. (Right) System for hardware-implemented EEG processing. On-chip processing enables fast and low-power operations on EEG devices

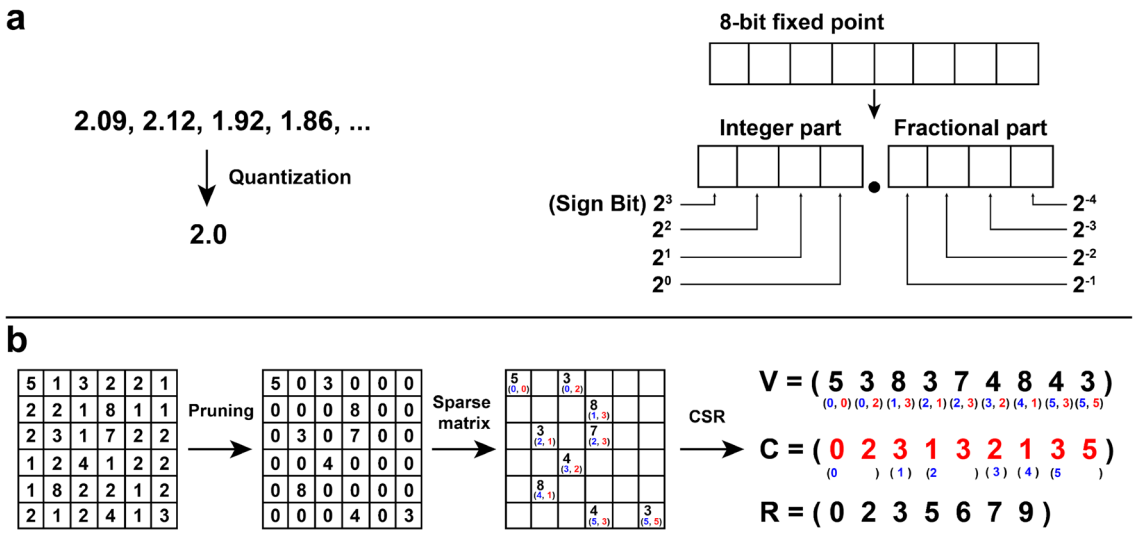

Fig. 5 **a** Simple illustration of quantization and fixed-point format. **b** Flow for model compression of a data matrix. The values smaller than the threshold value (in this case, 3) are pruned to zero. After pruning, a matrix is transformed into a sparse matrix. Using special format such as CSR, sparse matrix is even compressed

(Fig. 5 a). Using this format, data previously defined as a long bit-width floating-point format can be represented with a low-bit fixed point.

Furthermore, another model compression method is reducing the amount of calculation by setting operands zero. The pruning method as one possible scheme zeros the numbers which are smaller than a specific threshold value and makes the following multiplication to simple zero (Fig. 5 b). Pruning was used as model compression in an EEG intend recognition system [108, 109]. Even with applying the pruning algorithm to data, no significant degradation in performance was observed. After the pruning, data can be represented in a sparse matrix form. Besides pruning, other techniques such as single value decomposition can be utilized to transform the data matrix to a sparse matrix during hardware implementation [110]. Moreover, storage requirements can be lowered by storing a sparse matrix in a unique format. One of the methods to store sparse matrix is compressed sparse row (CSR). The CSR method represents a spares matrix by three arrays containing non-zero values, column indices, and the extent of rows. With this method, the storage requirement of data can be even compressed, which alleviates the memory bottleneck of hardware [111].

Finally, hardware-optimization for algorithm calculation can be considered to fully exploit the limited resource. One of the methods is to optimize repeated calculations such as matrix-vector multiplication. Utilizing parallel computing and pipe-lining characteristics of hardware, matrix-vector multiplications are performed much faster with high energy-efficiency compared to the calculation on computers [112]. Another possible method is to refine data flow. As the resource of FPGA is limited, data fetching and data controlling should be carefully conducted. To optimize memory-related data flow, the tiling of for-looped operations is focused [113, 114]. These approaches enable real-time BCI systems and EEG device miniaturization through processing acceleration and small battery usage.

4 Conclusion

This article reviews miniaturization techniques for EEG measurement and classification simultaneously. From the perspective of developing compact EEG recording hardware, various technologies are applicable to the acquisition system. Small-size electrodes and nano-meter scale IC technology are studied to measure EEG within a small area. Moreover, miniaturized devices such as in-ear EEG get high research interest to measure EEG easily and comfortably. Along with the hardware miniaturization, channel selection techniques and hardware implementation of EEG classification were studied for the compact EEG processing.

As this paper reviewed, miniaturization is essential for developing wearable healthcare EEG systems. However, as front-end hardware gets much smaller, the number of channels decreases. High-performance signal classification techniques are inevitably required to monitor meaningful human brain information with even fewer channels. Therefore, the limitation of hardware miniaturization at the front-end is determined by signal processing performance at the back-end. In addition, to ease the burden of the classification processes, it is necessary to extract a high SNR EEG signal

by utilizing well-manufactured compact electrodes and IC chips. Eventually, this intertwined relationship makes co-research of EEG recording and processing indispensable.

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Declarations

Conflict of interest Kim M declares that he has no conflict of interest in relation to the work in this article. Yoo S declares that he has no confict of interest in relation to the work in this article. Kim C declares that he has no conflict of interest in relation to the work in this article.

Ethical approval This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to participate This article does not contain any studies with human participants or animals performed by any of the authors.

Consent to publish This article does not contain any studies with human participants or animals performed by any of the authors.

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