



Article

Oxide-Oxide Thermocompression Direct Bonding Technologies with Capillary Self-Assembly for Multichip-to-Wafer Heterogeneous 3D System Integration

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Abstract: Plasma- and water-assisted oxide-oxide thermocompression direct bonding for a self-assembly based multichip-to-wafer (MCtW) 3D integration approach was demonstrated. The bonding yields and bonding strengths of the self-assembled chips obtained by the MCtW direct bonding technology were evaluated. In this study, chemical mechanical polish (CMP)-treated oxide formed by plasma-enhanced chemical vapor deposition (PE-CVD) as a MCtW bonding interface was mainly employed, and in addition, wafer-to-wafer thermocompression direct bonding was also used for comparison. N₂ or Ar plasmas were utilized for the surface activation. After plasma activation and the subsequent supplying of water as a self-assembly mediate, the chips with the PE-CVD oxide layer were driven by the liquid surface tension and precisely aligned on the host wafers, and subsequently, they were tightly bonded to the wafers through the MCtW oxide-oxide direct bonding technology. Finally, a mechanism of oxide-oxide direct bonding to support the previous models was discussed using an atmospheric pressure ionization mass spectrometer (APIMS).

Keywords: multichip-to-wafer; direct bonding; capillary self-assembly; liquid surface tension; 3D integration; CMP; heterogeneous integration

1. Introduction

Although interconnect pitches in microelectronic packaging have scaled by a factor of three to four since the 1970s in industry, Si has approximately scaled by 1000-fold during the same time frame [1]. Therefore, the demand on interconnect scaling will be further enhanced in flip-chip assembly. 3D integration with metal microbumps can address the issue of packaging density, and in addition, parallel signal processing with through-Si vias (TSVs) can realize high-speed and

low-power heterogeneous system integration with microelectromechanical systems (MEMS) photonics, passives, and complementary metal-oxide semiconductor (CMOS) toward upcoming internet of things (IoT) societies [2–6]. In recent years, the pitches of solder microbumps with Cu pillars have been significantly decreased down to 10 μm or less [7–9]. Good cross-sectional scanning electron microscope (SEM) images showing bonded microbumps have been seen from the previous papers, however, perfect interconnection with millions of microbumps or beyond is still challenging due to poor height uniformity of electroplated solder/Cu microbumps and contamination issues for wafer-level integration. More recently, we have reported a high-yield and high-density Cu-Cu interconnect technology with a sheet of Cu nanopillar based on a MCtW 3D stacking we call reconfigured wafer-to-wafer 3D integration [10].

As is also mentioned in the paper, a known good dies (KGDs) array can be simultaneously and precisely self-assembled on a host wafer by liquid surface tension as a driving force [7,11–13]. This methodology can solve a potential tradeoff issue between assembly throughput and assembly accuracies in one-by-one pick-and-place assembly used in conventional chip-to-chip, chip-to-wafer, and chip-to-substrate approaches. Thus, the MCtW integration with the use of KGDs would be expected for advanced packaging including multi-layer chip stacking [14].

Another serious issue is underfilling into small gaps between three-dimensionally stacked chips with fine-pitch microbumps. Pre-underfill materials such as non-conductive paste (NCP) and non-conductive film (NCF) have been developed to solve the issue. However, the NCP technology involves sequential low-throughput dispensing processes, whereas the NCF technology called wafer-level underfilling still requires pick-and-place assembly after dicing of NCF-laminated wafers. We have presented a fully wafer-level underfill technology using a new NCF technology combined with MCtW capillary self-assembly [15,16]. The NCF technology can reduce the pitches of solder/Cu microbump down to 30 μm or less.

Hybrid bonding has also been actively studied to further reduce interconnect pitches. Simultaneous bonding of metals/metals and dielectrics/dielectrics is essential for the technologies. Fine-pitch interconnections using the hybrid bonding technologies have been introduced by several researchers [17–21]. These hybrid bonding methods using plasma surface treatments are processed at temperatures in the range of 200–350 $^{\circ}\text{C}$ in wafer-level processing. Since hybrid bonding technologies are challenged by the momentous tasks of Cu-CMP processes to obtain extremely small surface roughness and total thickness variation (TTV) with low cost and high process controllability, new metal/metal bonding technologies insensitive to the surface topography and uniformity are recommended as described above [10].

On the other hand, oxide-oxide direct bonding is a promising candidate for ultra fine-pitch interconnect formation without metal/metal bonding including microbumps [22,23]. Using the direct bonding technologies, wafers or KGDs can be tightly bonded to the corresponding target wafers without adhesives or underfill resins. The technologies have been traditionally used to fabricate silicon on insulator (SOI) wafers [24]. In addition, no sophisticated CMP processes with heterogeneous materials of metals and dielectrics are required. Ultra fine-pitch TSVs with the pitches of 3 μm [25] can be formed through directly bonded wafers/KGDs with traditional high-resolution photolithography processes, and thereby, upper and lower wafers/KGDs can be electrically connected after direct bonding. In this paper, we employ oxide-oxide direct bonding for self-assembly based MCtW 3D integration, especially for via-last/backside-via 3D stacking. The direct bonding technologies need to be processed at relatively low temperatures with plasma surface activation so as not to apply thermal stress to the devices and wirings of wafers or KGDs [26]. We have previously studied a unique room-temperature pressure-free oxide-oxide direct bonding process combined with surface tension-driven self-assembly using water droplets including a small quantity of hydrogen fluoride [27].

Multichip-to-wafer 3D integration approaches using self-assembly and oxide-oxide direct bonding are classified into two categories: “non-transfer stacking” without support wafers and “transfer stacking” with support wafers which we call Self-Assembly and Electrostatic (SAE) carrier wafers [28].

Since no support wafers are required for the non-transfer stacking based 3D integration, this approach seems to be cost effective and high throughput, but this is not necessarily advisable. Target bottom wafers and lower KGDs receive repeated thermomechanical stresses and damages through the 3D integration processes with thinning and TSV formation, as the number of stacked layers increases. This means that transfer-stacking based 3D integration would be useful for multi-layer 3D chip stacking to increase total production yields. In this paper, however, we focus on 3D stacking of the first layer KGDs on target wafers using oxide-oxide thermocompression direct bonding [29]. Therefore, non-transfer stacking based 3D integration using MCtW self-assembly is adopted.

Figure 1 schematically shows the total process flow of the non-transfer based heterogeneous 3D integration approach using MCtW oxide-oxide direct bonding with self-assembly. The sequence is also applicable to 3D stacking of KGDs with TSVs fabricated in via-middle processes. First, KGDs with a CMP-treated plasma-CVD SiO₂ layer on their top are self-assembled in a face-down configuration to a host target wafer on which hydrophilic assembly areas and the hydrophobic background region are formed. Prior to the self-assembly process, plasma activation is performed on the surface of the wafers and/or KGDs. After liquid evaporation, the KGDs are thermally compressed on the wafer, followed by multichip thinning. Then, ultra fine-pitch TSVs are formed on the KGDs. When multi-layer chip stacking is required, the repetition of these process can produce 3D chips with high-density TSVs. When MEMS chips with brittle movement elements and thermally unstable devices are integrated in heterogeneous microelectronic 3D system, it would be suitable for stacking on the top or directly mounted on the Si interposers due to the process compatibility.

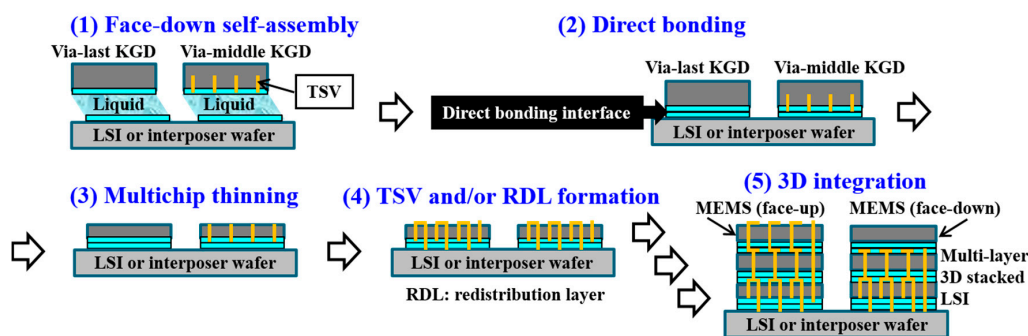


Figure 1. Typical non-transfer stacking based heterogeneous 3D system integration using MCtW self-assembly and thermocompression direct bonding.

2. Results and Discussion

2.1. Evaluation of Interfacial Energies of Directly Bonded Wafers

Prior to MCtW direct bonding, wafer-to-wafer direct bonding processes are employed to measure oxide-oxide bonding energies of CMP-treated and plasma-activated SiO₂ used in our experiments. Although a cleavage method with blade insertion is applicable to quantitatively evaluate bonding interface between wafers with beveled edges, typical chips have no bevel parts around their edges, and thus, their bonding interface energies cannot be determined by the method. First of all, the dependences of the bonding energies of directly bonded wafers on oxide types (thermal oxide or PE-CVD oxide) and gaseous activated species (Ar or N₂) are investigated for comparison to previous works [30–34].

In the experiment, 0.28-mm thick Si wafers with 0.3- μ m-thick thermally oxidized (high-purity steam is generated by burning H₂ and O₂ gases at 1000 °C) or 1.5- μ m-thick PE-CVD deposited SiO₂ layers were used for direct bonding. The PE-CVD SiO₂ layers were planarized by SiO₂-CMP with a ceria-based slurry, resulting in the R_a roughness of 0.2 nm. The as-deposited thermally oxidized wafers and the CMP-treated wafers with PE-CVD SiO₂ were cleaned with deionized water in a megasonic

bath. In the subsequent plasma irradiation process, the surfaces of the wafers were activated with N₂ or Ar plasma with a widely used sputtering system (CFS-4ES, Shibaura Mechatronics Corporation), followed by dipping in deionized water for 10 min and spin-drying.

In the next bonding process, these wafers were thermally compressed at 300 °C in a vacuum atmosphere of 5 Pa, using a wafer bonder (EV520, EVG). Here, direct bonding experiments were performed under seven different conditions. The top wafers were directly bonded to the bottom wafers with the same oxide types (thermal or PE-CVD oxide). The SiO₂ surfaces of the top and/or bottom wafers were activated by plasma irradiation using Ar or N₂ gas.

The bonding strengths of wafer-to-wafer direct SiO₂ bonding were determined by the fracture toughness (bonding energy) *G*. These bonding energies using the double cantilever beam (DCB) technique were calculated by a crack length that appeared when a blade was inserted into a bonded wafer on the basis of a crack propagation theory as follows [35,36]:

$$G = 3Et^3y^2/4L^4,$$

where *2y*, *L*, and *t* are the blade thickness, the crack length from the wafer edge to a bonding/debonding border, and the wafer thickness, respectively. *E* is the Young’s modulus. In this study, the wafer thickness *t* is 0.28 mm, the blade thickness *2y* is 0.15 mm, and the Young’s modulus of Si<110> is 166 GPa [35]. The crack length *L* was measured by the distance between the first fringe from the crack tip and the actual blade edge using a ruler and IR camera (Infrared Transmission Analysis Inspection System IRise, Moritex Corporation) as shown in Figure 2a. Indeed, when the fringes are observed with the IR light passing through Si, the wafers are separated by a quarter of the observation wavelength (*λ*/4): the value is typically 250 nm or above (*λ* is 1 μm at least). We do not take into account the small distance between the first fringe position and the real crack tip position. The measurements were performed within 5 min at 60% relative humidity or more immediately after the blade insertion with a blade speed of more than 600 mm/min. The blade velocity was not precisely controlled. The surface energy *γ* meaning intrinsic surface energy of one crack surface is generally expressed by dividing the fracture toughness (bonding energy) *G* of bonded wafers by two [37]. Regarding the above-mentioned equation, the errors about 20% or more have to be taken into account, considering a wafer thickness variation around ±20 μm, a crack length accuracy around ±5%, and a blade thickness precision.

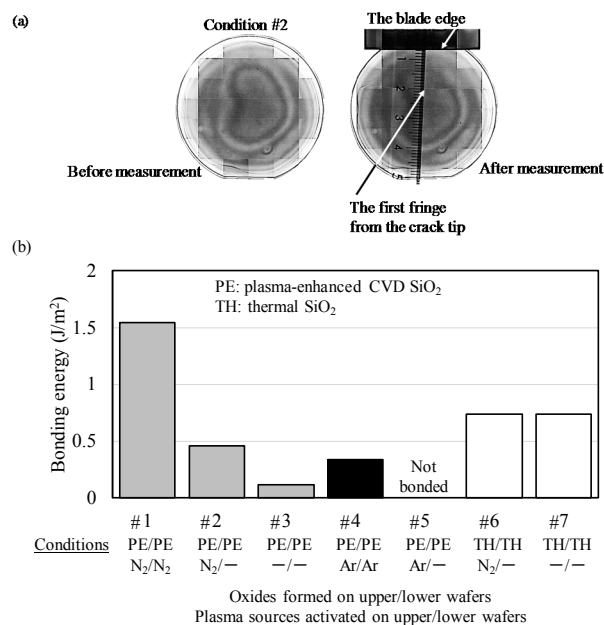


Figure 2. An example of IR images of PE-CVD oxide-oxide bonding (#2) before and after blade insertion test (a) and bonding interfacial energies of directly bonded wafers (#1–#7) (b).

Figure 2b shows the interfacial bonding energies of bonded wafers prepared by wafer-to-wafer oxide-oxide direct bonding under the various seven conditions. As seen from this figure, the bonding energies of the bonded wafers activated with N₂ plasma under the conditions #1 and #2 were significantly higher than those of the ones activated with Ar plasma under the conditions #4 and #5. These results indicate that N₂ plasma is a more effective surface activation species than Ar plasma to obtain high bonding quality. Figure 3 shows atomic force microscopy (AFM) profiles before and after plasma irradiation on the surface of CMP-treated PE-CVD oxide. As seen from this figure, Ar plasma induces large surface roughness of 0.81 nm on the CMP-treated oxide due to the ion bombardment effect of Ar atoms that are heavier than N₂. The N₂ plasma keeps the extremely smooth SiO₂ surface with a roughness R_a of around 0.44 nm after plasma irradiation. The bonding energy obtained from the condition #1 (CMP-treated PE-CVD oxide activated with N₂ plasma both on upper and lower wafers) is good consistent with that reported in the previous work [33]. In contrast, CMP-treated PE-CVD oxide without plasma activation (the condition #3) shows much lower bonding energy of the previous one [33]. There are no detailed CMP/cleaning conditions and activation power/time in the previous work, but the low bonding energy is due to the total thickness variation of the CMP-treated wafers and the locally high points shown in Figure 3a coming from residual particles such as slurries used in our SiO₂-CMP process although plasma activation with N₂ tends to reduce the asperity summits shown in Figure 3b. In other word, the PE-CVD-treated oxide-oxide bonding without plasma activation in this work has high potential to give further high bonding energies by optimizing the CMP/cleaning conditions. In this work, wafer-to-wafer bonding was performed by thermal compression because of the large wafer bow caused by the mechanical stress of the PE-CVD oxide. The measured wafer warpage profile was not shown here, but the value was 25 μm over the 2-inch Si wafer with an as-deposited 1- μm -thick PE-CVD oxide deposited at 350 °C, which would be attributed to the low bonding energies.

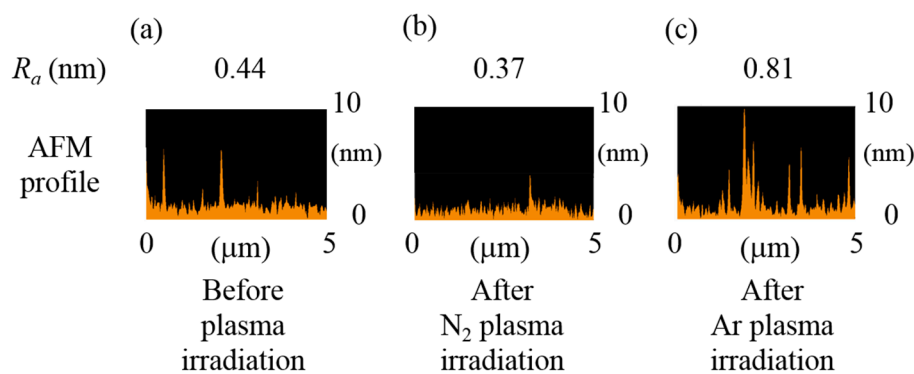


Figure 3. AFM profiles and surface roughness before (a) and after plasma irradiation (b,c) on the surface of CMP-treated PE-CVD oxide.

On the other hand, the wafers bonded through the thermal oxide layers under the conditions #6 and #7 show quite larger bonding energies than those through the PE-CVD oxide layers under the conditions #2 and #3. The bonding energy of #7 (non-activated thermal oxide bonding) is slightly higher than that in previous direct bonding works [31,33]. However, the bonding energy of #6, thermal oxide bonding activated on one wafer, seems to be approximately half of that reported in the previous work [31]. There is the possibility that the low bonding energies obtained from plasma-activated thermally oxidized wafers bonding in this work are due to the N₂ conditions such as plasma power, activation time, and/or organic contamination from the sputtering equipment used in this plasma activation process. Since the quick blade insertion in this work has been carried out at high humidity atmosphere although the bonding energy measurement has been done within 5 min directly after the blade stop, the resulting bonding energies could show lower values due to external water stress

corrosion during the DCB measurement [34], especially for low-power deposited PE-CVD oxides sensitive to moisture [38].

2.2. Evaluation of Bonding Strengths of Directly Bonded Chips

MCtW direct bonding is demonstrated and the shear bonding strengths of the chips assembled on wafers are measured using thermal SiO₂ or CMP-treated PE-CVD deposited SiO₂ with N₂ plasma activation and the subsequent water dipping processes. In the experiments, 0.28-mm thick wafers and chips with a size of 5 mm × 5 mm were used. The wafers were treated with N₂ plasma, and subsequently dipped into deionized water and spin-dried. In contrast, the non-activated chips were cleaned with a H₂SO₄/H₂O₂/H₂O solution to remove organic contaminants prior to assembly. The wafers were set on the lower stage of a wafer bonder EV 520, and the chips were assembled on the wafers in a face-down configuration. After that, a compliant soft graphite sheet and an additional carbon plate were placed on the top of the chip array. Because the graphite sheet is a deformable material, the sheet acts as a TTV absorber to provide uniform compressions for all the KGD chips on the corresponding wafers. In addition, the graphite sheet has high thermal conductivity, and thereby, the heating temperature can be well controlled during the MCtW bonding process. In the direct bonding, the chips were thermally compressed to the corresponding wafers through the graphite sheet at 300 °C in a vacuum atmosphere of 5 Pa with a bonding pressure of 0.8 N/chip or 10 N/chip. After the direct bonding process, the shear bonding strengths between the chips and the wafers were measured with a bond tester.

Table 1 shows the bonding yields of the chips simultaneously and directly bonded to N₂ plasma-assisted wafers under the three conditions. The bonding yield is determined by the ratio of the number of tightly bonded chips that withstand 5-kg shear load to total number of measured 12 chips. The chips with share bonding strengths of below approximately 2 MPa are defined as non-bonded chips. As seen from the table, the bonding yield in the low bonding pressure of 0.8 N/chip was much lower than that of the high bonding pressure of 10 N/chip. The MCtW direct bonding between thermal oxide layers shows a good yield, exceeding 90% when the bonding pressure of 10 N/chip was used. The reason why the yield has not reached 100% is probably due to particles resulted from the experimental environment and/or the chipping defects of chip edges. In contrast, the yields are approximately 30% when the pressure of 0.8 N/chip was used for MCtW direct bonding with thermal oxides. Therefore, high bonding pressure above 10 N/chip seems to be appropriate to stably obtain the thermocompression direct bonding yields beyond 90%. The low bonding pressure of 0.8 N/chip would provide the chip array and the wafers with non-uniform thermal compression, because this pressure might not be sufficient to completely deform the graphite sheet.

Table 1. Effect of oxide types and bonding load on bonding yields of chips directly bonded to wafers with N₂ plasma activation on chips.

Bonding Conditions	TH/TH	TH/TH	PE/PE
	N ₂ /— 0.8 N/chip	N ₂ /— 10 N/chip	N ₂ /— 10 N/chip
Bonding Yield (%)	33	92	92

Figure 4 shows the shear bonding strengths between the chips and the wafers of the three conditions described above. As shown in this figure, the low bonding pressure of 0.8 N/chips resulted in a relatively high bonding strength of 15 MPa although the bonding yield was low. On the other hand, the average shear bonding strengths with the high bonding pressure of 10 N/chip were 18.3 MPa and 14.0 MPa for thermal oxide and CMP-treated PE-CVD oxide, respectively, as shown in this figure. These results show that the shear bonding strengths between the chips/wafers with the PE-CVD oxide layer were comparable to those with the thermal oxide layer. This tendency is similar to that observed in the wafer-to-wafer direct bonding experiment described in the previous

section of #2 and #6 in Figure 2b. These resulting bonding strength of PE-CVD oxide-oxide bonding in Figure 4 is high enough to endure the back side grinding and CMP processes during multichip thinning. These results give a positive prospect for the application of the MCtW oxide-oxide direct bonding technologies for 3D integration. In addition, these advanced direct bonding technologies can be expected to further progresses in via-last/backside-via TSV formation, because the thermally stable bonding interface is required to the repeated 3D stacking processes.

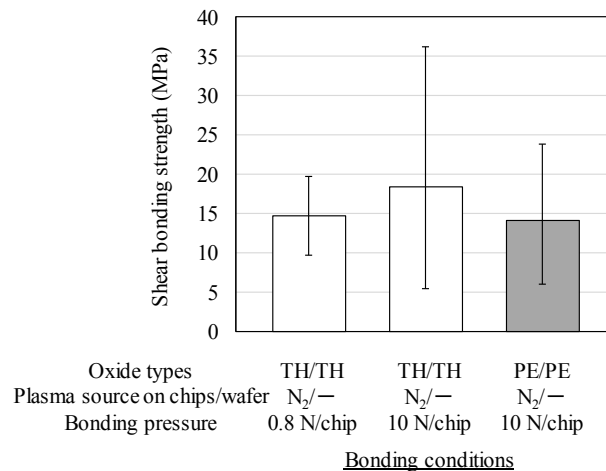


Figure 4. Shear bonding strengths of chips directly bonded to wafers with N₂ plasma activation.

The effect of both the N₂ plasma activations and water dipping processes on the shear bonding strengths is evaluated. Three types of surface treatments were employed: the first condition was plasma activation without water dipping water. The second condition was water dipping without plasma activation and the third one was plasma activation and the subsequent water dipping. The plasma activation with N₂ gas was performed with a widely-used sputtering system (SH-550, ULVAC). After the MCtW direct bonding processes, the shear bonding strengths of the directly bonded chips were measured with the bond tester.

Next, in order to evaluate the in-plane uniformity of the bonding strengths of a chip directly bonded to the corresponding wafers under these conditions, dicing tests were performed. In the dicing tests, the 5-mm-square chips directly bonded on the wafers were further singulated into 1-mm-square dies with a saw dicer, and the number of the remaining dies against the dicing stress were counted for evaluating bonding uniformity. Here, we used 3 chips for each direct bonding condition, so totally 75 pieces of 1-mm-square dies are obtained. Figure 5a shows an IR image and a photomicrograph of a directly bonded chip before and after cutting into the 1-mm² dies, respectively. Unbounded areas or entrapped particles can be easily observed by the IR images, but the bonding strengths of the bonded areas are not figured out. In this figure, the percentage of the 1-mm² dies that are remained bonded after the dicing process represents the bonding uniformity of the chips directly bonded through the CMP-treated PE-CVD oxide under the three surface treatment conditions. The bonding uniformity obtained by the dicing method is not necessarily quantitative. However, this method was employed to compare among various conditions of surface treatments for oxide-oxide direct bonding [39]. As shown in the figure, the bonding uniformity decreases with the used surface treatment in the following order: plasma activation with water dipping, water dipping without plasma activation, and plasma activation without water dipping. These results suggest that N₂ plasma irradiation not only helps to strengthen the MCtW direct bonding with PE-CVD oxide, but also increases the bonding yields evaluated by dicing.

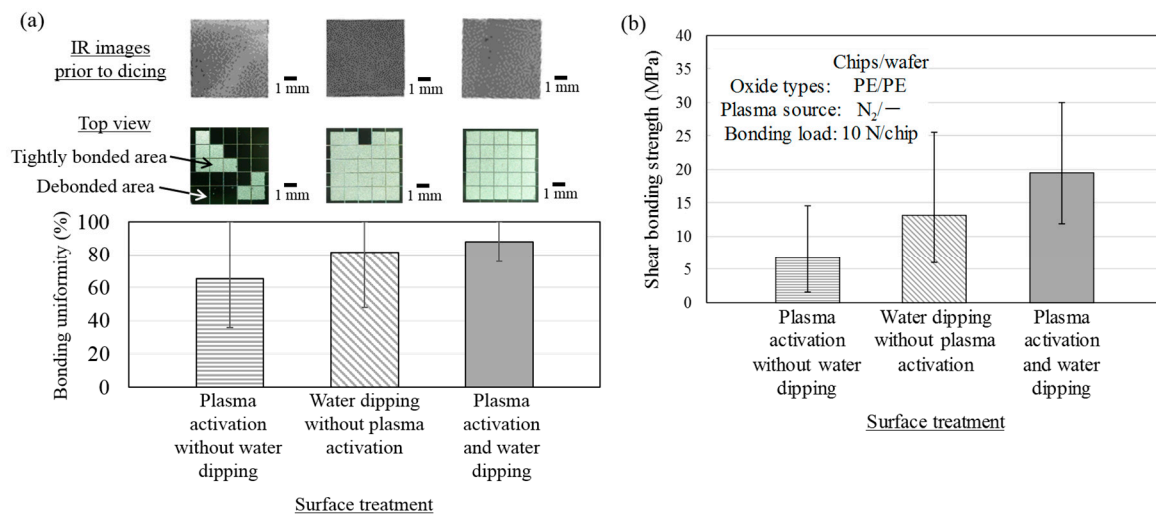


Figure 5. Bonding uniformity of chips directly bonded to wafers conditioned with different surface treatments (a). The IR images of chips are taken after MCtW direct bonding prior to dicing and the top views show a whole chip after dicing. The error bars indicate the max. and min. ratio of “the number of non-debonded 1-mm-square small dielets per a 5-mm-square chip” to “25 (the total number of the small dielets after dicing per the chip)”. Shear bonding strengths of chips directly bonded to wafers conditioned with different surface treatments (b).

Figure 5b shows the shear bonding strengths of the directly bonded chips using the three types of surface treatments. The strongest average shear bonding strength was 19.5 MPa, and was obtained with both the surface treatment of plasma activation and water dipping. The surface treatments with plasma activation exhibited average direct bonding strengths of 6.8 MPa, whereas the water dipping treatment exhibited 13.1 MPa. These results indicate that the wafer surface pre-treatment by water dipping makes a strong contribution to the achievement of the high bonding strengths for the MCtW direct bonding processes, compared to N₂ plasma irradiation. As seen from Figure 5a,b, water absorption on the surface and/or subsurface [31] of the host wafers would act as a dominant factor to obtain both high bonding strengths and high bonding uniformity on the entire surface of the chips.

2.3. Self-Assembly of Chips on Wafer

In the “non-transfer stacking” scheme, plasma activation is applied only on chips to be self-assembled because the N₂ plasma treatment decreases the hydrophobicity of the regions surrounding the assembly areas. The water contact angle is reduced from 119° to 85° after N₂ plasma activation, as shown in Figure 6. When the low hydrophobic surrounding region is employed for self-assembly, the alignment accuracies are significantly decreased. Therefore, plasma activation is applied only on the surface of chips prior to self-assembly. The chips with CMP-treated PE-CVD oxide are self-assembled upside down to the host wafer. As shown in Figure 7a, almost all the chips exhibit high alignment accuracies within approximately 2 μm even when these chip are manually positioned at the release point higher than the surface of the droplets by 1 mm or more with coarse X/Y/θ pre-alignment. The average alignment accuracies of all self-assembled chips before direct bonding are −0.36 μm and 0.27 μm with a standard deviation of 1.46 μm and 1.10 μm in *x* and *y* directions, respectively. These accuracies include systematic errors caused by wafer tilt and *xy* silt in photolithography processes to define the size of chips and assembly areas. The size shrinkage of chips used in this study were within 2 μm that was resulted from the excess side etching under the plasma dicing conditions for fabricating thick chips with a thickness of 0.28 mm. In addition, the outer size patterns of the 5-mm-square chips and micro-vernier patterns formed on the chips to evaluate self-alignment accuracies were determined by a mask aligner that empirically gives alignment error

of $\pm 2 \mu\text{m}$ at most. However, misalignment of photomasks generally includes not only xy errors but also theta error, and thus, the potential maximum self-assembly error cannot be precisely defined. On the other hand, the average alignment accuracies and standard deviations with absolute numbers in x/y directions are $0.73 \mu\text{m} / 0.76 \mu\text{m}$ and $1.29 \mu\text{m} / 0.80 \mu\text{m}$ for all self-assembled chips before direct bonding, respectively. The relatively large statistics are explained by the local minimum energies that are present in this capillary chip self-assembly system. Ideally, a chip would be positioned to the center of the host hydrophilic assembly area by self-assembly, otherwise the chip would be positioned to the edges of the hydrophilic area. On the way to final positioning in self-assembly processes, the chips are often fixed due to the chip own weight against restoring forces driven by water surface tension and/or friction force from host wafers (hydrophobic surfaces) due to the chip tilt. The big statistics is also mainly attributed to the manual chip handling (not well controlled chip pre-positioning), giving large initial offsets in $x/y/z/\theta$ directions in addition to chip tilt prior to chip landing onto the top of the water droplets immediately after chip release [40–43]. We can further increase the alignment accuracies and reduce the variation by chip thickness reduction down to $100 \mu\text{m}$ or below, by the use of automatic/robotic chip handling systems, and by optimization of lithographic conditions using steppers to define the vernier positions toward outer sizes of the corresponding hydrophilic assembly areas.

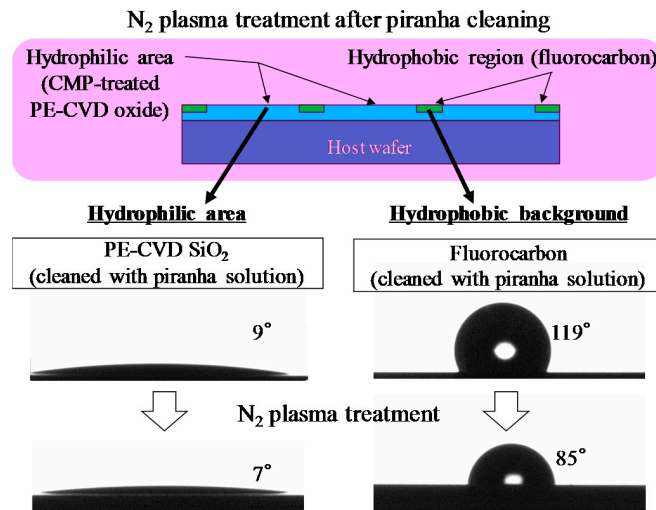


Figure 6. Water contact angles before and after N_2 plasma activation on a hydrophilic assembly area, and hydrophobic background region.

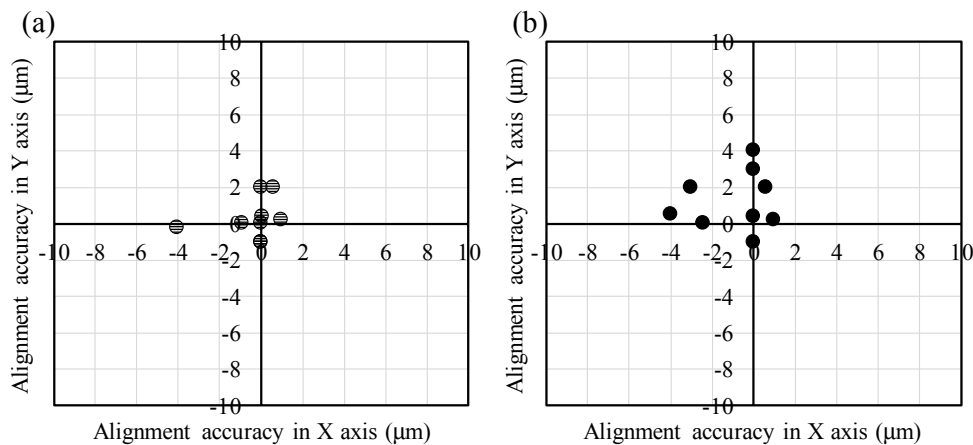


Figure 7. Alignment accuracies of self-assembled chips before and after thermal compression of MCtW direct bonding.

The following oxide-oxide direct bonding is carried out with the EV520 bonder to provide thermal compression through the flexible graphite sheet used as a TTV absorber for uniform compression of the self-assembled chips on the host wafers. As shown in Figure 8, these chips are precisely aligned and bonded on wafer when the high hydrophobic surrounding region are employed. Finally, these chips are annealed at 300 °C in vacuum under 5 Pa with a bonding load of 10 N/chip. Prior to the thermal compression process, the self-assembled chips are not tightly bonded on the wafer through Van der Waals interaction between the oxide surface and water used as a self-assembly mediate. As shown in Figure 7b, the alignment accuracies are slightly degraded due to the chip shift by the compressive force. The average alignment accuracies of all self-assembled chips after direct bonding in x and y directions are 1.22 and 1.46 μm with a standard deviation of 1.78 and 1.61 μm , respectively. The slight chip shift by thermal compression would be restricted by transfer-stacking based MCtW 3D integration with SAE carrier technologies in which self-assembled KGDs are temporarily fixed by electrostatic adhesion [28]. The yields of successful chip bonding are nearly 100% when we use 10 N/chip in bonding load. The resulting shear bonding strengths are 16.0 MPa on average for the CMP-treated chips conditioned with plasma activation and water dipping treatments. It is said that the effect of water dipping is much higher than that of plasma activation. These bonding strengths are sufficiently high enough to allow backside grinding and Si-CMP during multichip thinning.

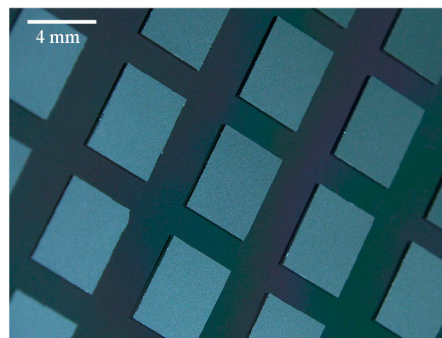


Figure 8. A photomicrograph of self-assembled chips directly bonded to a wafer through CMP-treated PE-CVD oxide.

2.4. Impact of Plasma Activation on Oxide-Oxide Direct Bonding

The effects of N_2 plasma irradiation and water dipping on MCtW direct bonding are characterized in this session. Therefore, most papers have discussed oxide-oxide bonding with thermally oxidized Si wafers and/or bare Si wafers in detail [30,31,44,45]. A few papers have described the detailed mechanism of direct bonding through CVD oxide [34,38].

Gösele et al. have reported that the chemistry of the Si-Si bonding process with wafers is basically the same as in the case of fused silica, since bare Si wafers are normally covered with at least a few angstroms of native oxide [30]. In the Gösele model, Van der Waals forces based on hydrogen bond networks between oxygen and hydrogen atoms dominates SiO_2 - SiO_2 direct bonding through absorbed water layers in which water molecules form a water cluster at the temperature of below 100 °C. As the temperature goes up at above 100 °C, the water can diffuse around the bonding interface, resulting in hydrogen bonds between silanol groups on the surface of upper and lower wafers. Then, covalent bonds of siloxane linkages are formed at the SiO_2 - SiO_2 bonding interface at temperatures ranging from 200 °C to 700 °C. It is not until the temperature is increased beyond 700 °C that the SiO_2 - SiO_2 interface permits closure of nano-gaps between the Si wafers. This mechanism of SiO_2 viscous flow at high temperature by annealing is illustrated in Figure 9a.

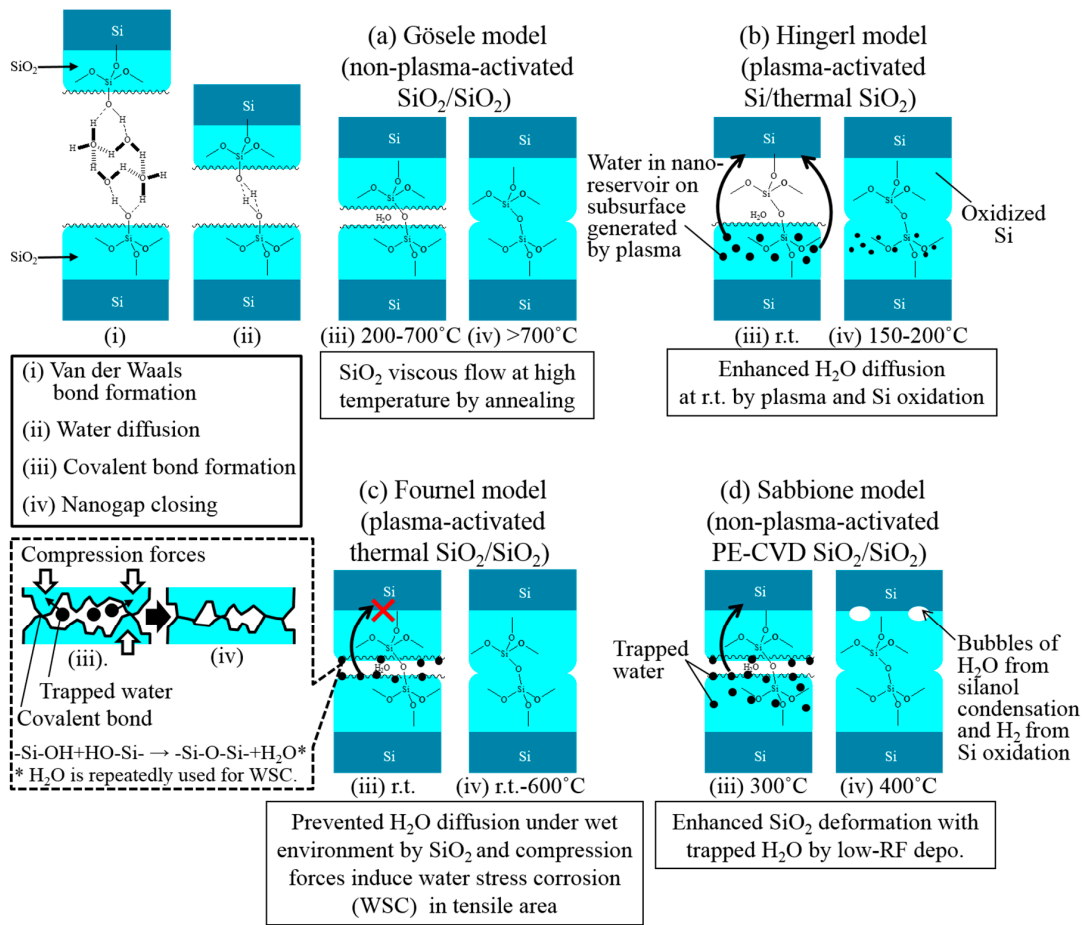


Figure 9. Four models of Si/SiO₂ and SiO₂/SiO₂ direct wafer bonding.

On the other hand, a model for plasma-activated oxide-oxide direct bonding of Si wafers has been recently proposed by Hingerl et al. [31]. They have described that the creation of subsurface defects (nano-reservoir) is caused by surface plasma irradiation and that the reservoirs contribute to the high surface energies of the directly bonded wafers. Figure 9b shows a schematic drawing explaining the nanogap closing mechanism on plasma-assisted direct bonding of Si wafers. Direct bonding with a thermally oxidized wafer and a bare Si wafer with a very thin native oxide layer is assumed in this model. As shown in the figure, the water trapped in the nano-reservoirs diffuses to Si bulk through a thin native oxide layer and oxidizes the Si to close the nanogap between the wafers by minimizing the sum of the free surface energy and strain energy in the oxide. By using the plasma surface activation, ≡Si–O–Si≡ covalent bonds would be not only formed at room temperature but also the closure of nanogaps could take place at around 200 °C. Although Hingerl et al. have not referred to their detailed SiO₂/SiO₂ bonding mechanism [31], the bonding energy seems to be lower than that of Si/SiO₂. Perhaps, this is because thick oxide layer prevents the diffusion of the water molecules into the Si bulk.

Fournel et al. have reported SiO₂/SiO₂ bonding mechanism where the difference between Si/SiO₂ and SiO₂/SiO₂ interfaces for plasma-activated direct bonding is described [34]. They have proposed roughness asperity evolution with internal water stress corrosion for plasma-activated Si/SiO₂ or SiO₂/SiO₂ direct bonding. In the Fournel model, as shown in Figure 9c, the interfacial water is consumed during low-temperature Si oxidation that starts around 150 °C, which means no remaining water at the Si/SiO₂ interface. In contrast, SiO₂/SiO₂ interfaces prevent the interfacial water from diffusing through the thick SiO₂ layers of a 145-nm-thick thermal oxide. Therefore, the remaining water between contacted asperities penetrates the tensile SiO₂ regions induced by compression forces,

and then, the small gaps are closed by the internal water stress corrosion at the SiO₂/SiO₂, resulting in high bonding energy.

In this work, to analyze the mechanism of plasma-assisted oxide-oxide direct bonding with a water dipping process, the water storage properties of CMP-treated PE-CVD SiO₂ surfaces with and without N₂ plasma irradiation were quantitatively measured with an APIMS. APIMS enables us to know the quite small amount of vaporized H₂O molecules desorbed from wafer surfaces at atmospheric pressure [46]. Compared with thermal desorption spectroscopy (TDS), APIMS can precisely detect H₂O concentrations because almost all H₂O molecules are desorbed from the surface of the wafers prior to measurement at a desired temperature region under the high-vacuum conditions of TDS. For the APIMS measurement, 0.28-mm thick Si wafers with a PE-CVD SiO₂ layer were prepared. The wafers were treated with/without N₂ plasma, and then, dipped into deionized water and subsequently spin-dried. After that, the wafers were set into an APIMS system and H₂O concentrations were detected. Figure 10 shows the water storage properties on the PE-CVD SiO₂ treated with/without N₂ plasma. In the figure, the *x*- and *y*-axis indicate measurement time and H₂O concentrations. 2498 ng of H₂O molecules were detected with a non-activated wafer with PE-CVD oxide, whereas 3304 ng of H₂O molecules were detected with the plasma-activated wafer with the oxide layer. As seen from these results, approximately 1.3-fold H₂O molecules are stored on/in the PE-CVD SiO₂ treated with N₂ plasma, compared with that without the plasma treatment. The water molecules stored on the surface of the PE-CVD SiO₂ layer are dramatically increased at above 70 °C. These results show that plasma activation is effective to obtain high-water-content surfaces. It can be said that the amount of absorbed water molecules on the surface of the oxide is increased by the plasma activation. There is also the possibility that the nano-reservoirs generated by the plasma irradiation process could contribute to the water storage property of SiO₂ surfaces as described by Hingerl et al. [31]. As reported by Fournel et al. [34], however, if water stress corrosion is happened at the plasma-activated PE-CVD SiO₂/SiO₂ interface, the high bonding energy under the condition #1 against #3 listed in Figure 2 is good agreement with their model dealing with internal water stress corrosion that induces high bonding energies. On the other hand, Sabbione et al. [38] have expatiated on the PECVD oxide-oxide direct bonding in which absorbed water in the oxide reduces the hardness as a mechanical property, leading to an increase in local bonding area due to the enhanced elastic deformation. In addition, low RF power of the PE-CVD oxide deposition gives a decrease in the modulus and hardness as well. They also have demonstrated that the absorbed water diffuses through a 400-nm-thick PE-CVD oxide and reaches Si bulk, followed by oxidation at 400 °C although plasma activation is not employed. Considering these previous works, it will be noted that water molecules play a crucial role for oxide-oxide direct bonding. As seen from the results obtained under the conditions #1 and #3 in Figure 2, our thermocompression oxide-oxide bonding would be affected by the internal water stress corrosion. In this study, it is not clear whether the silanol condensation and oxidation reactions are occurred at the Si/SiO₂ interface as shown in Figure 9d. However, our oxide-oxide thermocompression direct bonding is actually enhanced by “water” trapped on the surface (and/or subsurface) of and the inside of the PE-CVD oxide deposited at relatively lower RF. As seen from the APIMS analysis of the plasma-activated PE-CVD oxide, the water uptake quantity is undoubtedly high. As is also seen from the AMF profiles in Figure 3a,b, the asperity summits must be reduced by the plasma treatment. The elastic deformation of our PE-CVD oxides would be supported by the thermocompression bonding although Sabbione et al. have described small difference in bonding energy between thermocompression and load-free simple annealing [38]. The other parameters such as CMP/cleaning conditions, internal stress, the amount of Si–OH content on the surface of CMP-treated PE-CVD oxides, and the deposition temperature would impact on the thermocompression direct bonding energies. For these reasons, a comprehensive understanding of oxide-oxide bonding mechanisms warrants separate studies on PE-CVD chemistries.

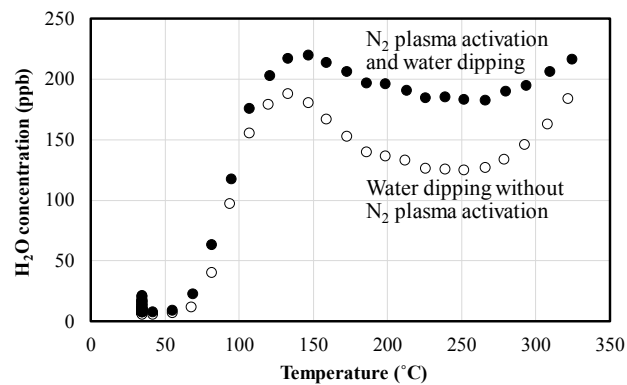


Figure 10. Water storage properties of PE-CVD SiO₂ layers with and without N₂ plasma irradiation.

3. Experimental Section

3.1. Chip/Wafer Fabrication

Chips and wafers used for self-assembly in this study were fabricated with 100-nm-thick thermally oxidized p-type Si(100) wafers with a thickness of 0.28 mm. In the chip fabrication process, micro-vernier patterns were formed on 1- μ m-thick PE-CVD oxide with 100-nm-thick sputtered Al by standard *i*-line photolithography with a mask aligner (MA8, SUSS MicroTec.) and the subsequent wet etching. The PE-CVD oxide was formed with tetraethyl orthosilicate (TEOS) at 350 °C in this study. The RF power of the PE-CVD system was 300 W. Then, an additional 2- μ m-thick PE-CVD oxide layer was planarized by SiO₂-CMP with a table-top high precision lapping machine (NF-300, Nanofactor) using a CMP pad of IC1000 (Nitta Haas Inc.) and a ceria-based slurry system consisting of CeO₂ (HS-8005) and additives (HS-8102GP), kindly supplied from Hitachi Chemical Co., Ltd., followed by cleaning with PC07B (Stella-Chemifa Co.) and water without ultrasonication. After that, plasma dicing was implemented with Bosch etching to obtain the 0.28-mm-thick chips to be self-assembled: the outer sizes of chips were also determined by the *i*-line photolithography technique. The resulting chip size was 4 mm \times 5 mm. On the other hand, the procedures of micro-vernier pattern formation and SiO₂-CMP on host wafers were the same to the chip fabrication. After the SiO₂-CMP process, recess etching with a depth of 10 μ m was performed on the planarized wafers. Finally, a 10-nm-thick fluorocarbon material was deposited on the wafers by a lift-off technique with acetone, resulting in an array of hydrophilic SiO₂ assembly areas and a hydrophobic fluorocarbon background region.

3.2. Self-Assembly

Self-assembly with the chips and the host wafers are schematically shown in Figure 11. The chips fabricated by plasma dicing is cleaned with a solution of H₂SO₄/H₂O₂/H₂O and then pre-treated with N₂ plasma using a widely-used sputtering system (SH-550, ULVAC) prior to self-assembly. The plasma activation power is 180 W and activation time is 1 min. On the other hand, the wafers were pre-treated without plasma irradiation: the wafers were only cleaned with the piranha solution (H₂SO₄/H₂O₂/H₂O) prior to self-assembly. Then, a microliter of pure water was supplied to each hydrophilic assembly area. After that, the chips with the hydrophilic oxide layer on their front-sides were coarsely pre-aligned with tweezers and placed upside down to the surfaces of the water droplet by hand. Immediately after chip release, the chips were precisely aligned to the pre-determined assembly areas formed on the host wafers. Finally, the water droplets were evaporated at room temperature to give MCtW structures in which the chips and wafers were bonded through hydrogen bond networks with the absorbed water molecules.

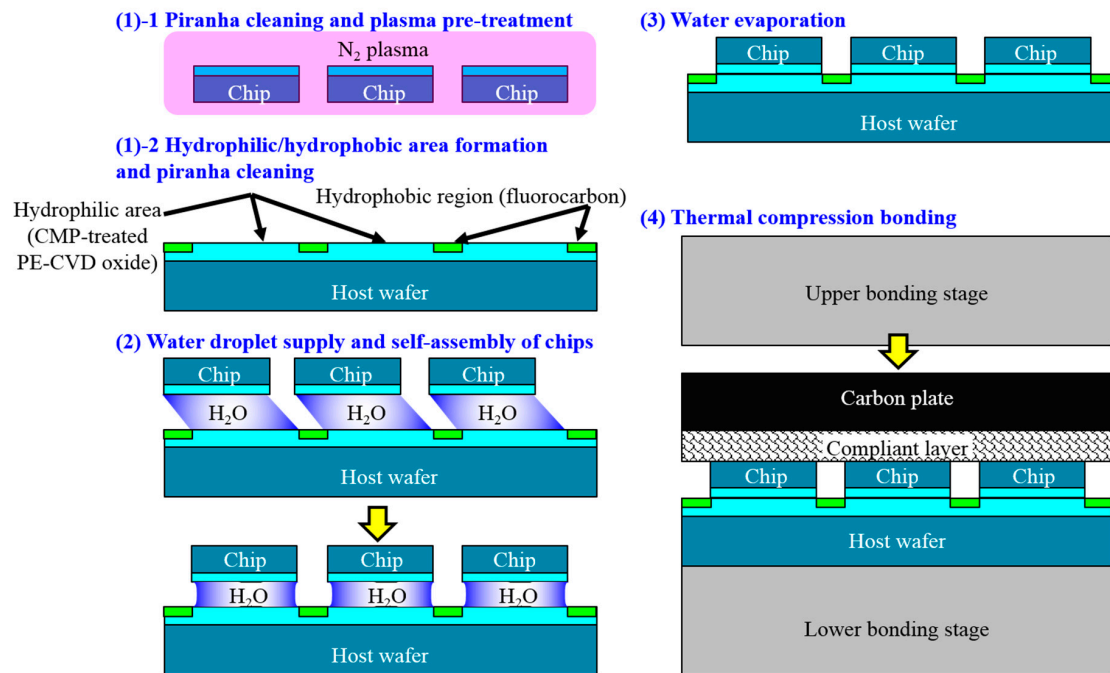


Figure 11. A process flow of MCtW self-assembly and direct bonding.

3.3. Contact Angle

The contact angle was measured on an optical contact angle meter (CAM101, KSV Instruments Ltd.) using a droplet of ultrapure water with a volume of approximately 1 μL by means of the sessile drop method. The droplet was monitored by a high resolution charge-coupled device (CCD) camera and analyzed by Drop Shape Analysis software (CAM 200, KSV Instruments Ltd.) utilizing a monochromatic light source which generates the highest quality images with minimal sample heating. The complete profile of the droplet was fitted by the Young-Laplace equation to give the slope at the three-phase boundary where a liquid, gas, and solid intersect. The resulting static contact angles were determined both at the right and left sides.

3.4. Bonding Strength

The shear bonding strength test was carried out with a multi-purpose bond tester (4000Plus, Dage Co.). DS100KG and SHR-250-3000 were used as a load cell and a shear tool: the length of the tip of the tool was 3 mm. Measurement conditions were 100 $\mu\text{m}/\text{s}$ in shear speed and 20 μm in shear height.

3.5. Alignment Accuracy

Alignment accuracies were evaluated by the observation of micro-vernier patterns formed on the surfaces of chips/wafers on an IR microscope (MX61L, Olympus) with an IR camera (ORCA-Flash4.0 V2 C11440-22C, Hamamatsu Photonics). The resolution is 2048×2048 pixels and the pixel size is $6.5 \mu\text{m} \times 6.5 \mu\text{m}$. The IR optical system gave space resolutions of $0.13 \mu\text{m} \times 0.13 \mu\text{m}$ for 50-power objective lens. The measurement resolution of the micro-vernier patterns is 0.2 μm .

3.6. Atomic Force Microscopy (AFM)

Surface roughness of Si substrates was characterized by AFM (Nano Cute, Seiko Instruments Inc.). The AFM topography images were operated in tapping mode by the use of phosphorous doped Si (1–10 $\Omega \cdot \text{cm}$) cantilevers. AFM images were recorded on a maximum scan region of $5 \mu\text{m} \times 5 \mu\text{m}$ and with 512 lines.

3.7. Atmospheric Pressure Ionization Mass Spectrometer (APIMS)

Plasma-activated and non-activated specimens were prepared on 2-inch wafers with a CMP-treated 2- μm -thick PE-CVD oxide layer. The desorption of H_2O molecules from the wafers were detected with an atmospheric pressure ionization mass spectrometer (APIMS) (UG-410P, Nippon API). The specimens were thermally annealed with a quartz glass furnace and an IR ray lamp. The measurement conditions were as follows: carrier gas was Ar, flow rate of Ar was 1 L/min, temperature range was 23 °C r.t. to 320 °C, and heating rate was 10 °C/min.

4. Conclusions

In this study, we demonstrated plasma- and water-assisted MCtW oxide-oxide thermocompression direct bonding at 300 °C using surface tension-driven self-assembled chips, and evaluated the effect of plasma activation and the subsequent water dipping processes on bonding properties (strength, yield, and uniformity). N_2 plasma was found to be more effective activation species for this direct bonding technology with PE-CVD oxide than Ar plasma. In addition, the bonding strengths obtained with PE-CVD oxide assisted by N_2 plasma and absorbed water were comparable to that obtained with thermal oxide in MCtW direct bonding process. We have not yet determined the presence of water reservoirs like nano- or micro-pores. However, it was noteworthy that water supply onto the surface and/or subsurface of the wafers was essential for high-strength and high-uniformity MCtW oxide-oxide direct bonding in addition to N_2 plasma assistance. The plasma activation is effective for obtaining the high-water-content surfaces on PE-CVD oxide, which is considered as an important parameter to obtain high bond strengths between the chips and the host wafers. This approach consisting of direct bonding with self-assembly can be expected for multichip grinding and TSV liner dielectric deposition in high-throughput and high-yield MCtW 3D integration with high-density via-last/back-via TSV formation due to the mechanically and thermally stable oxide-oxide bonding interface.

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Conflicts of Interest: The authors declare no conflict of interest.

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