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An 18.8–33.9 GHz, 2.26 mW Current-Reuse Injection-Locked Frequency Divider for Radar Sensor Applications

Kwang-Il Oh [1], Goo-Han Ko [1], Jeong-Geun Kim [2] and Donghyun Baek [1,*]

[1] Microwave Embedded Circuit & System (MECAS) Lab., School of Electrical Engineering, Chung-Ang University, 84 Heukseok, Dongjack, Seoul 06974, Korea; dhrhkddlf123@cau.ac.kr (K.-I.O.); rngks79@cau.ac.kr (G.-H.K.)

[2] Integrated Radar Lab., Department of Electronic Engineering, KwangWoon University, 20 Gwangun, Nowon, Seoul 01897, Korea; junggun@kw.ac.kr

* Correspondence: dhbaek@cau.ac.kr; Tel.: +82-02-820-5828

Abstract: An 18.8–33.9 GHz, 2.26 mW current-reuse (CR) injection-locked frequency divider (ILFD) for radar sensor applications is presented in this paper. A fourth-order resonator is designed using a transformer with a distributed inductor for wideband operating of the ILFD. The CR core is employed to reduce the power consumption compared to conventional cross-coupled pair ILFDs. The targeted input center frequency is 24 GHz for radar application. The self-oscillated frequency of the proposed CR-ILFD is 14.08 GHz. The input frequency locking range is from 18.8 to 33.8 GHz (57%) at an injection power of 0 dBm without a capacitor bank or varactors. The proposed CR-ILFD consumes 2.26 mW of power from a 1 V supply voltage. The entire die size is 0.75 mm × 0.45 mm. This CR-ILFD is implemented in a 65 nm complementary metal-oxide semiconductor (CMOS) technology.

Keywords: current-reuse; injection-locked frequency divider; radar sensor; wideband

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1. Introduction

Recently, the demand for radar sensors has been rapidly increasing with the development of the Internet of Things (IoT) industry and the autonomous vehicle industry. The complementary metal-oxide semiconductor (CMOS) radar is characterized by various operating methods such as doppler, frequency-modulated continuous wave (FMCW), and (continuous-wave) CW. In the doppler radar, a low frequency to millimeter-wave (mm-Wave) must be used to acquire a two-dimensional image through synthetic aperture radar (SAR). Bandwidths of 500 MHz or more are used to obtain high-resolution images [1,2]. In addition, wideband performance is very important in frequency-modulated continuous wave (FMCW) radars because wideband chirp is directly related to the high-resolution distance information [3]. Therefore, the wideband performance of the signal generator, the core of the sensor, is required [4,5].

Generally, the performance of the phase-locked loop (PLL) in the signal generator must be concerned to obtain low noise mm-Wave signals. Figure 1 shows the block diagram of conventional PLL structure that consists of a phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage-controlled oscillator (VCO) and frequency divider. The key blocks that determine the specification of the PLL in the mm-Wave band are VCO [6,7] and frequency divider [8]. The mm-Wave frequency divider should operate at high speed and should have a wide operating range for applying the wideband sensor applications.

Frequency dividers are designed as the current mode logic (CML) divider, regenerative divider, and LC oscillator-based injection-locked frequency divider (ILFD). The CML divider is a combination of two flip-flops that perform simple logical operations [9–12]. Generally, CML dividers have a wide operating range and occupy a small chip area with no inductor design. However, CML dividers suffer from large power consumption, limited maximum operation frequency, and process, voltage, and temperature (PVT)

variation at the mm-Wave. To address these shortcomings, tunable self-resonant circuit [9], dynamic latches with load modulation [10,11], and additional calibration circuits [12] have been studied. However, these still consume large powers of 4.8 [11], and 6.2 mW [12], respectively. The regenerative divider and ILFD are also popular frequency dividers. These two types of frequency dividers are LC oscillator-based circuits and both of them are quite similar. The regenerative divider comprises an LC-based band pass filter (BPF) and active-type mixer [13–15]. The active type of mixer consumes power and takes over the role of $-g_m$ core. Conversely, the ILFD comprises an LC-based BPF, $-g_m$ core, and passive-type mixer that does not consume power. Therefore, regenerative dividers consume more power than ILFDs and are not generally used for mm-Wave applications because of the influence of many parasitic capacitors of the active-type mixer such as the Gilbert cell. The even-harmonic mixer [14] and digital-assisted circuit [15] are employed to widen the locking ranges of the regenerative divider. Their locking ranges are 33% and 57.4%, respectively. However, the highest input frequencies are limited to 18.4 and 14.8 GHz, consuming 10.8 and 12 mW power, respectively.

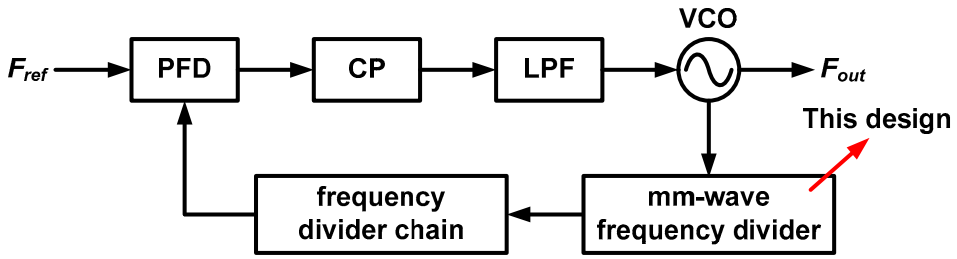


Figure 1. Conventional phase-locked loop with mm-Wave frequency divider.

The most attractive mm-Wave frequency divider is the LC oscillator-based ILFD. The reasons for its high popularity are as follows. First, the ILFD self-oscillates when there is no input signal applied. It is possible to obtain a large output signal with a small input signal using the oscillator-based operation. Second, because of the LC resonator, the ILFD is advantageous for operation at the mm-Wave band. Finally, because the ILFD uses a passive type of mixer, it consumes less power than regenerative and CML dividers. However, the disadvantage is that the locking range is narrow because of a high-quality factor (Q) LC resonator. Several studies are being conducted to widen the locking range of ILFD [16–18]. The forward-body-bias techniques [16,17] are some of the effective ways of increasing the gain of the mixer and extending the locking range. Although the ILFD with the forward-body-bias techniques have a wide locking range of 90% in [17], there are several reasons why this technique is impractical in mm-Wave synthesizers. First, if a positive bias is applied to the body of an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET), the leakage current cannot be ignored, and the possibility of a large diffusion current flow because of forward-bias increases. Second, the power of the harmonic signal increases because of non-linearity in devices. Applying an injection signal with an edge frequency in the locked range can make it difficult to distinguish the power difference between the output and harmonic signals. Finally, an additional circuit may be required to control the harmonic power, which can increase the circuit complexity and power consumption. The dual-resonance resonator is also considered as a suitable technique [18]. This ILFD has a locking range of 71.46%; however, it requires external bias control and has a small output power. Moreover, when a -3 dBm injection power is applied, an unlocking part occurs in the locking range.

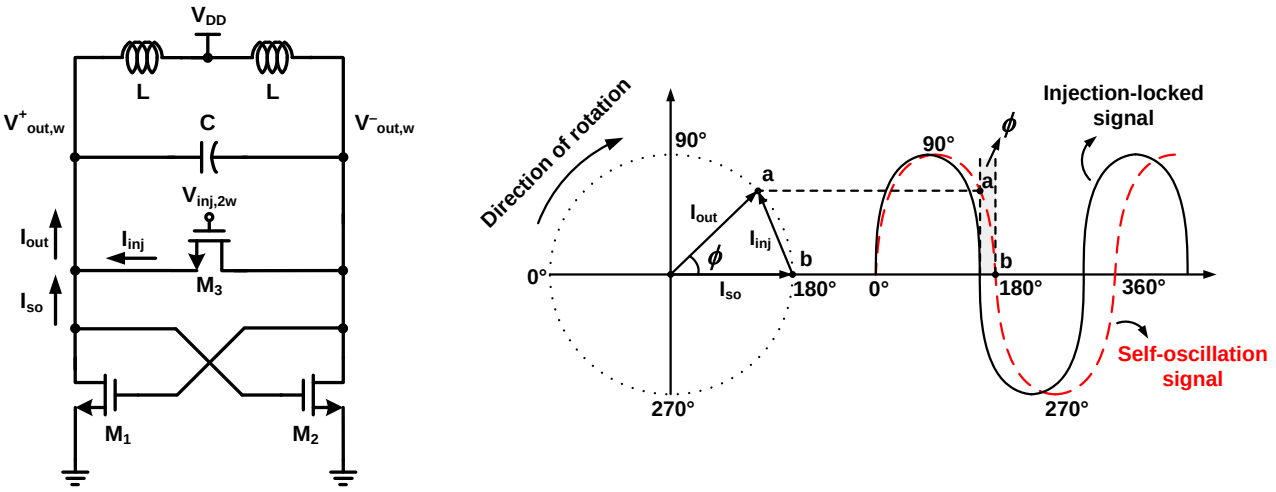
In this paper, a low power and wide locking range LC oscillator-based current-reuse (CR) ILFD using a fourth-order resonator with the distributed inductor is proposed. The CR technique is employed to reduce power consumption. This paper is organized as follows. Section 2 presents an analysis of the ILFD locking range. The limitations of the maximum locking range and harmonic issues are also presented. Section 3 presents the circuit design of the proposed CR-ILFD including the modeling of the transformer and

design flow chart. The measurement results are shown in Section 4. Finally, conclusions are organized in Section 5.

2. Locking Range Analysis of ILFD

Figure 2a shows a schematic of the conventional cross-coupled pair ILFD with a second-order resonator. This ILFD consists of an N-channel metal-oxide semiconductor (NMOS) cross-coupled pair (M_1, M_2), injection switch (M_3) and LC resonator. The ILFD self-oscillates if there is no injection signal at the gate of M_3. Biasing the injection signal of $V_{inj,2w}$ at the gate of M_3, the ILFD outputs $V^+_{out,w}$ and $V^-_{out,w}$. When the frequency of the output signal is exactly half the frequency of the injection signal, it is referred to as "locking". To easily understand the locking operation, the current is classified into three types, namely, I_{so}, I_{inj}, and I_{out}. I_{so} represents the self-oscillation current flowing through the core when the ILFD self-oscillates without an injection signal. I_{inj} is the injection current flowing through M_3 when an injection signal is applied. I_{out} is the output current, which is the sum of I_{so} and I_{inj}. Figure 2b shows the phasor diagram for the three current types. The phasor rotates clockwise. Point "a" shows that the phase has changed from I_{so} by ϕ. Point "b" shows the phase when the ILFD self-oscillates without an injection signal. The relational expression of the current vectors is as follows.

$$I_{out} = I_{so} + I_{inj}. \tag{1}$$



(**a**) (**b**)

Figure 2. (**a**) Schematic of the conventional cross-coupled pair ILFD with second-order resonator and (**b**) phasor diagram for the basic principle of the conventional ILFD.

Two waves are shown in Figure 2b, one is the self-oscillation signal of the ILFD and the other is the injection-locked signal. Point "b" of the self-oscillation signal is moved to point "a" by the injection signal. Therefore, the phase at 180° of the injection-locked signal is point "a" of the self-oscillation signal. Injection is instantaneously performed every half period, and the range of ϕ can be derived using the following equations.

$$\phi = \angle I_{out} = \angle\left(I_{so} + I_{inj}\right), \tag{2}$$

$$V_{out} = Z_L \cdot I_{out}, \tag{3}$$

$$\angle I_{out} = \angle V_{out} - \angle Z_L, \tag{4}$$

where V_{out} is the output voltage signal when the ILFD is locked, and Z_L represents the load impedance of the LC resonator. Equation (4) can be derived using the phasor in (3).

To replace V_{out} with the self-oscillation and injection signals, the following equations are derived as

$$V_{out} = V_{so} + V_{inj}, \tag{5}$$

where V_{so} is the output voltage signal when the ILFD self-oscillates and V_{inj} is the injection voltage signal generated from M_3. It should be noted that V_{inj} is different from the input voltage signal, $V_{inj,2w}$. According to Equations (4) and (5), the ϕ is calculated as

$$\phi = \angle(V_{so} \pm V_{inj}) - \angle Z_L. \tag{6}$$

The sign of V_{inj} is determined based on the value of the locked frequency relative to the self-oscillation frequency. When the ILFD self-oscillates with no injection signal, (6) is calculated as follows.

$$\phi|_{V_{inj}=0} = \angle\, V_{so} - \angle\, Z_L. \tag{7}$$

V_{inj} is zero, and V_{so} is expressed as the product of I_{so} and Z_L. Because Z_L is canceled out, the following equation is satisfied:

$$\phi|_{V_{inj}=0} = \angle I_{so}. \tag{8}$$

Meanwhile, ϕ_{max} is derived when the following condition is satisfied:

$$I_{out} \perp I_{inj}. \tag{9}$$

The largest angle between I_{so} and I_{out} can be realized by considering the phasor as shown in Figure 2b. This is the condition of (9) where I_{out} and I_{inj} are vertical. Using the trigonometric function,

$$\sin\phi_{\max} = \pm\frac{|I_{inj}|}{|I_{so}|}, \tag{10}$$

$$\phi_{\max} = \pm\arcsin\left(\frac{|g_{inj} \cdot V_{inj}|}{|g_m \cdot V_{so}|}\right), \tag{11}$$

where g_m and g_{inj} represent the transconductance of the cross-coupled pair and injection switch, respectively.

According to (6), the conditions for extending the locking range of the ILFD can be determined qualitatively. First, the magnitude of the self-oscillation signal V_{so} is decreased by reducing the sizes of M_1 and M_2 to decrease the transconductance of the cross-coupled pair. However, when the transconductance of the cross-coupled pair is too small, it can make failure in the self-oscillation, causing the ILFD to act as a harmonic buffer. Second, to increase the amplitude of V_{inj} generated by M_3, the size of M_3 can be increased or the injection signal $V_{inj,2w}$ can be amplified. However, the operation frequency may be limited by large parasitic capacitors. A pre-buffer, which consumes additional power, will be required to increase the amplitude of $V_{inj,2w}$. Finally, the phase of the load impedance can be changed. The phase of Z_L can increase or decrease ϕ. However, the maximum and minimum values of the phase, $\pm\phi_{\max}$, limit the range of ϕ. Therefore, the phase of Z_L should be close to zero value in the wide frequency range. In conclusion, the maximum and minimum values of ϕ are determined by (11), and the method of extending the range of ϕ is consistent with the equation in (6).

The power of the output signal should be greater than that of the input signal. Two graphs of the load impedance magnitude against the angular frequency are shown in Figure 3, which presents two cases. The first case is the normal case where the power of the input signal is significantly smaller than that of the output signal as shown in Figure 3a. The range from w_1 to w_2 is the operation frequency band obtained by dividing by two, and the range from $2w_1$ to $2w_2$ is the injection frequency band. The operation and injection frequency bands do not overlap in the normal case because $2w_1$ is larger than w_2. Therefore, the input signal does not exceed the start-up condition and is not amplified more than

the output signal. The second case is the abnormal case where the power of the input signal can be larger than that of the output signal, as in Figure 3b. Here, the operation and injection frequency bands overlap because $2w_1$ is smaller than w_2. The injection frequency band contains the parts that exceed the start-up conditions, which are determined by the following "Barkhausen formula".

$$g_m \cdot |Z_L| \geq 1. \tag{12}$$

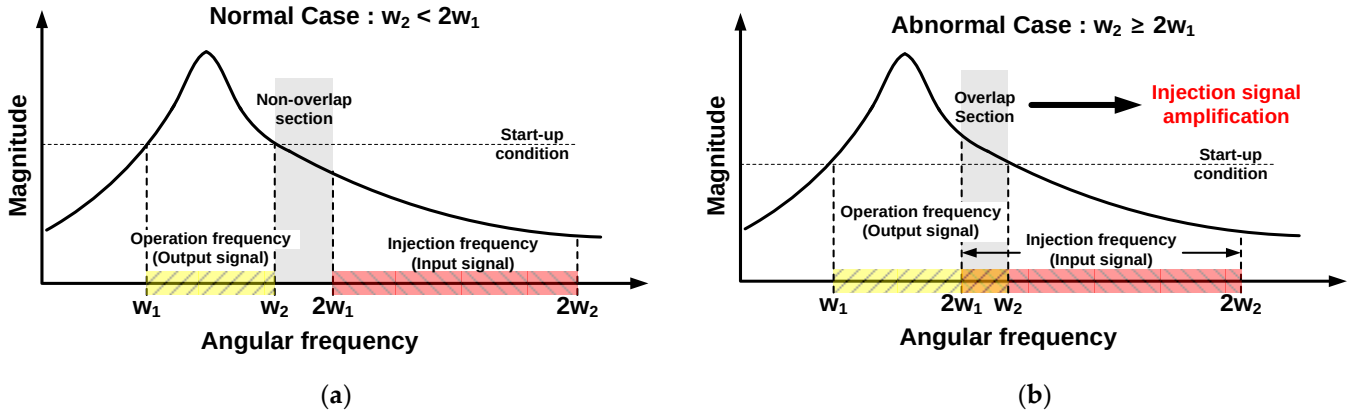


Figure 3. Graphs of magnitude of load impedance against angular frequency; (**a**) normal case, (**b**) abnormal case.

In the abnormal case, the ILFD cannot be used in mm-Wave applications, because the input and output signals are amplified together in the frequency band used.

This problem can be solved by increasing the division ratio of the ILFD. However, to operate at high division ratio, a harmonic signal with a small magnitude should be used, which results in a narrow locking range of the ILFD [19,20]. Additionally, the injection mixer for the high division ratio creates larger parasitic capacitance than the injection switch of the divide-by-two ILFD. Consequently, an ILFD that operates at a high division ratio greater than two is disadvantageous for application in the mm-Wave band. Therefore, a divide-by-two ILFD optimized to have a wide locking range without including the abnormal case would be most suited as a mm-Wave frequency divider. The following equation is used to calculate the locking range of the ILFD.

$$LR = \frac{w_2 - w_1}{w_1 + (w_2 - w_1)/2} \cdot 100\ (\%). \tag{13}$$

Under the normal case condition, $w_2 < 2w_1$, the maximum locking range of the divide-by-two ILFD can be obtained when w_2 is equal to $2w_1$. Therefore, the maximum locking range is

$$LR_{\max}|_{w_2=2w_1} = 66.7\%, \tag{14}$$

where LR is the locking range. If the locking range of the divide-by-two ILFD exceeds 66.7%, the power of the input signal may be greater than that of the output signal. In conclusion, the locking range of the ILFD should be designed to be less than 66.7%.

3. Circuit Design of Proposed CR-ILFD

3.1. Fourth-Order Resonator and CR Core

As mentioned in the previous section, to extend the locking range of the ILFD, the phase plot of the load impedance should be flat in the range of $\pm\phi_{\max}$ [8,21]. A fourth-order resonator with two poles is required to flatten the phase plot. Figure 4a shows a schematic of the conventional cross-coupled pair-based ILFD with a fourth-order resonator consisting of a resonator (L_1, C_1, R_1, L_2, C_2, R_2), cross-coupled pair (M_1, M_2) and injection switch (M_3).

The "k" is the coupling factor between L_1 and L_2. Z_L is the load impedance of the resonator, which is calculated as

$$Z_L = \frac{(1-k^2)L_1L_2C_2s^3 + L_1s}{(1-k^2)L_1L_2C_1C_2s^4 + (L_1C_1 + L_2C_2)s^2 + 1}. \quad (15)$$

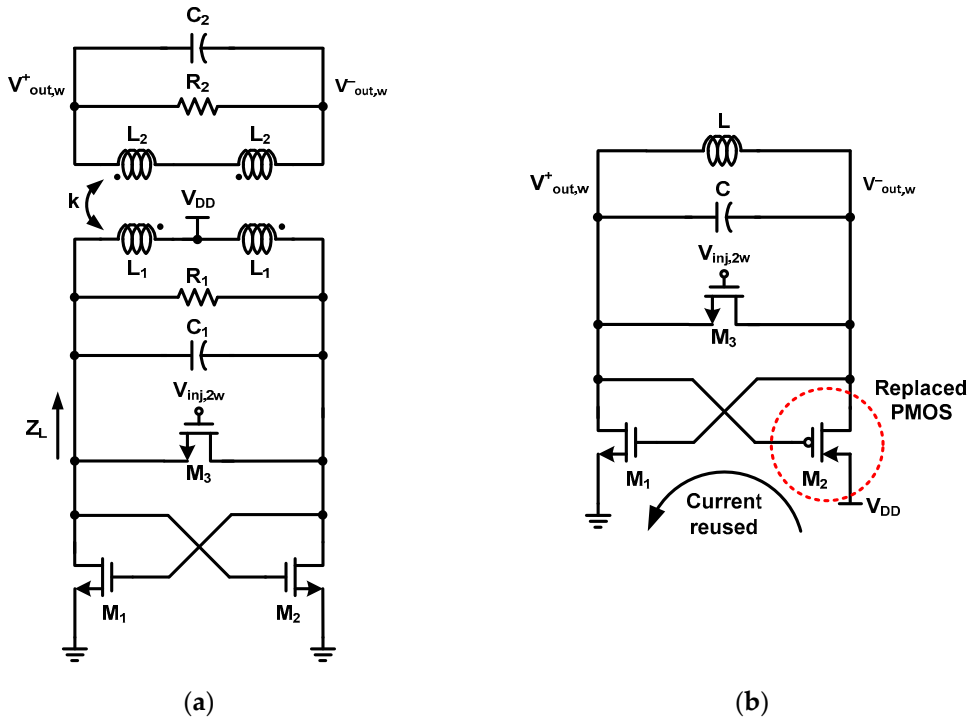


Figure 4. Schematic of (**a**) conventional cross-coupled pair ILFD with fourth-order resonator and (**b**) CR core-based ILFD.

R_1 and R_2 are resistors that affect the quality (Q) factor of the resonator and have been approximated in this calculation. Two poles that make the denominator zero are represented using the following equation [22],

$$w_{R,L} = \sqrt{\frac{L_1C_1 + L_2C_2 \pm \sqrt{(L_1C_1 + L_2C_2)^2 - 4(1-k^2)L_1L_2C_1C_2}}{2(1-k^2)L_1L_2C_1C_2}}. \quad (16)$$

Assuming that $L_1 = L_2$ and $C_1 = C_2$,

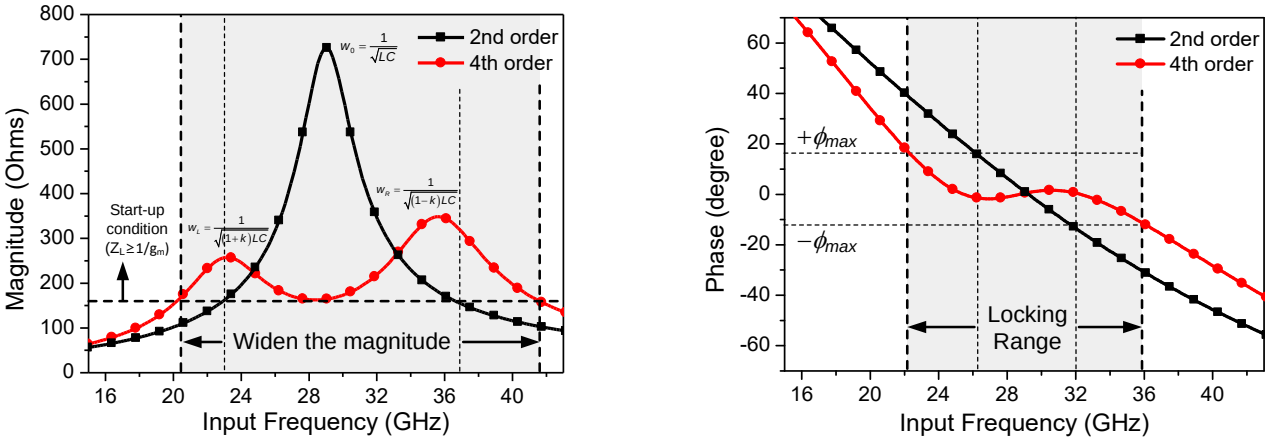
$$w_{L,R} = \frac{1}{\sqrt{(1 \pm k)LC}}. \quad (17)$$

According to (17), the distance between the two poles increases as the value of k increases and the distance between the two poles decreases as the k value decreases. If k is zero, the pole value is obviously equal to that of the second-order resonator (18). Figure 4b shows a schematic of the conventional ILFD with the CR core. For the CR core, M_2 of the cross-coupled pair ILFD in Figure 2a is replaced by P-channel metal-oxide semiconductor (PMOS) [23–27]. The oscillation of the CR core can be divided into two half periods. In the first half period, the current flows through M_1 and M_2, and in the second half period, no current flows through M_1 and M_2. Unlike the oscillation in the cross-coupled pair core, the oscillation of the CR core reduces the current by simultaneously turning the MOSFET on and off [24].

Figure 5 shows the magnitude and phase plots of the second- and fourth-order resonator-based ILFDs. The schematic of the second-order resonator-based ILFD is shown

in Figure 2a. Figure 5a shows the graph of the load impedance magnitude against the input frequency. The second-order resonator-based ILFD has one pole, w_0, that is expressed as follows.

$$w_0 = \frac{1}{\sqrt{LC}}. \tag{18}$$



(**a**) (**b**)

Figure 5. (**a**) Simulated magnitude plot and (**b**) phase plot of second-order resonator-based ILFD and fourth-order resonator-based ILFD.

If the fourth-order rather than the second-order resonator-based ILFD is applied, the magnitude plot of the load impedance becomes wider even if the maximum magnitude value decreases. However, because a new minimum value occurs between the two poles, it is necessary to simulate whether locking is sufficiently achieved at this value. If the minimum value between the two poles is less than the start-up condition (12), the ILFD does not operate in that frequency range. Figure 5b shows the phase plot against the input frequency. According to (11), the $\pm\phi_{\max}$ limits the locking range of the ILFD. Unlike the phase of the second-order resonator-based ILFD, that of the fourth-order resonator-based ILFD has a value approximately equal to zero over a wide frequency range because of the formation of a ripple. Consequently, the simulated locking range of the ILFD is increased by 22% from 26–32 GHz (21%) to 22–36 GHz (43%).

3.2. Proposed CR-ILFD

Figure 6 shows a schematic of the proposed CR-ILFD, consisting of a fourth-order resonator (L_1, C_1, L_2, C_2), distributed inductor (L_3), injection switch (M_3), CR core (M_1, M_4), center-tap generator (M_2, M_5), and output buffer. $V_{inj,DC}$ and $V_{inj,2w}$ are the input signals, whereas $V_{out,w}$ is the output signal. The center-tap generator biases the node of the primary coil, L_1 to V_{CT}. If the g_m matching of PMOS and NMOS is well adjusted, mathematically, V_{CT} would be $V_{DD}/2$. The DC value of the injection switch can be biased to V_{CT} without additional supply, but it was not connected for measurement. The distributed inductor is employed to extend the locking range of the ILFD. The distributed inductor is also referred to as the inductor distributed technique [28,29]. The magnitude of the load impedance can be increased by distributing the primary inductor into two series inductors.

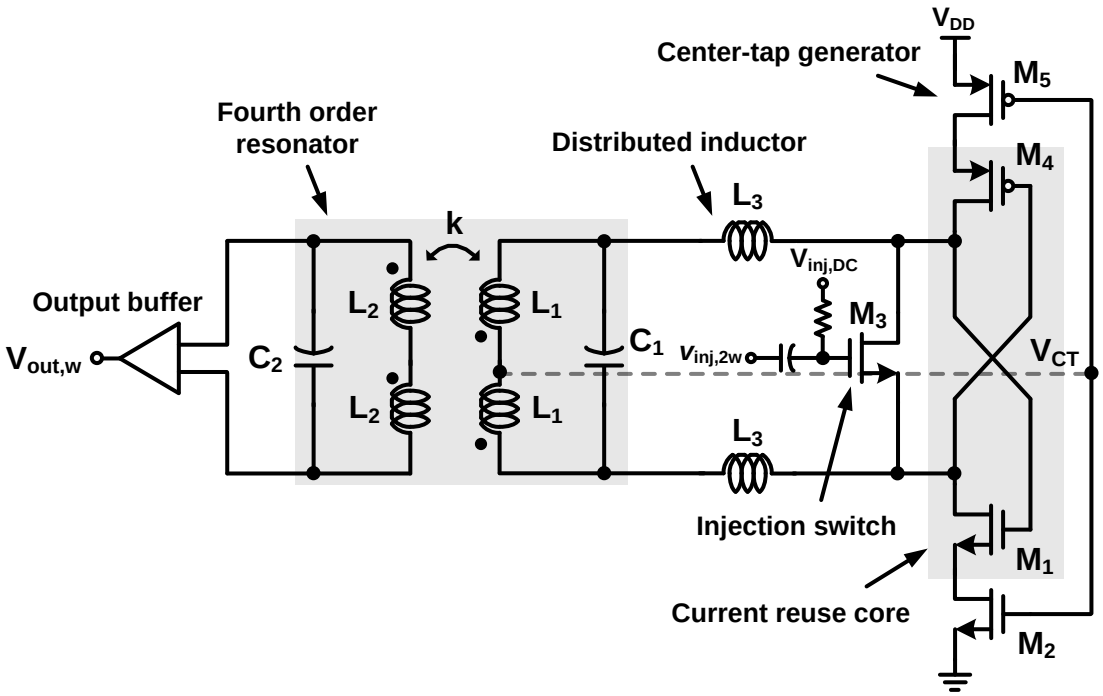
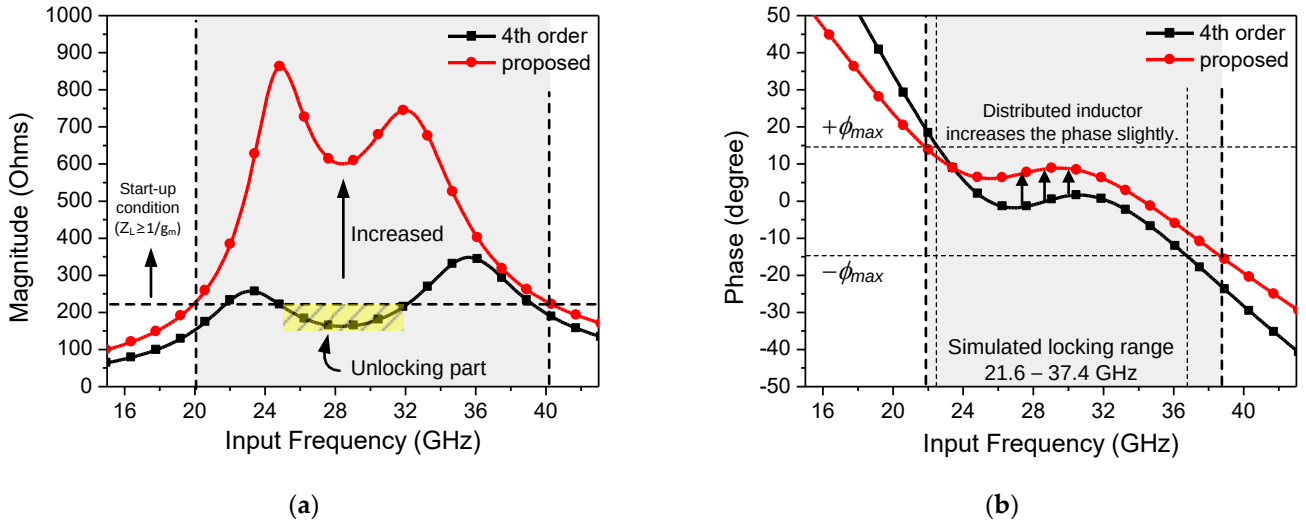


Figure 6. Schematic of the proposed CR-ILFD.

Figure 7a shows the simulated magnitude plot and phase plot of the fourth-order resonator-based ILFD and the proposed CR-ILFD with the fourth-order resonator with a distributed inductor. The start-up condition in Figure 7a is determined by the "Barkhausen formula" in (12). In the case of the fourth-order resonator-based ILFD, an unlocking part may occur because of the minimum value that is less than the start-up condition. However, the magnitude of the load impedance is sufficiently increased by using the inductor distributed technique. Figure 7b shows the slightly increased phase. This is not a critical amount of change because the phase ripple still exists between the $\pm\phi_{\max}$. The simulated locking range of the proposed ILFD is from 21.6 to 37.4 GHz, which is limited by the $\pm\phi_{\max}$ in (11).



(**a**) (**b**)

Figure 7. (**a**) Simulated magnitude plot and (**b**) phase plot of the fourth-order resonator-based ILFD and proposed CR-ILFD.

Figure 8 shows an equivalent model of the fourth-order resonator using a transformer with the distributed inductor. Figure 8a shows a model including the parasitic capacitors

and resistors of the passive components. Zin is the input impedance and "k" is the coupling factor between L_1 and L_2. C_{p1}, R_{p1}, C_{p2}, and R_{p2} represent the parasitic components. In the mm-Wave band, the analog circuits are affected more by electromagnetism. Therefore, the modeling of the resonator must be considered at the initial design stage. Because analyzing every parasitic component is difficult, modeling should be simplified by approximation as shown in Figure 8b. C_{T1} is the sum of C_{p1} and C_1. Similarly, C_{T2} is the sum of C_{p2} and C_2. Additionally, the Q factor of the inductor includes the parasitic resistances. V_t and I_t are the test voltage and test current, respectively. V_t/I_t is equal to Z_{in} in the simplified model. The value of Z_{in} is calculated as follows.

$$Z_{in}(s) = \frac{(1-k^2)L_1L_2C_{T2}s^3 + L_1s}{(1-k^2)L_1L_2C_{T1}C_{T2}s^4 + (L_1C_{T1} + L_2C_{T2})s^2 + 1} \times (1 + 2L_3C_{T1}s^2). \quad (19)$$

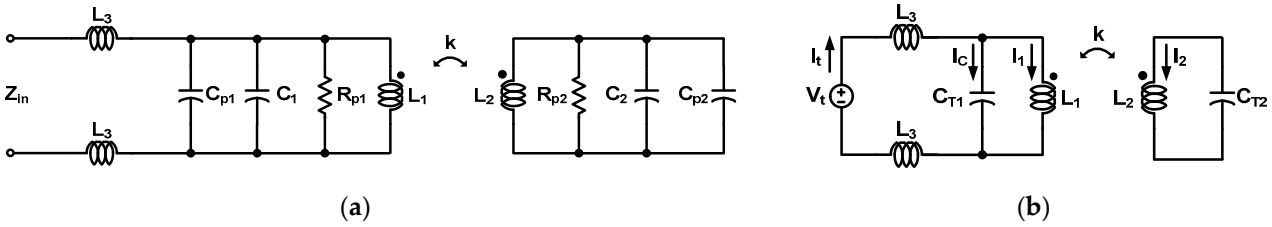


Figure 8. (**a**) Modeling of the fourth-order resonator using a transformer with distributed inductor. (**a**) Modeling of including the parasitic capacitors and resistors. (**b**) Approximate modeling applied to simplify calculations.

If the distributed inductor (L_3) is zero, then (19) is equal to (15). That is, the distributed inductor does not directly affect the pole value in (17), and if the distributed inductor value is increased, the magnitude of Z_{in} can be increased.

The design parameters are listed in Table 1. Because the center-tap generator should not limit the core operation, the width of the center-tap generator should be significantly larger than that of the CR core. The parasitic capacitor of the center-tap generator is separated from the resonator and does not affect the operating frequency. The sizes of the CR core and injection switch are not only determined by (11) and (12), but also by the influence of the parasitic capacitors.

Table 1. Design parameters of the proposed CR-ILFD.

Design Parameter	Value
M_1, M_2, M_4, M_5 (unit W/L)	2 µm/0.06 µm
M_3 (unit W/L)	1 µm/0.06 µm
Finger of M_1, M_3, M_4	20
Finger of M_2, M_5	50
L_1	230 pH
L_2	265 pH
L_3	433 pH
k	0.51
C_1	144 fF
C_2	240 fF

Figure 9 shows a flowchart of the design approach for the proposed CR-ILFD. First, the equivalent circuit model must be implemented in the simulator. Second, the values of the design parameters should be determined. In the proposed CR-ILFD, the center frequency is set to receive an injection signal of 28 GHz. Because the distributed inductor does not directly affect the pole value, the values of L_1, C_1, L_2, C_2 and k are first determined. Subsequently, L_1 is divided into two series inductors, L_1 and L_3. In this design, L_1, L_2, and L_3 are 230, 265, and 433 pH, respectively. C_1 and C_2 are 144 and 240 fF, respectively. The value of k is 0.51. When $k < 0.5$, which represents a weak coupling, the distance between

the poles increases, and a wide magnitude plot of the load impedance can be obtained. However, a coupling that is too weak can cause an unlocking part in which the ILFD does not work. Considering the locking range and unlocking part, the proposed CR-ILFD is designed with a coupling factor of 0.51. Finally, the layout and locking simulation are repeated in the order shown in the flowchart. Electromagnetic simulation is essential in the mm-Wave band. Therefore, it should be ensured that the difference between the equivalent modeling and implementation in the simulation of this circuit is reasonable.

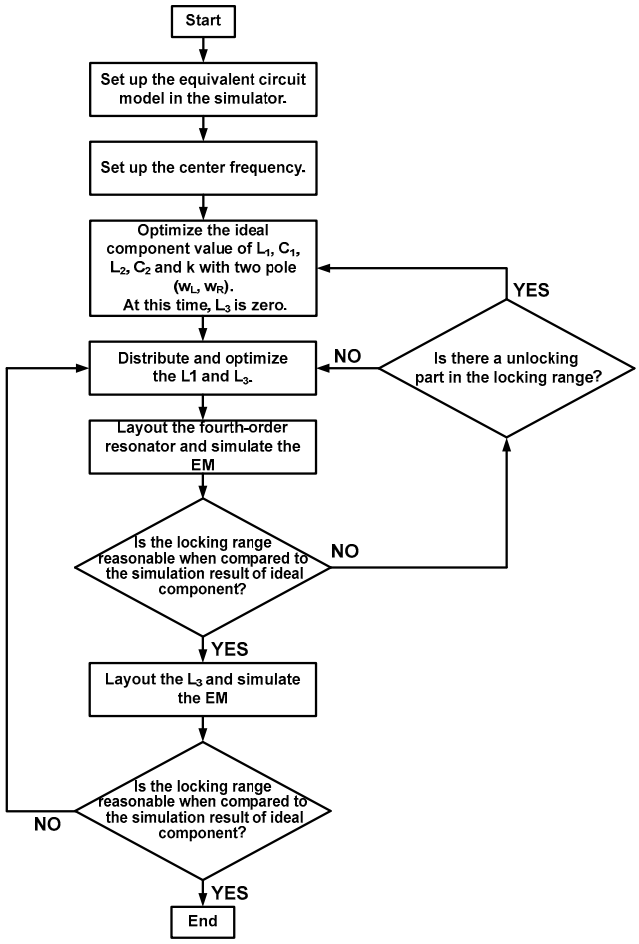


Figure 9. Flowchart of the design approach for the proposed CR-ILFD.

4. Measurement Results

Figure 10 shows the die photograph of the proposed CR-ILFD, which was fabricated in a 65 nm CMOS technology. The die size including the entire pad is 0.75 mm × 0.45 mm and the chip size including the core and output buffer is 0.49 mm × 0.3 mm. The measurement setup for the proposed CR-ILFD is shown in Figure 11. The measurements were obtained using a probe station. The DC voltage was biased from the power supply. The CR core of the proposed CR-ILFD consumes 2.26 mW from a 1 V supply voltage, when no signal is applied to the injection switch. As $V_{inj,DC}$ increases, the power consumption increases. When $V_{inj,DC}$ is 0.7 V, the power consumption of the core increases by approximately 0.5 mW. The power consumption of the output buffer is approximately 3 mW. The injection signal was generated by Anritsu MG3694, which can generate frequencies up to 40 GHz. The output signal of the proposed CR-ILFD is analyzed by KEYSIGHT N9030B, which can analyze frequencies up to 50 GHz. When conducting measurements using mm-Wave signals, several losses occur around the device under test (DUT). Therefore, the calibration tests must be carried out carefully. In this measurement, the ground–signal–ground (GSG) probe tip has a loss of approximately 2.5 dB and that of the radio frequency (RF) cable has

approximately 3 dB. Approximately a 1 dB loss occurs even when the signal generator output is 10 dBm. The loss of the signal generator was analyzed by connecting the signal analyzer and RF cable. All losses described above are based on the 28 GHz signal. Generally, the loss increases as the frequency increases, and decreases as the frequency decreases.

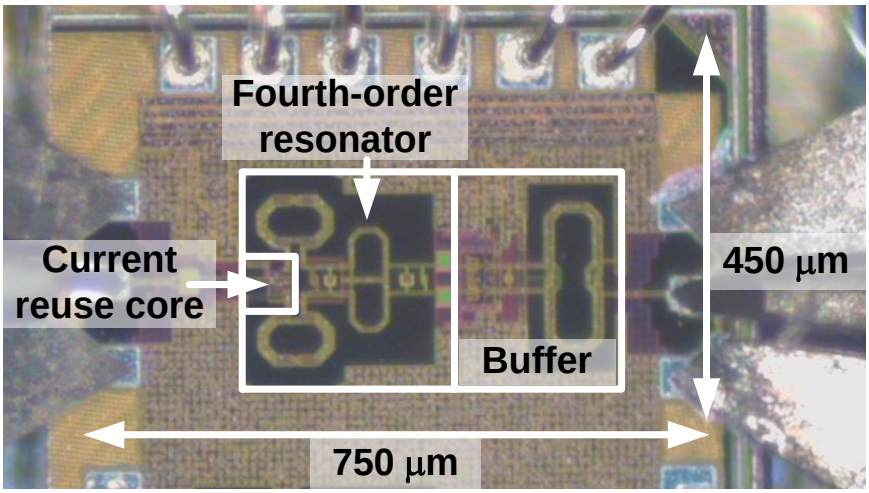


Figure 10. Die photograph of the proposed CR-ILFD.

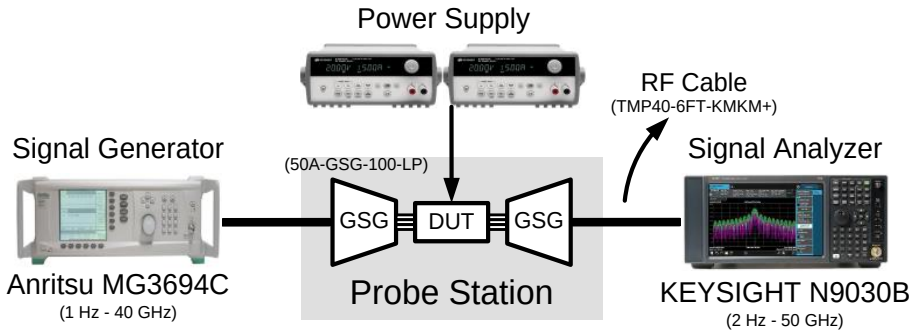
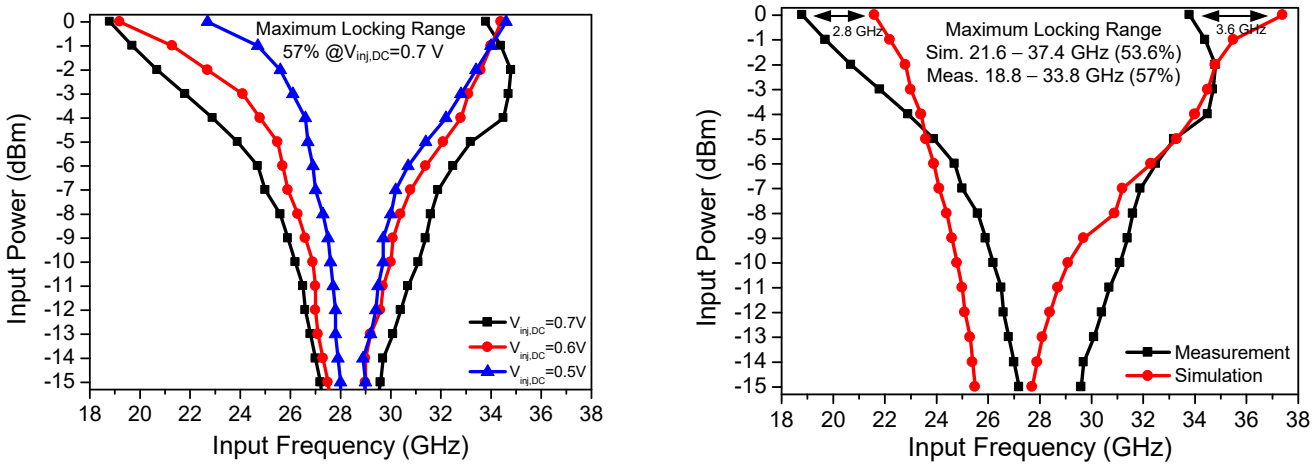


Figure 11. Measurement setup for the proposed CR-ILFD.

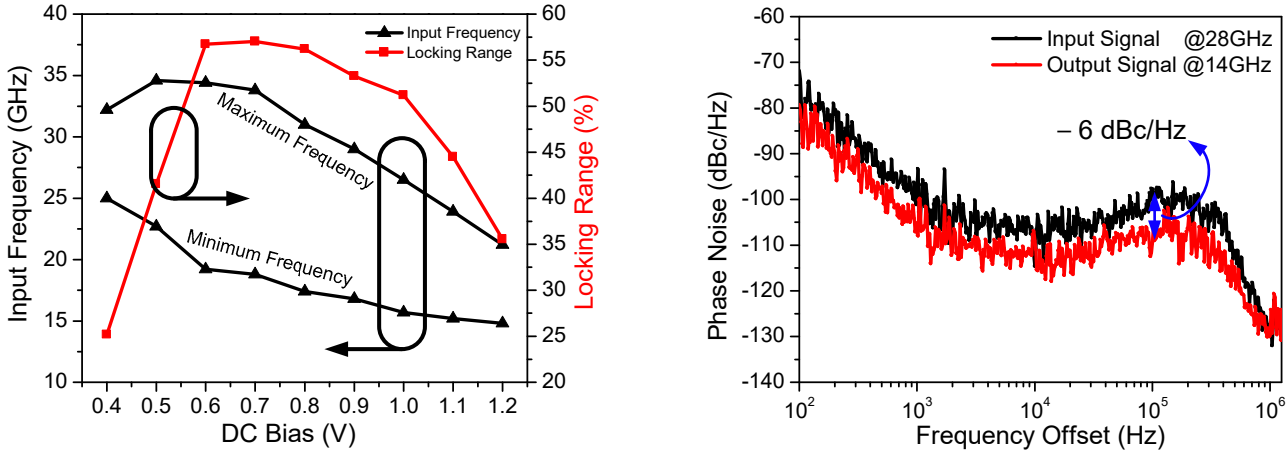
Figure 12a shows the measured locking range of the proposed CR-ILFD with different $V_{inj,DC}$ values. The maximum locking range is from 18.8 to 33.8 GHz (57%) at $V_{inj,DC}$ of 0.7 V. When the $V_{inj,DC}$ is biased to 0.6 V, the locking range is from 19.2 to 34.4 GHz (56.7%), and when the $V_{inj,DC}$ is biased to 0.5 V, the locking range is reduced from 22.7 to 34.6 GHz (41.5%). The above ranges were obtained from 0 dBm input power and 1 V supply voltage. As the $V_{inj,DC}$ decreases, the locking range also tends to decrease. Figure 12b shows a comparison of the measured and simulated locking range results of the proposed CR-ILFD. The measured locking range is 57%, and simulated locking range is from 21.6 to 37.4 GHz (53.6%). When 0 dBm input power is injected to the CR-ILFD, the measured locking range is typically changed to a lower frequency band than the simulated locking range. The operating frequency band was lowered by approximately 3 GHz. This is because of various electromagnetic components, such as RF pads, printed circuit board (PCB), and metal lines that were not considered in the simulations. The measured maximum operation frequency is higher when the input power is −3 dBm compared to when the input power is 0 dBm. This is because of the saturation of the input signal level.



(**a**) (**b**)

Figure 12. (**a**) Measured locking range results of the proposed CR-ILFD with different $V_{inj,DC}$; (**b**) measured and simulated locking range results of the proposed CR-ILFD.

Figure 13a shows the measured maximum and minimum operation frequencies of the proposed CR-ILFD with different $V_{inj,DC}$ values. This measurement was carried out with 0 dBm input power and 1 V supply voltage. $V_{inj,DC}$ is swept from 0.4 to 1.2 V, and the widest locking range is obtained at the $V_{inj,DC}$ of 0.7 V. When $V_{inj,DC}$ increases from 0.7 V, the maximum and minimum operation frequencies decrease, and the locking range also decreases.

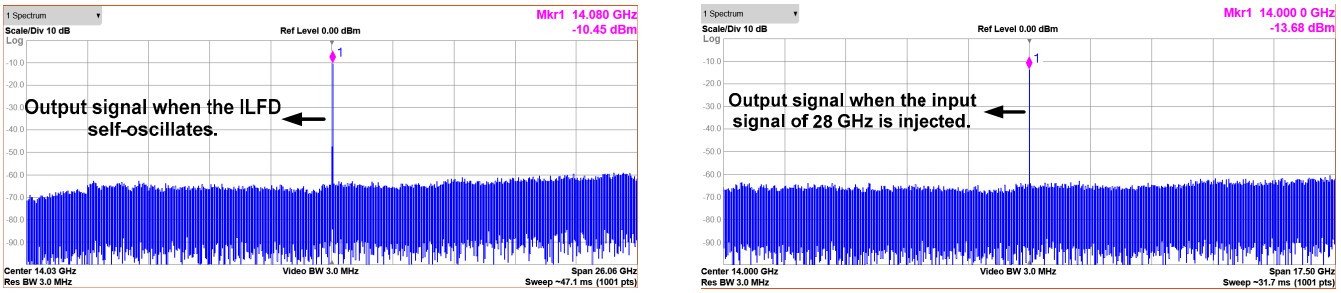


(**a**) (**b**)

Figure 13. (**a**) Measured maximum and minimum operation frequency of the proposed CR-ILFD with different $V_{inj,DC}$; (**b**) Measured phase noise of input and output signal.

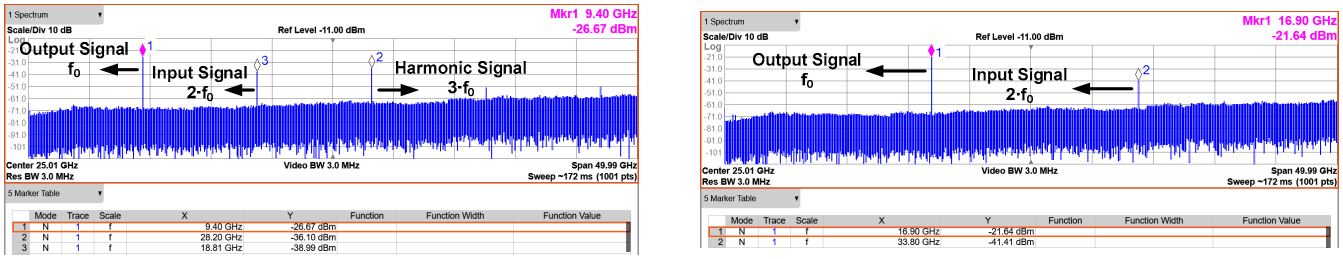
The measured phase noise of the input and output signal is shown in Figure 13b. The 28 GHz input signal is generated by Anritsu MG3694, which is applied to the proposed CR-ILFD and the output signal is 14 GHz. The phase noise of the output signal is −109.57 and −129.81 dBc/Hz at 100 kHz and 1 MHz offset frequency, respectively. The phase noise of the output signal should be measured at 6 dBc/Hz lower than that of the input signal because the input signal frequency is twice that of the output signal. Figures 14 and 15 show the results of several spectrums of the CR-ILFD's output signal measured using the KEYSIGHT N9030B. The spectrum of the output signal when the proposed CR-ILFD self-oscillates is shown in Figure 14a. The output frequency is 14.08 GHz, and output

power is −10.45 dBm. If the loss of the RF cable and GSG probe tip is calibrated, the output power will be approximately −5 dBm. The spectrum of the output signal when the 28 GHz input signal is injected to the proposed CR-ILFD is shown in Figure 14b. The frequency of the output signal is 14 GHz, which is exactly half the frequency of the input signal. The output power is approximately −8 dBm with loss calibration. Figure 15a shows the full span spectrum when the minimum input frequency, 18.8 GHz, is injected. Three tones are visible in the spectrum: the output signal (f_0), input signal ($2f_0$), and harmonic signal ($3f_0$). As shown in Figure 3, several harmonic components are amplified at output when the minimum input frequency is injected to the CR-ILFD. Locking is possible even if a lower input frequency is injected. However, the input signal is amplified such that the power difference from the output signal is less than 10 dB. When 18.8 GHz is injected, the power difference between the desired output signal and the harmonic signal is approximately 10 dB. Figure 15b shows the full span spectrum when the maximum frequency input signal of 33.8 GHz is injected. The power difference between the output and input signals is more about 20 dB. It can be observed that the amplified input signal is smaller when the maximum input frequency is injected than when the minimum input frequency is injected. As a result, harmonic rejection ratio of the input signal over the entire locking range is more than 10 dBc.



(**a**) (**b**)

Figure 14. Spectrums of the output signal (**a**) when the proposed CR-ILFD self-oscillates; (**b**) when the proposed CR-ILFD is locked with a 28 GHz injection signal.



(**a**) (**b**)

Figure 15. Full span spectrums (**a**) when the minimum input frequency is injected (18.8 GHz); (**b**) when the maximum input frequency is injected (33.8 GHz). The power difference between the output and input signals is approximately 10 dB or more.

Table 2 summarizes the performance comparison of different core ILFDs. These include challenging and typical ILFD cores such as Darlington [30], Armstrong [31], Colpitts [32], and cross-coupled pair [33–35]. This work has the highest figure of merit (FOM) compared to other ILFDs presented in Table 2.

Table 2. Performance comparison of different core ILFDs.

	This Work	**[30] 15′MTT**	**[31] 09′MWCL**	**[32] 08′MWCL**	**[33] 14′MWCL**	**[34] 15′APMC**	**[35] 17′MWCL**
Technology	65-nm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm SiGe BiCMOS	0.18-µm CMOS	0.18-µm CMOS
Core topology	Current reuse	Darlington	Armstrong	Colpitts + Current reuse	Complementary cross-coupled pair	NMOS cross-coupled pair	NMOS cross-coupled pair
Self-oscillation frequency (GHz)	14.08	N/A	4.77–5.08 (w/varactor)	5.85–6.17 (w/varactor)	N/A	N/A	2.97–4.66 (w/varactor)
Input signal power (dBm)	0	0	0	0	0	0	0
Division ratio	2	2	2	2	2	2	4
Input frequency range (GHz)	18.8–33.8	20.5–22.9	7.7–11.5	7.3–14.4	20.1–25.9	10.2–15.5	13–19
Locking range (%)	57	11	39.6	65.4	25.1	41.4	37.5 *
Supply voltage (V)	1	1.2	1.4	1.5	1.8	1.2	0.8
Power consumption of core (mW)	2.26	1.73	9.02	7.65	4.8	2.71	7.09
Phase noise (dBc/Hz @1 MHz)	−129.81 (14 GHz)	−138.3 (N/A)	−134.942 (4.9 GHz)	−134.8 (6 GHz)	−124 (12.5 GHz)	−120.53 (5.495 GHz) @ 100 kHz	−133.26 (4 GHz)
FOM_1 (GHz/mW)	6.64	1.38	0.42	0.93	1.21	1.96	0.85
FOM_2 (GHz/mW)	13.28	2.76	0.84	1.86	2.42	3.92	3.4
Chip size (mm^2)	0.75 × 0.45	0.8 × 0.75	0.55 × 0.74	0.46 × 0.52	0.75 × 0.78	0.57 × 0.68	1.01 × 1.18

FOM_1 = Input frequency range/power consumption [GHz/mW], FOM_2 = (Input frequency range × division ratio)/power consumption [GHz/mW], *: Total locking range (low band + high band).

Table 3 summarizes the performance comparison of the mm-Wave ILFDs [36–41]. ILFDs with division ratio greater than two are also included such as four [37,38] and six [41], but still have the highest FOM_1 values.

Table 3. Performance comparison of mm-Wave ILFDs.

	This Work	[36] 15′MWCL	[37] 13′TCAS1	[38] 11′MTT	[39] 17′JSSC	[40] 09′ISSCC	[41] 20′MWCL
Technology	65-nm CMOS	65-nm CMOS	65-nm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	90-nm CMOS
Self-oscillation frequency (GHz)	14.08	17.5	N/A	5.9	25.9	N/A	9.7
Input signal power (dBm)	0	0	0	0	0	0	−5
Division ratio	2	2	4	4	2	2	6
Input frequency range (GHz)	18.8–33.8	31.7–39.3	58.5–72.9	13.5–30.5	35–4441–59.5	35.6–39.3	54.5–60.1
Locking range (%)	57	21.4	21.9	77.3	53 *	9.9	9.8
Supply Voltage (V)	1	1	0.6	1.4	1.15	1	N/A
Power consumption of core (mW)	2.26	2.5	2.2	7.3	3.8	3.12	5.6
Phase noise (dBc/Hz @1 MHz)	–129.81 (14 GHz)	–102 (N/A)	–126.74 (N/A)	–137.4 (6 GHz)	–124 (24 GHz)	–133.7 (N/A)	–140 (9.7 GHz)
FOM_1 (GHz/mW)	6.64	3.04	6.54	2.33	6.45	1.19	1
FOM_2 (GHz/mW)	13.28	6.08	26.16	9.32	12.9	2.38	6
Chip size (mm^2)	0.75 × 0.45	0.6 × 0.75	0.16 × 0.26	0.52 × 0.64	1 × 0.9	0.13 × 0.18 **	0.83 × 0.61

*: Total locking range (low band + high band), **: Only core size.

5. Conclusions

This paper presents the wide locking range and low-power divide-by-two CR-ILFD. The fourth-order resonator is applied to extend the narrow operating range of the ILFD. In addition, the CR core decreases the power consumption. The input frequency locking range is from 18.8 to 33.8 GHz (57%) at an injection power of 0 dBm. The full-span spectrums at the maximum or minimum frequency are presented. The power difference between the output and harmonic signals is approximately 10 dB or more over the entire locking range. The proposed CR-ILFD dissipates 2.26 mW from a 1 V supply voltage and the die size is 0.75 mm × 0.45 mm. This CR-ILFD is implemented in a 65 nm CMOS technology.

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